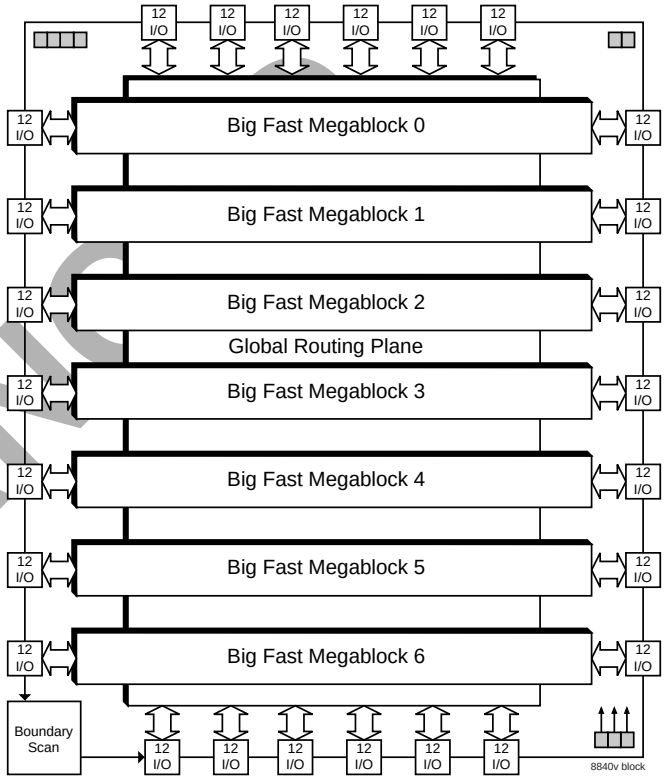
ispLSI® 8840V

3.3V In-System Programmable SuperBIG™ High Density PLD

Features

- **SuperBIG HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **— 3.3V Power Supply**
  - **— 45,000 PLD Gates/840 Macrocells**
  - **— 312 I/O Pins Supporting 3.3V/2.5V I/O**
  - **— 1152 Registers**
  - **— High-Speed Global and Big Fast Megablock (BFM) Interconnect**
  - **— Wide 20-Macrocell Generic Logic Block (GLB) for High Performance**
  - **— Wide Input Gating (44 Inputs per GLB) for Fast Counters, State Machines, Address Decoders, Etc.**
  - **— PCB-Efficient Ball Grid Array (BGA) Package Options**
- **HIGH-PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 110 MHz Maximum Operating Frequency**
  - **— t_{pd} = 8.5 ns Propagation Delay**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— Programmable Speed/Power Logic Path Optimization**
- **IN-SYSTEM PROGRAMMABLE**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE AND 3.3V IN-SYSTEM PROGRAMMABLE**
- **ARCHITECTURE FEATURES**
  - **— Enhanced Pin-Locking Architecture, Symmetrical Generic Logic Blocks Connected by Hierarchical Big Fast Megablock and Global Routing Planes**
  - **— Product Term Sharing Array Supports up to 28 Product Terms per Macrocell Output**
  - **— Macrocells Support Concurrent Combinatorial and Registered Functions**
  - **— Embedded Tristate Bus Can Be Used as an Internal Tristate Bus or as an Extension of an External Tristate Bus**
  - **— Macrocell and I/O Registers Feature Multiple Control Options, Including Set, Reset and Clock Enable**
  - **— I/O Pins Support Programmable Bus Hold, Pull-Up, Open-Drain and Slew Rate Options**
  - **— Separate VCCIO Power Supply to Support 3.3V or 2.5V Input/Output Logic Levels**
  - **— I/O Cell Register Programmable as Input Register for Fast Setup Time or Output Register for Fast Clock to Output Time**
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram



ispLSI 8000V Family Description

The ispLSI 8000V Family of Register-Intensive, 3.3V SuperBIG In-System Programmable Logic Devices is based on Big Fast Megablocks of 120 registered macrocells and a Global Routing Plane (GRP) structure interconnecting the Big Fast Megablocks. Each Big Fast Megablock contains 120 registered macrocells arranged in six groups of 20, a group of 20 being referred to as a Generic Logic Block, or GLB.

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