



## Intel386™ CXSA EMBEDDED MICROPROCESSOR

- **Static Intel386™ CPU Core**
  - Low Power Consumption
  - Operating Power Supply
    - 4.5V to 5.5V - 25 and 33 MHz
    - 4.75V to 5.25V - 40 MHz
  - Operating Frequency
    - SA-40 = 40 MHz
    - SA-33 = 33 MHz
    - SA-25 = 25 MHz
- **Transparent Power-management System Architecture**
  - Intel System Management Mode Architecture Extension for Truly Compatible Systems
  - Power Management Transparent to Operating Systems and Application Programs
  - Programmable Power-management Modes
- **Clock Freeze Mode Allows Clock Stopping at Any Time**
- **Full 32-bit Internal Architecture**
  - 8-, 16-, 32-bit Data Types
  - 8 General Purpose 32-bit Registers
- **Runs Intel386 Architecture Software in a Cost-effective, 16-bit Hardware Environment**
  - Runs Same Applications and Operating Systems as the Intel386 SX and Intel386 DX Processors
  - Object Code Compatible with 8086, 80186, 80286, and Intel386 Processors
- **High-performance 16-bit Data Bus**
  - Two-clock Bus Cycles
  - Address Pipelining Allows Use of Slower, Inexpensive Memories
- **Integrated Memory Management Unit (MMU)**
  - Virtual Memory Support
  - Optional On-chip Paging
  - 4 Levels of Hardware-enforced Protection
  - MMU Fully Compatible with Those of the 80286 and Intel386 DX Processors
- **Virtual 8086 Mode Allows Execution of 8086 Software in a Protected and Paged System**
- **Large, Uniform Address Space**
  - 64 Megabyte Physical
  - 64 Terabyte Virtual
  - 4 Gigabyte Maximum Segment Size
- **Numerics Support with Intel387™ SX and Intel387 SL Math Coprocessors**
- **On-chip Debugging Support Including Breakpoint Registers**
- **Complete System Development Support**
- **High-speed CHMOS Technology**
- **100-pin Plastic Quad Flatpack Package**

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The Intel386™ CXSA embedded microprocessor is a 5-volt, 32-bit, fully static CPU with a 16-bit external data bus, a 26-bit external address bus, and Intel's System Management Mode (SMM). The Intel386 CXSA CPU brings the vast software library of the Intel386 architecture to embedded systems. It provides the performance benefits of 32-bit programming with the cost savings associated with 16-bit hardware systems.

The Intel386 CXSA microprocessor is manufactured on Intel's 0.8-micron CHMOS V process. This process provides high performance and low power consumption for power-sensitive applications. Figure 3 and Figure 4 illustrate the flexibility of low power devices with respect to temperature and frequency relationships.

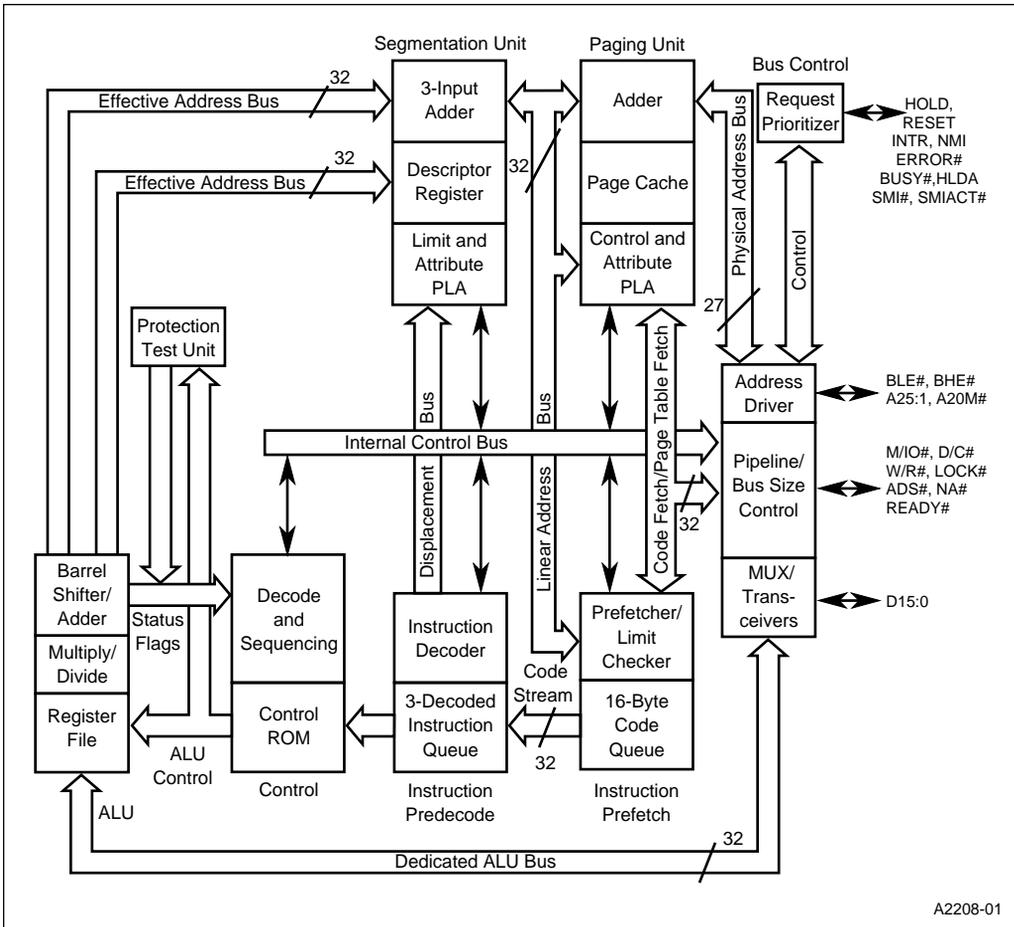


Figure 1. Intel386™ CXSA Microprocessor Block Diagram

### 1.0 PIN ASSIGNMENT

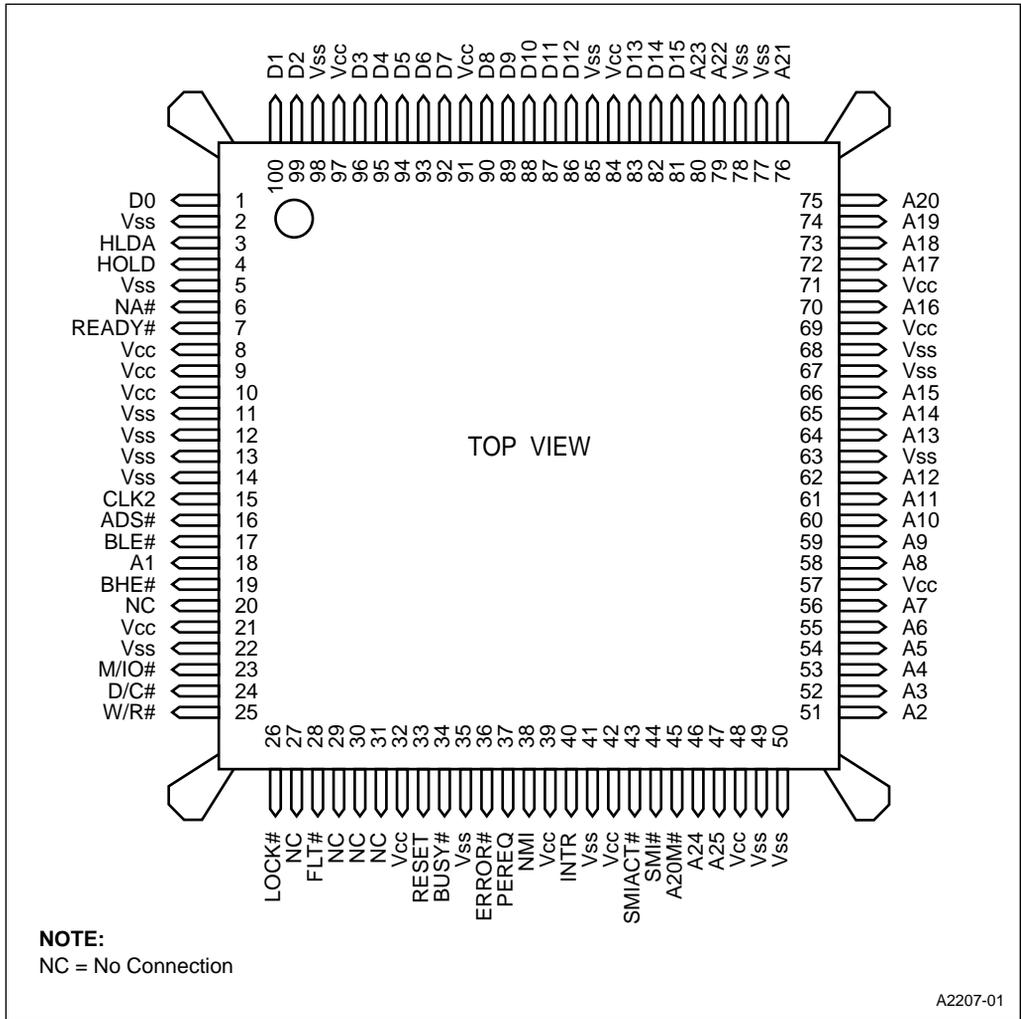


Figure 2. Intel386™ CXSA Microprocessor Pin Assignment (PQFP)

Table 1. Pin Assignment

| Pin | Symbol          | Pin | Symbol               | Pin | Symbol          | Pin | Symbol          |
|-----|-----------------|-----|----------------------|-----|-----------------|-----|-----------------|
| 1   | D0              | 26  | LOCK#                | 51  | A2              | 76  | A21             |
| 2   | V <sub>SS</sub> | 27  | NC                   | 52  | A3              | 77  | V <sub>SS</sub> |
| 3   | HLDA            | 28  | FLT#                 | 53  | A4              | 78  | V <sub>SS</sub> |
| 4   | HOLD            | 29  | NC                   | 54  | A5              | 79  | A22             |
| 5   | V <sub>SS</sub> | 30  | NC                   | 55  | A6              | 80  | A23             |
| 6   | NA#             | 31  | NC                   | 56  | A7              | 81  | D15             |
| 7   | READY#          | 32  | V <sub>CC</sub>      | 57  | V <sub>CC</sub> | 82  | D14             |
| 8   | V <sub>CC</sub> | 33  | RESET                | 58  | A8              | 83  | D13             |
| 9   | V <sub>CC</sub> | 34  | BUSY#                | 59  | A9              | 84  | V <sub>CC</sub> |
| 10  | V <sub>CC</sub> | 35  | V <sub>SS</sub>      | 60  | A10             | 85  | V <sub>SS</sub> |
| 11  | V <sub>SS</sub> | 36  | ERROR#               | 61  | A11             | 86  | D12             |
| 12  | V <sub>SS</sub> | 37  | PEREQ                | 62  | A12             | 87  | D11             |
| 13  | V <sub>SS</sub> | 38  | NMI                  | 63  | V <sub>SS</sub> | 88  | D10             |
| 14  | V <sub>SS</sub> | 39  | V <sub>CC</sub>      | 64  | A13             | 89  | D9              |
| 15  | CLK2            | 40  | INTR                 | 65  | A14             | 90  | D8              |
| 16  | ADS#            | 41  | V <sub>SS</sub>      | 66  | A15             | 91  | V <sub>CC</sub> |
| 17  | BLE#            | 42  | V <sub>CC</sub>      | 67  | V <sub>SS</sub> | 92  | D7              |
| 18  | A1              | 43  | SMI <sub>ACT</sub> # | 68  | V <sub>SS</sub> | 93  | D6              |
| 19  | BHE#            | 44  | SMI#                 | 69  | V <sub>CC</sub> | 94  | D5              |
| 20  | NC              | 45  | A20M#                | 70  | A16             | 95  | D4              |
| 21  | V <sub>CC</sub> | 46  | A24                  | 71  | V <sub>CC</sub> | 96  | D3              |
| 22  | V <sub>SS</sub> | 47  | A25                  | 72  | A17             | 97  | V <sub>CC</sub> |
| 23  | M/IO#           | 48  | V <sub>CC</sub>      | 73  | A18             | 98  | V <sub>SS</sub> |
| 24  | D/C#            | 49  | V <sub>SS</sub>      | 74  | A19             | 99  | D2              |
| 25  | W/R#            | 50  | V <sub>SS</sub>      | 75  | A20             | 100 | D1              |

## 2.0 PIN DESCRIPTIONS

Table 2 lists the Intel386 CXSA microprocessor pin descriptions. The following definitions are used in the pin descriptions:

- # The named signal is active low.
- I Input signal.
- O Output signal.
- I/O Input and output signal.
- P Power pin.
- G Ground pin.

**Table 2. Pin Descriptions**

| Symbol            | Type | Pin  | Name and Function   |
|-------------------|------|--|---|
| A20M#<br>(Note 1) | I    | 45   | <b>Address 20 Mask</b> controls the A20 address signal. When A20M# is low, the CPU masks off (forces low) the internal A20 physical address signal. This enables the CPU to run software that was developed using the 8086 address “wraparound” techniques. When A20M# is high, A20 is available on the address bus. While the bus is floating, A20M# has no effect on the A20 address signal. A20M# should be deasserted during SMM if the SMM handler accesses more than 1 Mbyte of memory. |
| A25:1<br>(Note 2) | O    | 47–46, 80–79,<br>76–72, 70, 66–<br>64, 62–58,<br>56–51, 18 | <b>Address Bus</b> outputs physical memory or port I/O addresses.   |
| ADS#              | O    | 16   | <b>Address Status</b> indicates that the processor is driving a valid bus-cycle definition and address onto its pins (W/R#, D/C#, M/I/O#, BHE#, BLE#, and A25:1).   |
| BHE#              | O    | 19   | <b>Byte High Enable</b> indicates that the processor is transferring a high data byte.  |
| BLE#              | O    | 17   | <b>Byte Low Enable</b> indicates that the processor is transferring a low data byte.  |
| BUSY#             | I    | 34   | <b>Busy</b> indicates that the math coprocessor is busy.  |
| CLK2              | I    | 15   | <b>CLK2</b> provides the fundamental timing for the device.   |
| D/C#              | O    | 24   | <b>Data/Control</b> indicates whether the current bus cycle is a data cycle (memory or I/O) or a control cycle (interrupt acknowledge, halt, or code fetch). When D/C# is high, the bus cycle is a data cycle; when D/C# is low, the bus cycle is a control cycle.  |
| D15:0             | I/O  | 81–83, 86–90,<br>92–96, 99–100,<br>1                       | <b>Data Bus</b> inputs data during memory read, I/O read, and interrupt acknowledge cycles and outputs data during memory and I/O write cycles.   |

**NOTES:**

1. This pin supports the additional features of the Intel386 CXSA microprocessor; it is not present on the Intel386 SXSA microprocessor.
2. The A25:24 pins support the additional features of the Intel386 CXSA microprocessor; they are not present on the Intel386 SXSA microprocessor.

Table 2. Pin Descriptions (Continued)

| Symbol | Type | Pin           | Name and Function   |
|--------|------|---------------|---|
| ERROR# | I    | 36            | <b>Error</b> indicates that the math coprocessor has an error condition.  |
| FLT#   | I    | 28            | <b>Float</b> forces all bidirectional and output signals, including HLDA, to a high-impedance state.  |
| HLDA   | O    | 3             | <b>Bus Hold Acknowledge</b> indicates that the CPU has surrendered control of its local bus to another bus master.  |
| HOLD   | I    | 4             | <b>Bus Hold Request</b> allows another bus master to request control of the local bus.  |
| INTR   | I    | 40            | <b>Interrupt Request</b> is a maskable input that causes the CPU to suspend execution of the current program and then execute an interrupt acknowledge cycle.   |
| LOCK#  | O    | 26            | <b>Bus Lock</b> prevents other system bus masters from gaining control of the system bus while it is active (low).  |
| M/IO#  | O    | 23            | <b>Memory/IO</b> indicates whether the current bus cycle is a memory cycle or an input/output cycle. When M/IO# is high, the bus cycle is a memory cycle; when M/IO# is low, the bus cycle is an I/O cycle. |
| NA#    | I    | 6             | <b>Next Address</b> requests address pipelining.  |
| NC     |      | 20, 27, 29–31 | <b>No Connection</b> should always be left unconnected. Connecting a NC pin may cause the processor to malfunction or cause your application to be incompatible with future steppings of the device.        |
| NMI    | I    | 38            | <b>Nonmaskable Interrupt Request</b> is a nonmaskable input that causes the CPU to suspend execution of the current program and execute an interrupt acknowledge function.                                  |
| PEREQ  | I    | 37            | <b>Processor Extension Request</b> indicates that the math coprocessor has data to transfer to the processor.   |
| READY# | I    | 7             | <b>Bus Ready</b> indicates that the current bus cycle is finished and the external device is ready to accept more data from the processor.  |
| RESET  | I    | 33            | <b>Reset</b> suspends any operation in progress and places the processor into a known reset state.  |

**NOTES:**

1. This pin supports the additional features of the Intel386 CXSA microprocessor; it is not present on the Intel386 SXSA microprocessor.
2. The A25:24 pins support the additional features of the Intel386 CXSA microprocessor; they are not present on the Intel386 SXSA microprocessor.

**Table 2. Pin Descriptions** (Continued)

| Symbol              | Type | Pin  | Name and Function   |
|---------------------|------|--|---|
| SMI#<br>(Note 1)    | I    | 44   | <b>System Management Interrupt</b> invokes System Management Mode (SMM). SMI# is the highest priority interrupt. It is latched on its falling edge and it forces the CPU into SMM upon completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# cannot interrupt LOCKed bus cycles or a currently executing SMM. If the processor receives a second SMI# while it is in SMM, it will latch the second SMI# on the SMI# falling edge. However, the processor must exit SMM by executing a Resume instruction (RSM) before it can service the second SMI#. |
| SMIACT#<br>(Note 1) | O    | 43   | <b>System Management Interrupt Active</b> indicates that the processor is operating in System Management Mode (SMM). It is asserted when the processor initiates an SMM sequence and remains asserted (low) until the processor executes the Resume instruction (RSM).  |
| W/R#                | O    | 25   | <b>Write/Read</b> indicates whether the current bus cycle is a write cycle or a read cycle. When W/R# is high, the bus cycle is a write cycle; when W/R# is low, it is a read cycle.  |
| V <sub>CC</sub>     | P    | 8–10, 21, 32, 39, 42, 48, 57, 69, 71, 84, 91, 97         | <b>System Power</b> provides the nominal DC supply input.   |
| V <sub>SS</sub>     | G    | 2, 5, 11–14, 22, 35, 41, 49–50, 63, 67–68, 77–78, 85, 98 | <b>System Ground</b> provides the 0V connection from which all inputs and outputs are measured.   |

**NOTES:**

1. This pin supports the additional features of the Intel386 CXSA microprocessor; it is not present on the Intel386 SXSA microprocessor.
2. The A25:24 pins support the additional features of the Intel386 CXSA microprocessor; they are not present on the Intel386 SXSA microprocessor.

### 3.0 DESIGN CONSIDERATIONS

This section describes the Intel386 CXSA microprocessor instruction set, component and revision identifier, and package thermal specifications.

#### 3.1. Instruction Set

The Intel386 CXSA microprocessor uses the same instruction set as the Intel386 SX microprocessor with the following exceptions.

The Intel386 CXSA microprocessor has one new instruction (RSM). This Resume instruction causes the processor to exit System Management Mode (SMM). RSM requires 338 clocks for execution.

The Intel386 CXSA microprocessor requires more clock cycles than the Intel386 SX microprocessor to execute some instructions. Table 4 lists these instructions and the Intel386 CXSA microprocessor execution times. For the equivalent Intel386 SX microprocessor execution times, refer to the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).

#### 3.2. Component and Revision Identifier

To assist users, the microprocessor holds a component identifier and revision identifier in its DX register after reset. The upper 8 bits of DX hold the component identifier, 23H. (The lower nibble, 3H, identifies the Intel386 architecture, while the upper nibble, 2H, identifies the second member of the Intel386 microprocessor family.)

The lower 8 bits of DX hold the revision level identifier. The revision identifier will, in general, chronologically track those component steppings that are intended to have certain improvements or distinction from previous steppings. The revision identifier will track that of the Intel386 CPU whenever possible. However, the revision identifier value is not guaranteed to change with every stepping revision or to follow a completely uniform numerical sequence, depending on the type or intent of the revision or the manufacturing materials

required to be changed. Intel has sole discretion over these characteristics of the component. The initial revision identifier for the Intel386 CXSA microprocessor is 09H.

#### 3.3. Package Thermal Specifications

The Intel386 CXSA microprocessor is specified for operation with case temperature ( $T_{CASE}$ ) as specified in the "DC SPECIFICATIONS" on page 10. The case temperature can be measured in any environment to determine whether the microprocessor is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

An increase in the ambient temperature ( $T_A$ ) causes a proportional increase in the case temperature ( $T_{CASE}$ ) and the junction temperature ( $T_J$ ). See Figures 3 and Figures 4 for case and ambient temperature relationships to frequency. A packaged device produces thermal resistance between junction and case temperatures ( $\theta_{JC}$ ) and between junction and ambient temperatures ( $\theta_{JA}$ ). The relationships between the temperature and thermal resistance parameters are expressed by these equations ( $P$  = power dissipated as heat =  $V_{CC} \times I_{CC}$ ):

1.  $T_J = T_{CASE} + P \times \theta_{JC}$
2.  $T_A = T_J - P \times \theta_{JA}$
3.  $T_{CASE} = T_A + P \times [\theta_{JA} - \theta_{JC}]$

A safe operating temperature can be calculated from equation 1 by using the maximum safe  $T_J$  of 115° C, the maximum power drawn by the chip in the specific design, and the  $\theta_{JC}$  value from Table 3. The  $\theta_{JA}$  value depends on the airflow (measured at the top of the chip) provided by the system ventilation. The  $\theta_{JA}$  values are given for reference only and are not guaranteed.

**Table 3. Thermal Resistances (0°C/W)  $\theta_{JA}$ ,  $\theta_{JC}$**

| Pkg      | $\theta_{JC}$ | $\theta_{JA}$ versus Airflow (ft/min) |      |      |
|----------|---------------|---------------------------------------|------|------|
|          |               | 0                                     | 100  | 200  |
| 100 PQFP | 5.1           | 46.0                                  | 44.8 | 41.2 |

**Table 4. Intel386™ CXSA Microprocessor Instruction Execution Times (in Clock Counts)**

| Instruction                         | Clock Count                   |   |   |
|-------------------------------------|-------------------------------|---|---|
|                                     | Virtual 8086 Mode<br>(Note 1) | Real Address Mode<br>or Virtual 8086 Mode | Protected Virtual<br>Address Mode<br>(Note 3) |
| POPA                                |                               | 28  | 35  |
| IN:<br>Fixed Port<br>Variable Port  | 27<br>28                      | 14<br>15                                  | 7/29<br>8/29                                  |
| OUT:<br>Fixed Port<br>Variable Port | 27<br>28                      | 14<br>15                                  | 7/29<br>9/29                                  |
| INS                                 | 30                            | 17  | 9/32  |
| OUTS                                | 31                            | 18  | 10/33   |
| REP INS                             | 31+6n (Note 2)                | 17+6n (Note 2)                            | 10+6n/32+6n (Note 2)                          |
| REP OUTS                            | 30+8n (Note 2)                | 16+8n (Note 2)                            | 10+8n/31+8n (Note 2)                          |
| HLT                                 |                               | 7   | 7   |
| MOV C0, reg                         |                               | 10  | 10  |

**NOTES:**

1. The clock count values in this column apply if I/O permission allows I/O to the port in virtual 8086 mode. If the I/O bit map denies permission, exception fault 13 occurs; see clock counts for the INT 3 instruction in the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).
2. n = the number of times repeated.
3. When two clock counts are listed, the smaller value refers to a register operand and the larger value refers to a memory operand.

## 4.0 DC SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS\*

|   |                          |
|---|--------------------------|
| Storage Temperature .....                     | -65°C to +150°C          |
| Case Temperature Under Bias .....             | -65°C to +112°C          |
| Supply Voltage with Respect to $V_{SS}$ ..... | -0.5V to 6.5V            |
| Voltage on Other Pins .....                   | -0.5V to $V_{CC} + 0.5V$ |

### OPERATING CONDITIONS\*

|  |                 |
|--|-----------------|
| $V_{CC}$ (Digital Supply Voltage - 25 and 33 MHz) ...  | 4.5V to 5.5V    |
| $V_{CC}$ (Digital Supply Voltage - 40 MHz) .....       | 4.75V to 5.25V  |
| $T_{CASE}$ minimum (Case Temperature Under Bias) ..... | 0°C             |
| $T_{CASE}$ maximum .....                               | see Figure 4    |
| Operating Frequency .....                              | 0 MHz to 40 MHz |

**NOTICE:** This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**\*WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 5. DC Characteristics

| Symbol    | Parameter  | Min.                  | Max.              | Unit           | Test Condition   |
|-----------|--|-----------------------|-------------------|----------------|--|
| $V_{IL}$  | Input Low Voltage  | -0.3                  | +0.8              | V              |  |
| $V_{IH}$  | Input High Voltage   | 2.0                   | $V_{CC} + 0.3$    | V              |  |
| $V_{ILC}$ | CLK2 Input Low Voltage   | -0.3                  | +0.8              | V              |  |
| $V_{IHC}$ | CLK2 Input High Voltage  | $V_{CC} - 0.8$        | $V_{CC} + 0.3$    | V              |  |
| $V_{OL}$  | Output Low Voltage   |                       | 0.45              | V              | $I_{OL} = 5 \text{ mA}$  |
| $V_{OH}$  | Output High Voltage  | 2.4<br>$V_{CC} - 0.5$ |                   | V<br>V         | $I_{OH} = -1 \text{ mA}$<br>$I_{OH} = -0.2 \text{ mA}$                   |
| $I_{LI}$  | Input Leakage Current<br>(for all pins except PEREQ,<br>BUSY#, FLT#, ERROR#,<br>A20M#, SMI#)                         |                       | ±15               | µA             | $0 \leq V_{IN} \leq V_{CC}$  |
| $I_{IH}$  | Input Leakage Current<br>(PEREQ)   |                       | 150               | µA             | $V_{IH} = 2.4V$ (Note 1)   |
| $I_{IL}$  | Input Leakage Current<br>(BUSY#, FLT#, ERROR#,<br>A20M#, and SMI#)   |                       | -120              | µA             | $V_{IL} = 0.45V$ (Note 2)  |
| $I_{LO}$  | Output Leakage Current   |                       | ±15               | µA             | $0.45V \leq V_{OUT} \leq V_{CC}$   |
| $I_{CC}$  | Supply Current<br>CLK2 = 80 MHz, CLK = 40<br>MHz<br>CLK2 = 66 MHz, CLK = 33<br>MHz<br>CLK2 = 50 MHz, CLK = 25<br>MHz |                       | 275<br>225<br>175 | mA<br>mA<br>mA | (Notes 3, 4)<br>typical = 200 mA<br>typical = 175 mA<br>typical = 140 mA |
| $I_{CCF}$ | Standby Current (Freeze Mode)  |                       | 150               | µA             | typical = 10 µA (Notes 3, 4)   |
| $C_{IN}$  | Input Capacitance  |                       | 10                | pF             | $F_C = 1 \text{ MHz}$ (Note 5)   |

#### NOTES:

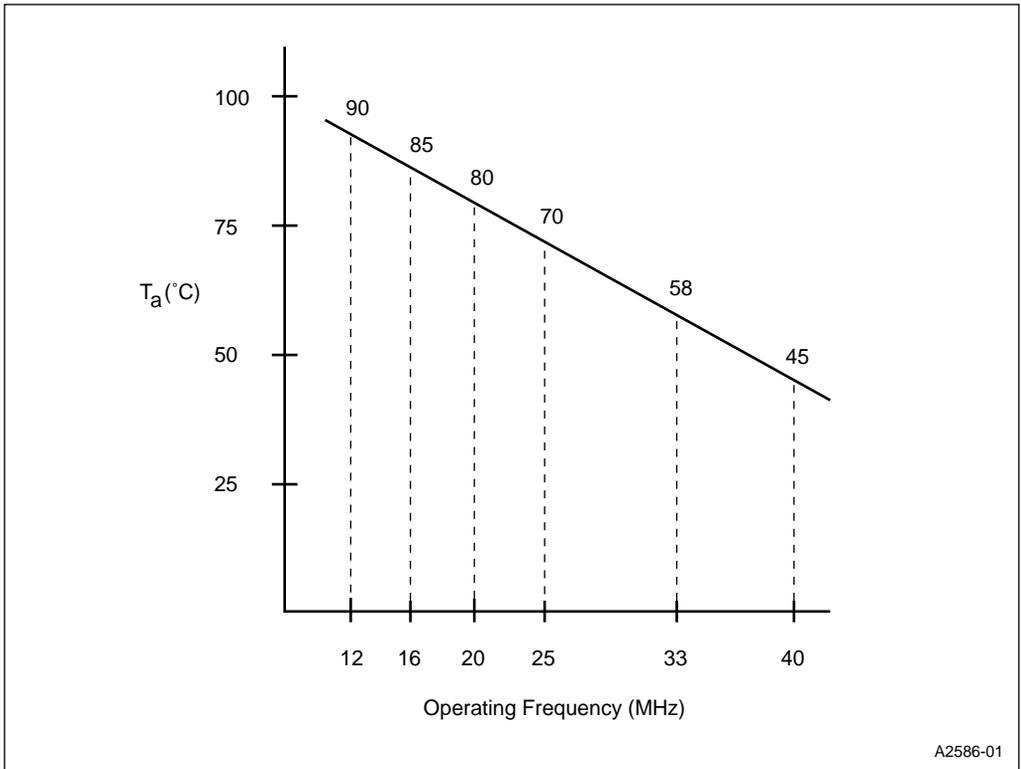
- PEREQ input has an internal weak pull-down resistor.
- BUSY#, FLT#, SMI#, A20M# and ERROR# inputs each have an internal weak pull-up resistor.
- $I_{CC}$  max measurement at worst-case frequency,  $V_{CC}$ , and temperature with reset active.
- $I_{CC}$  typical and  $I_{CCF}$  typical are measured at nominal  $V_{CC}$  and are not fully tested.
- Not fully tested.

**Table 5. DC Characteristics (Continued)**

| Symbol           | Parameter                 | Min. | Max. | Unit | Test Condition                  |
|------------------|---------------------------|------|------|------|---------------------------------|
| C <sub>OUT</sub> | Output or I/O Capacitance |      | 12   | pF   | F <sub>C</sub> = 1 MHz (Note 5) |
| C <sub>CLK</sub> | CLK2 Capacitance          |      | 20   | pF   | F <sub>C</sub> = 1 MHz (Note 5) |

**NOTES:**

1. PEREQ input has an internal weak pull-down resistor.
2. BUSY#, FLT#, SM#, A20M# and ERROR# inputs each have an internal weak pull-up resistor.
3. I<sub>CC</sub> max measurement at worst-case frequency, V<sub>CC</sub>, and temperature with reset active.
4. I<sub>CC</sub> typical and I<sub>CCF</sub> typical are measured at nominal V<sub>CC</sub> and are not fully tested.
5. Not fully tested.



**Figure 3. Ambient Temperature vs. Frequency at Zero Air Flow and T<sub>j</sub> = 115° C**

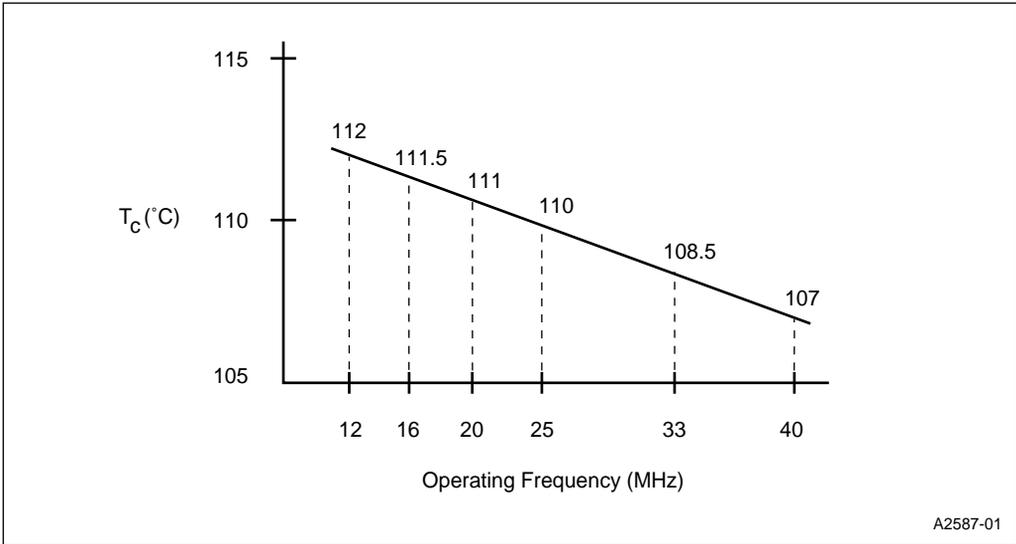


Figure 4. Case Temperature vs. Frequency at T<sub>j</sub> = 115° C

## 5.0 AC SPECIFICATIONS

Table 6 lists output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the CLK2 rising edge crossing the 2.0V level.

Figure 5 shows the measurement points for AC specifications. Inputs must be driven to the indicated voltage levels when AC specifications are measured. Output delays are specified with minimum and maximum limits measured as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest

acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs ADS#, W/R#, D/C#, MI/O#, LOCK#, BHE#, BLE#, A25:1, SMI<sup>ACT</sup># and HLDA change only at the beginning of phase one. D15:0 (write cycles) change only at the beginning of phase two.

The READY#, HOLD, BUSY#, ERROR#, PEREQ, FLT#, A20M# and D15:0 (read cycles) inputs are sampled at the beginning of phase one. The NA#, INTR, SMI# and NMI inputs are sampled at the beginning of phase two.

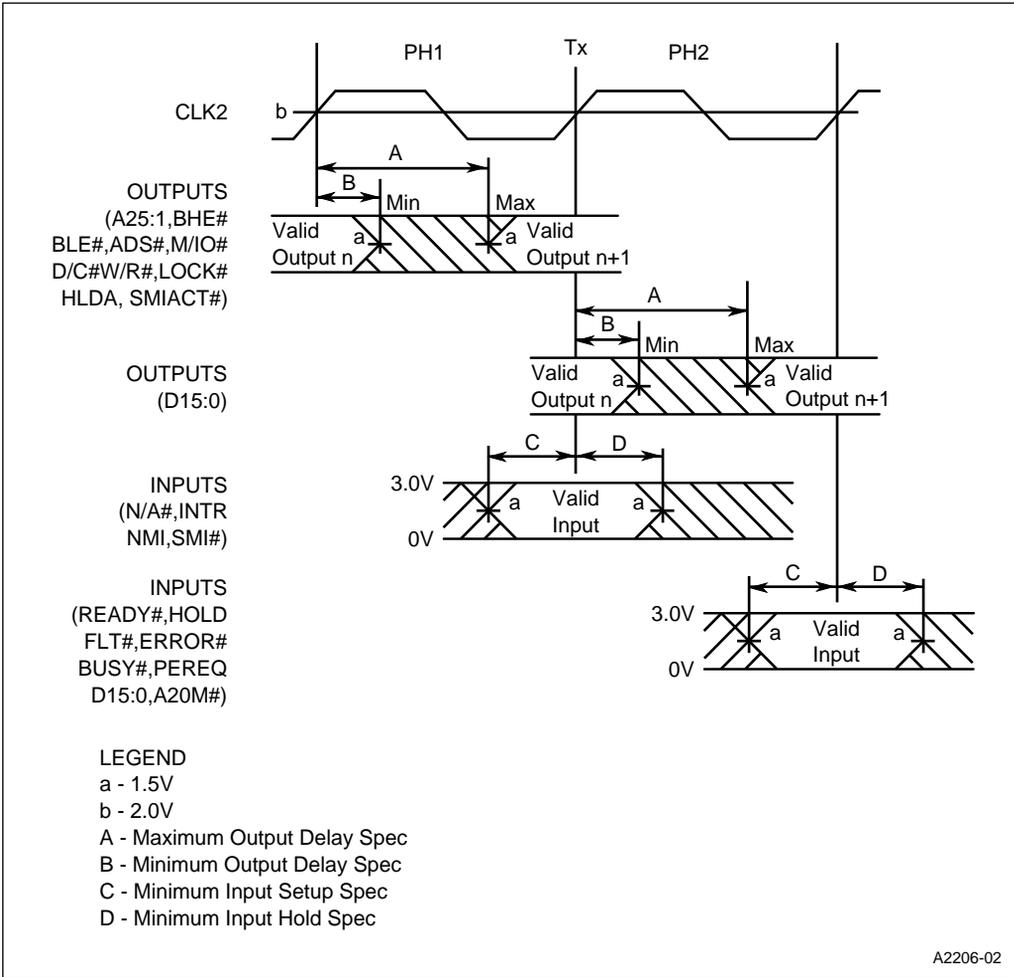


Figure 5. Drive Levels and Measurement Points for AC Specifications

**Table 6. AC Characteristics**

| Symbol | Parameter                           | 40 MHz    |           | 33 MHz    |           | 25 MHz    |           | Test Condition                  |
|--------|-------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|---------------------------------|
|        |                                     | Min. (ns) | Max. (ns) | Min. (ns) | Max. (ns) | Min. (ns) | Max. (ns) |                                 |
|        | Operating Frequency                 | 0         | 40        | 0         | 33        | 0         | 25        | MHz (Note 1)                    |
| t1     | CLK2 Period                         | 12.5      |           | 15        |           | 20        |           |                                 |
| t2a    | CLK2 High Time                      | 4.5       |           | 6.25      |           | 7         |           | (Note 2)                        |
| t2b    | CLK2 High Time                      | 3.5       |           | 4         |           | 4         |           | (Note 2)                        |
| t3a    | CLK2 Low Time                       | 4.5       |           | 6.25      |           | 7         |           | (Note 2)                        |
| t3b    | CLK2 Low Time                       | 3.5       |           | 4.5       |           | 5         |           | (Note 2)                        |
| t4     | CLK2 Fall Time                      |           | 4         |           | 4         |           | 7         | (Note 2)                        |
| t5     | CLK2 Rise Time                      |           | 4         |           | 4         |           | 7         | (Note 2)                        |
| t6     | A25:1 Valid Delay                   | 4         | 13        | 4         | 15        | 4         | 17        | C <sub>L</sub> = 50 pF          |
| t7     | A25:1 Float Delay                   | 4         | 20        | 4         | 20        | 4         | 30        | (Note 3)                        |
| t8     | BHE#, BLE#, LOCK# Valid Delay       | 4         | 13        | 4         | 15        | 4         | 17        | C <sub>L</sub> = 50 pF          |
| t8a    | SMIACK# Valid Delay                 | 4         | 13        | 4         | 15        | 4         | 17        | C <sub>L</sub> = 50 pF          |
| t9     | BHE#, BLE#, LOCK# Float Delay       | 4         | 20        | 4         | 20        | 4         | 30        | (Note 3)                        |
| t10    | W/R#, M/IO#, D/C#, ADS# Valid Delay | 4         | 13        | 4         | 15        | 4         | 17        | C <sub>L</sub> = 50 pF          |
| t11    | W/R#, M/IO#, D/C#, ADS# Float Delay | 4         | 20        | 4         | 20        | 4         | 30        | (Note 3)                        |
| t12    | D15:0 Write Data Valid Delay        | 7         | 18        | 7         | 23        | 7         | 23        | C <sub>L</sub> = 50 pF (Note 5) |
| t12a   | D15:0 Write Data Hold Time          | 2         |           | 2         |           | 2         |           | C <sub>L</sub> = 50 pF          |
| t13    | D15:0 Write Data Float delay        | 4         | 17        | 4         | 17        | 4         | 22        | (Note 3)                        |
| t14    | HLDA Valid Delay                    | 4         | 17        | 4         | 20        | 4         | 22        | C <sub>L</sub> = 50 pF          |
| t15    | NA# Setup Time                      | 5         |           | 5         |           | 5         |           |                                 |
| t16    | NA# Hold Time                       | 2         |           | 2         |           | 3         |           |                                 |
| t19    | READY#, A20M# Setup Time            | 7         |           | 7         |           | 9         |           |                                 |

**NOTES:**

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I<sub>LO</sub> in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
5. Minimum time not 100% tested.

Table 6. AC Characteristics (Continued)

| Symbol | Parameter                             | 40 MHz    |           | 33 MHz    |           | 25 MHz    |           | Test Condition |
|--------|---------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|----------------|
|        |                                       | Min. (ns) | Max. (ns) | Min. (ns) | Max. (ns) | Min. (ns) | Max. (ns) |                |
| t20    | READY#, A20M# Hold Time               | 4         |           | 4         |           | 4         |           |                |
| t21    | D15:0 Read Setup Time                 | 4         |           | 5         |           | 7         |           |                |
| t22    | D15:0 Read Hold Time                  | 3         |           | 3         |           | 5         |           |                |
| t23    | HOLD Setup Time                       | 4         |           | 9         |           | 9         |           |                |
| t24    | HOLD Hold Time                        | 2         |           | 2         |           | 3         |           |                |
| t25    | RESET Setup Time                      | 4         |           | 5         |           | 8         |           |                |
| t26    | RESET Hold Time                       | 2         |           | 2         |           | 3         |           |                |
| t27    | NMI, INTR Setup Time                  | 5         |           | 5         |           | 6         |           | (Note 4)       |
| t27a   | SMI# Setup Time                       | 5         |           | 5         |           | 6         |           | (Note 4)       |
| t28    | NMI, INTR Hold Time                   | 5         |           | 5         |           | 6         |           | (Note 4)       |
| t28a   | SMI# Hold Time                        | 5         |           | 5         |           | 6         |           | (Note 4)       |
| t29    | PEREQ, ERROR#, BUSY#, FLT# Setup Time | 5         |           | 5         |           | 6         |           | (Note 4)       |
| t30    | PEREQ, ERROR#, BUSY#, FLT# Hold Time  | 4         |           | 4         |           | 5         |           | (Note 4)       |

**NOTES:**

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than  $I_{LO}$  in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
5. Minimum time not 100% tested.

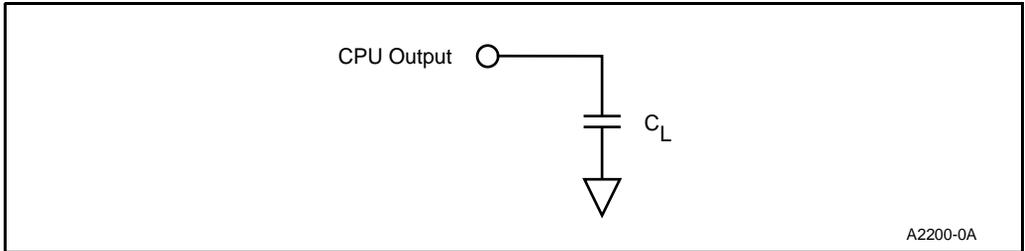


Figure 6. AC Test Loads

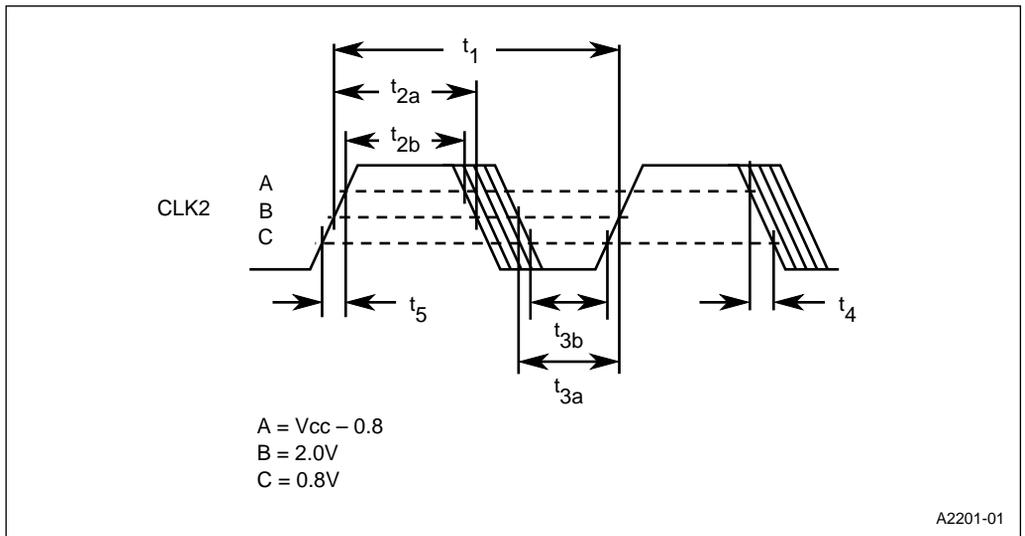


Figure 7. CLK2 Waveform

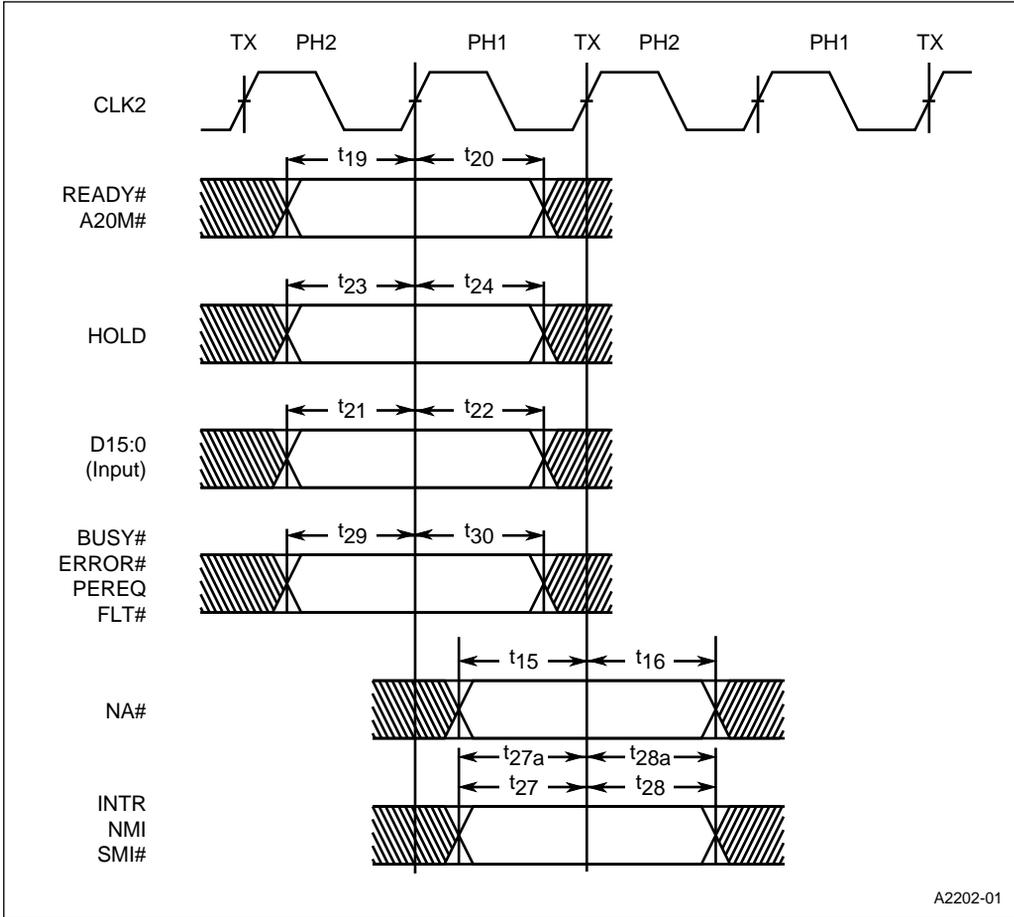


Figure 8. AC Timing Waveforms — Input Setup and Hold Timing

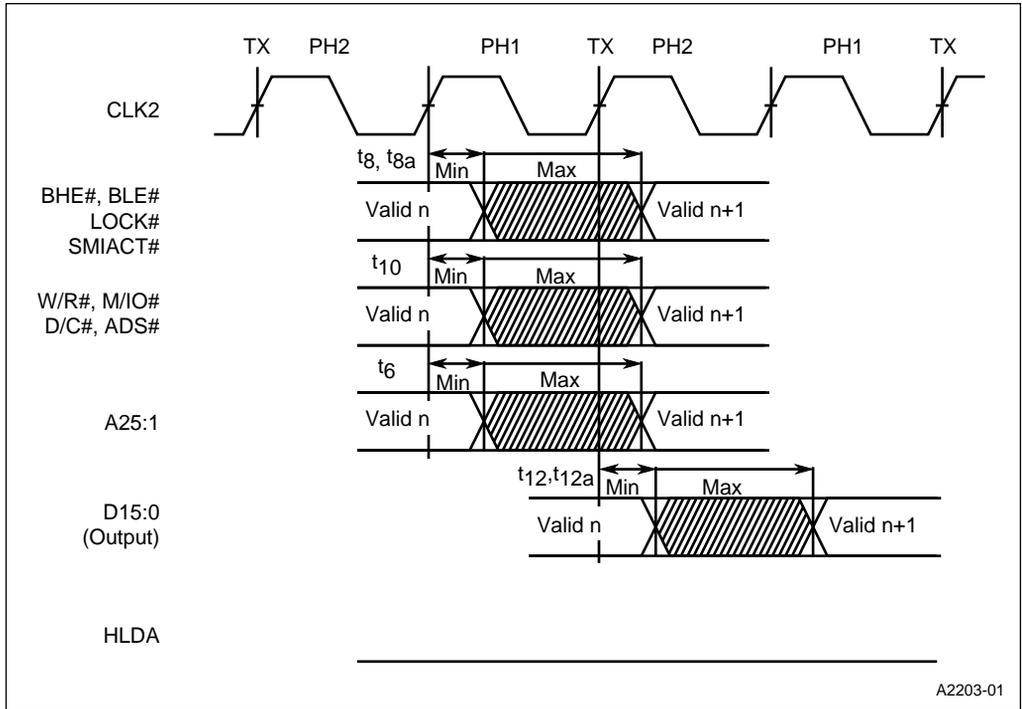


Figure 9. AC Timing Waveforms — Output Valid Delay Timing

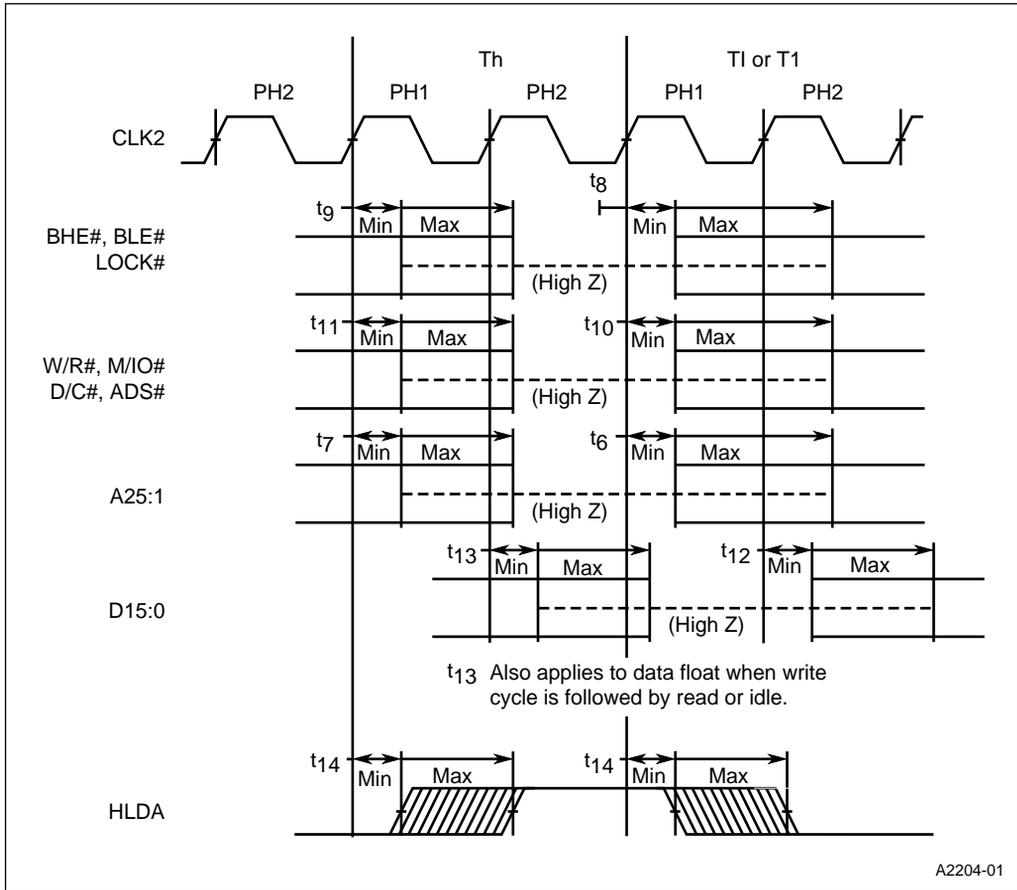


Figure 10. AC Timing Waveforms — Output Float Delay and HLDA Valid Delay Timing

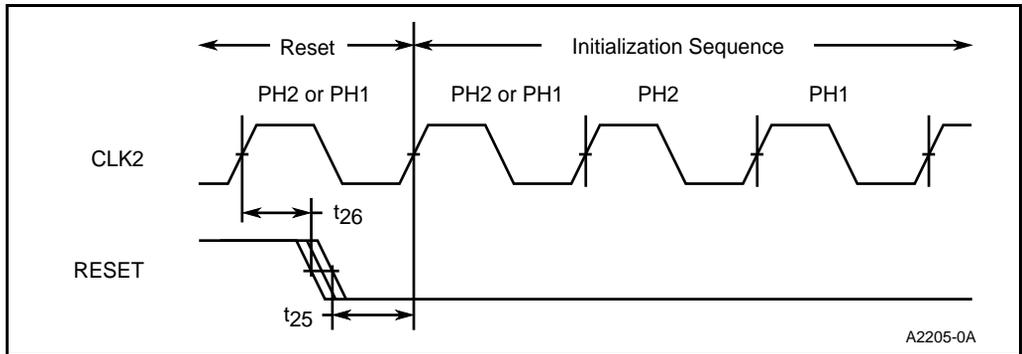


Figure 11. AC Timing Waveforms — RESET Setup and Hold Timing and Internal Phase

## 6.0 REVISION HISTORY

This -003 data sheet contains the following changes from the -002 version.

- Changed  $V_{CC}$  at 40 MHz to 4.75V to 5.25V (pages 1 and 10).
- Renamed “Powerdown Mode” to “Clock Freeze Mode” on page 1.
- Added clarifications to Figure 1.
- Corrected pin numbering for A25:1 in Table 2.
- Changed first sentence in Section 3.3 from “...on page 12” to “...on page 10.”
- Changed note 2 on page 10 to reflect A20M#
- Changed first sentence on page 13 from “Table 7 lists...” to “Table 6 lists...”
- Added INTR and A20M# to Figure 8 and removed BS8#.