



SERIAL INTERFACE PRODUCTS

Using the ISD33000 Device with 5-Volt Powered Processors

Today with the increased requirements for low voltage battery operation, many devices are offered that operate in the 3-volt range. The problem is the additional consideration that must be observed while using both 3-volt and 5-volt logic together. This brief assumes that the application requires a minimum of additional logic to interface the ISD33000 series powered at 3 volts to any microprocessor/controller powered at 5 volts.

The ISD33000 ChipCorder series provides high quality, 3-volt single chip record/playback solution for 1- to 4-minute message applications. Since the ISD33000 was designed to be used in conjunction with a microprocessor/controller, all addressing and control function are accomplished through a Serial Peripheral Interface (SPI) or microwire serial interface.

The I/O pads of the ISD33000 were designed without the need for the P channel device for ESD protection. Thus no level translation is required when connecting a 5-volt device to the inputs of the ISD33000. You may directly connect to any input on the ISD33000 from a 5-volt device.

All the outputs (except for MISO) are open drain, so if you would be connecting them to a device powered at 5 volt, simply pull up the output on the ISD33000 to the +5 volt supply of the microprocessor/controller.

The MISO output is the only exception on the ISD33000, and does include a P channel drive. At a +3 volt V_{CC} for the ISD33000, the specification will guarantee a minimum V_{OH} (output high voltage minimum) of $V_{CC}-0.4$ or +2.6 volts. Most +5 volt devices require a VIH (input high voltage minimum) in the range of +4 volts. To meet the V_{IH} specification of the +5 volt device we must add a level translation.

If the application can tolerate this pin being inverted then Figure 1 can be used for the level translation, otherwise Figure 2 will perform the level translation but will not invert the MISO signal.

One word of caution, presently ISD Engineering has approved this solution. Applications has tested it, However, the absolute maximum rating for voltage applied to any pin presently indicates $V_{\rm CC}+0.3$, and this brief is violating that specification. The procedure to relax that specification is presently in process with ISD Product Engineering and QC departments. Until the complete sign off by these departments, and the authorized relaxation of this specification, the use of the interface described within this brief will remain the responsibility of the end-applications design engineer.

ISD 1

Figure 1: Inverted MISO

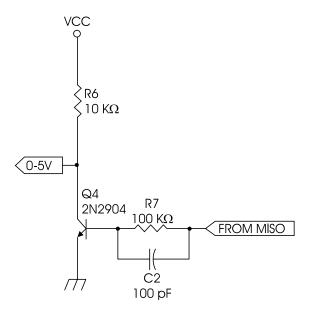
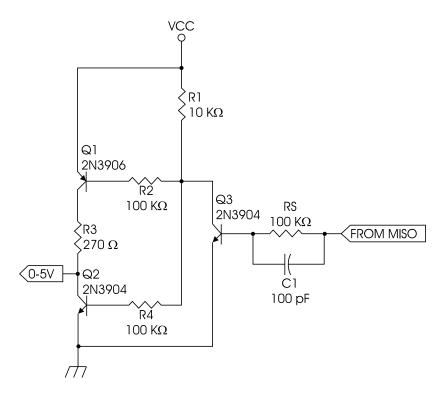


Figure 2: Non-Inverted MISO



The pseudo schematic outlined below demonstrates a typical interface between the ISD33000 powered at 3 volts and the microcontroller powered at 5 volts.

2 Voice Solutions in Silicon™

.C8 .0.1 μ F 15 14 14 DO U3 LT1121CZ-3.3 GND ATICAP ISD33000 ANA IN. VSSA VSSA VSSA VSSA \geq MISO MOSI SCLK SS RAC 26 1000 F R2 100 KΩ Q2 2N3904 C2 HF 4.7 <u>8</u>888 E **COP 820** U1 LM78M05 GND GND 23 C1 £

Figure 3: Typical Interface

ISD 3