Thermal considerations for FAST logic products

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INTRODUCTION

Thermal considerations by both supplier and user require more attention as package sizes shrink and operating frequencies increase. This is because an increase in junction temperature (T_j) can adversely affect the long term operating life of an IC. Some of the variables that affect T_j are controlled by the IC manufacturer while others are controlled by the system designer.

With increasingly frequent use of Surface Mount Device (SMD) technology, management of thermal characteristics becomes a growing concern. Not only are the SMD packages much smaller, but the thermal energy is concentrated more densely on the printed circuit board.

FAST PRODUCTS IN SSOP PACKAGE

The FAST product family is a high performance Bipolar Logic Family. In the SMD packages, such as SSOP, it is necessary to estimate operating junction temperatures of the FAST products in the system environment. The information provided herein should assist the system designer with thermal management considerations.

POWER DISSIPATION

The power dissipation equations, definition of terms and the assumptions made in estimating power dissipation are shown below.

The total power is the sum of the static power and dynamic power.

$$P_{total} = P_{static} + P_{dynamic.}$$

The equation for static power dissipation is,

$$P_{stat} = (V_{CC} \times I_{CC})$$

but since I_{CCH}, I_{CCL} and I_{CCZ} are different values, the equation becomes,

$$P_{stat} = V_{CC}[DC_{en}(N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1\text{-}DC_{en})I_{CCZ}]$$

where:
- DC_{en} = % duty cycle enabled
- N_H = number of outputs in high state
- N_L = number of outputs in low state
- N_T = total number of outputs.

The equation for the dynamic power dissipation is,

$$P_{dyn} = [DC_{en} \times N_{sw} \times V_{CC} \times f1 \times (V_{OH} - V_{OL}) \times C_L] + [DC_{en} \times N_{sw} \times V_{CC} \times f2 \times (ma/MH_Z/bit)] \times 10^{-3}$$

where:
- DC_{en} = % duty cycle enabled
- N_{sw} = total number of outputs switching
- f1 = operating frequency (in Hz)
- f2 = operating frequency (in MHz)
- C_L = external load capacitance (in F)
- mA/MHz/bit = slope of the I_{CC} vs frequency curve.

Thermal Resistance (Θ_{ja})

The ability of a package to conduct heat from the IC chip inside the package to the environment is expressed in terms of “thermal resistance”. It is measured in degrees Centigrade per watt of power dissipated by the chip. Table 1 lists some thermal resistance values for selected FAST products in SSOP packages. The values listed were measured in still air with no traces attached (worst case environment).

Table 1. FAST Products in SSOP Package

PRODUCT	PIN COUNT	Θ_{ja}	mA/MHz/bit (unloaded)
74F245	20	125	0.158
74F244	20	127	0.125
74F2244	20	127	0.045
74F373	20	125	0.158
74F374	20	125	0.102
74F543	24	118	0.512*
74F827	24	121	0.125
74F240	20	124	0.275
74F299	20	121	0.183
74F533	20	124	0.129
74F657	24	113	0.202

* The 74F543 I_{CC} vs Frequency slope increases above 20 MHz. From 20 MHz to 30 MHz, slope = 1.64. From 30 MHz to 40 MHz, slope = 2.55.

FACTORS AFFECTING Θ_{ja}

For a given package and lead frame, some factors which affect the thermal resistance (Θ_{ja}) in the application include (1) the die size of the IC chip, (2) the length of the printed circuit board traces attached to IC package on the system board and (3) the amount of airflow across the package.

Figure 1 through Figure 7 provide Θ_{ja} information for the 20 and 24 pin packages as a function of die size, airflow and trace length.

A SAMPLE CALCULATION

An example for the 74F244. Junction temperature is estimated from the equation:

$$T_j = (\Theta_{ja} \times P_{total}) + T_{amb}$$
$$P_{total} = P_{stat} + P_{dyn}$$

Assuming the number of outputs High = 4, V_{CC} at 5.25V, the enable duty cycle (DC_{en}) = 50%, and worst case I_{CC}'s (I_{CCL} = 90 mA, I_{CCH} = 60 mA, I_{CCZ} = 90 mA) the static power calculation is:

$$P_{stat} = (5.25)\{(0.50)[(4)(0.060)/8 + (4)(0.090)/8] + (1–0.50)(0.090)\}$$
$$= (5.25)[(0.0150) + (0.0225) + (0.045)]$$
$$= 0.433 \text{ watts}$$

Assuming the following,

DC_{en}	= 50%	N_{SW}	= 4
f1	= 25×10^6 Hz	V_{CC}	= 5.25V
f2	= 25 MHz	ma/MHz/bit	= 0.26
C_L	= 50 pf (50×10^{-12}F)	V_{OH}	= 3.4V
		V_{OL}	= 0.4V

the P_{dyn} becomes:

$$P_{dyn} = [(50\%)(4)(5.25)(25\text{x}10^6)(3.4–0.4)(50\text{x}10^{-12})] + [(50\%)(4)(5.25)(25)(0.26)](10^{-3})$$
$$= (0.0394) + (0.0682)$$
$$= 0.108 \text{ watts}$$

$$P_{total} = 0.433 + 0.108 = 0.541 \text{ watts}$$

The junction temperature estimation then becomes:

$$T_j = (127)(0.541) + T_{amb}$$
$$= 69 + T_{amb}$$

If the system ambient temperature is 55°C, then

$$T_j = 69 + 55 = 124 \text{ °C}.$$

With the junction temperature of a device established for a given system environment the expected operating life of the IC can be determined from the graph in Figure 6.

SYSTEM CONSIDERATIONS

The manner in which an IC package is mounted and positioned in its surrounding environment will have significant effects on operating junction temperatures. These conditions are under the control of the system designer and are worthy of serious consideration in the PC board layout and system ventilation and airflow features.

Forced-air cooling will significantly reduce thermal resistance.

Package mounting can affect thermal resistance. Surface mount packages dissipate significant amounts of heat through the leads that attach to the traces. Trace length is another significant factor.

Thermally conductive adhesive under the surface mount packages can lower thermal resistance by providing a direct heat path from the package to the board.

SSOP20 Θ_{ja} vs Die Size

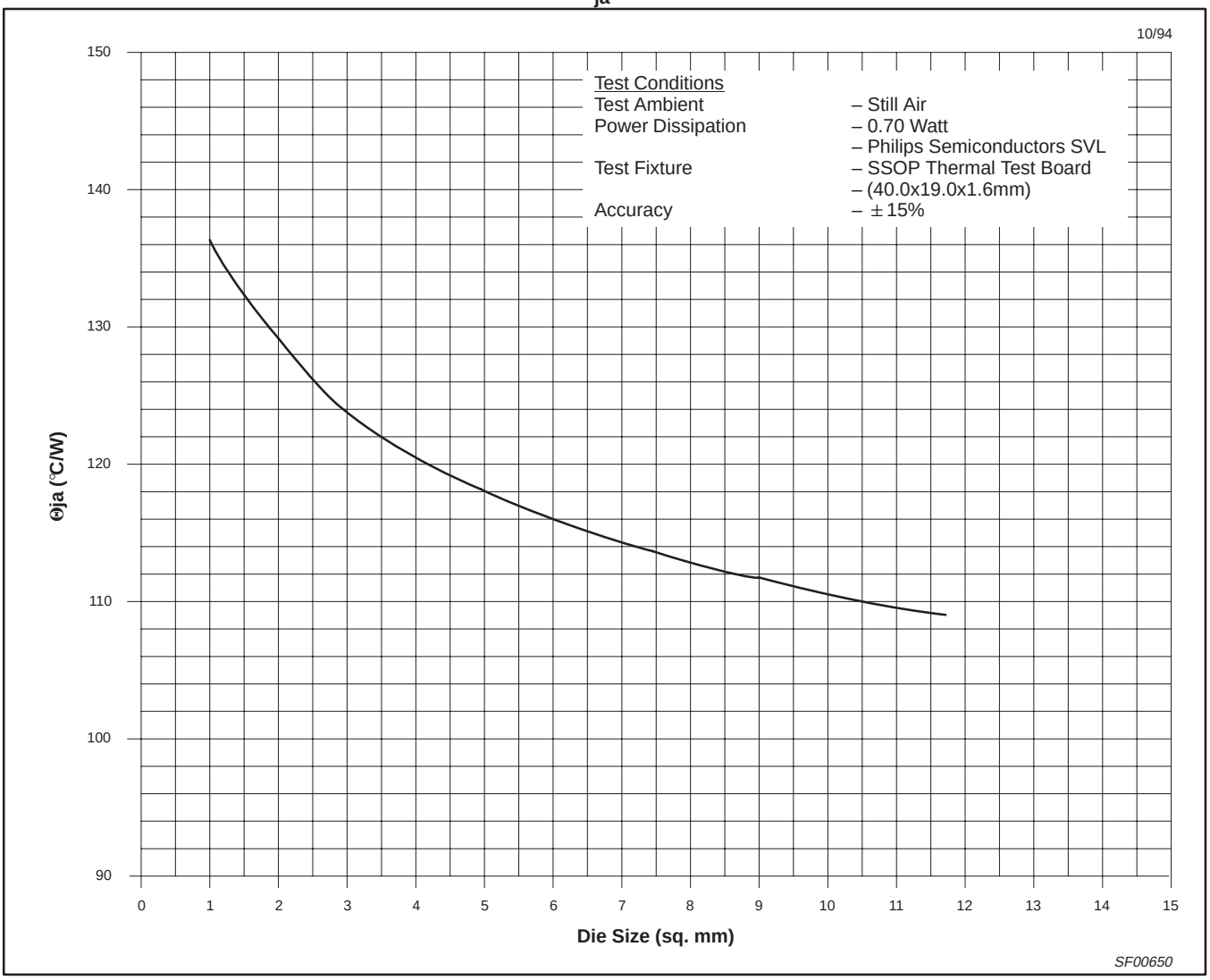

Figure 1.

SSOP20 Θja vs Airflow

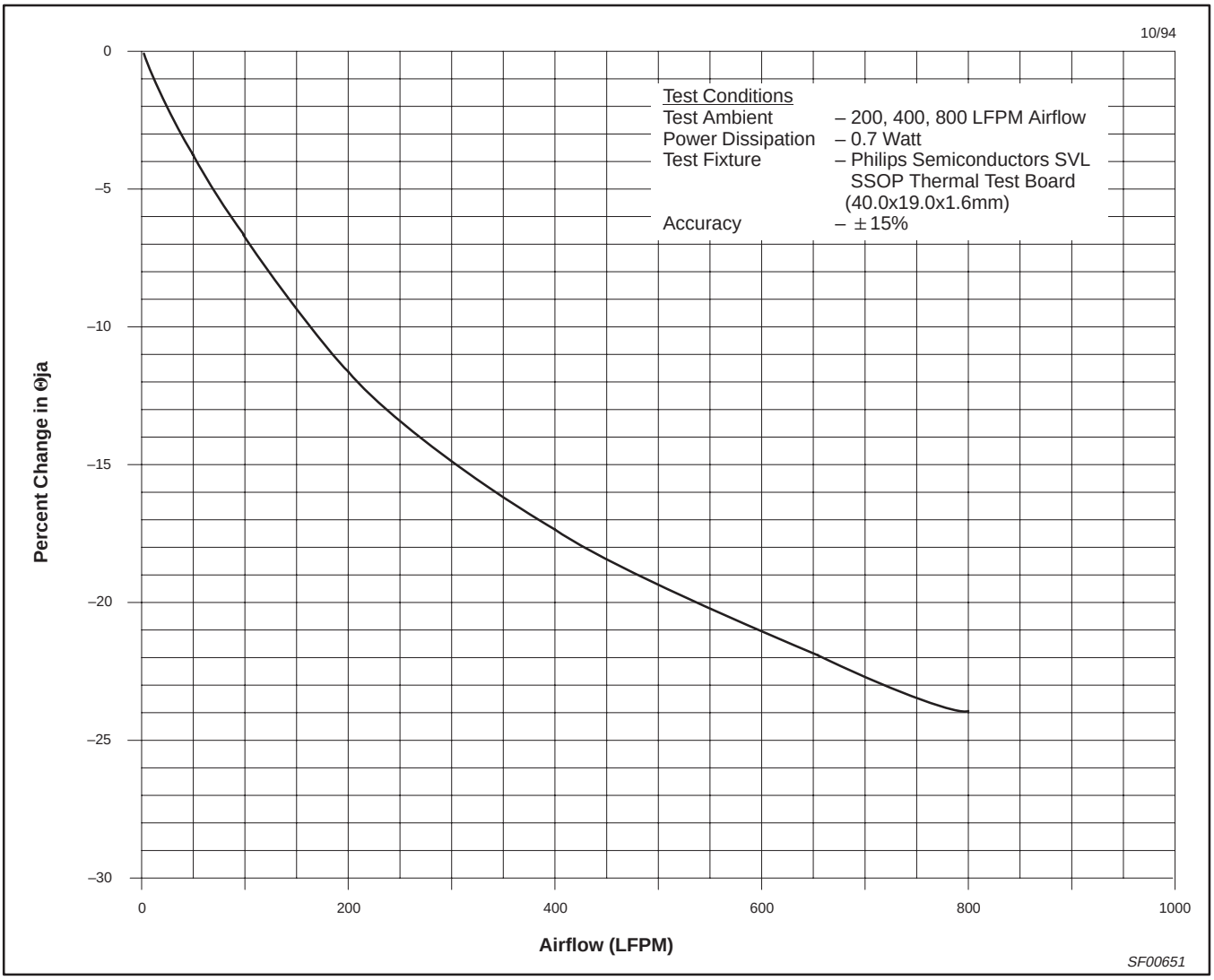

Figure 2.

SSOP24 Θja vs Die Size

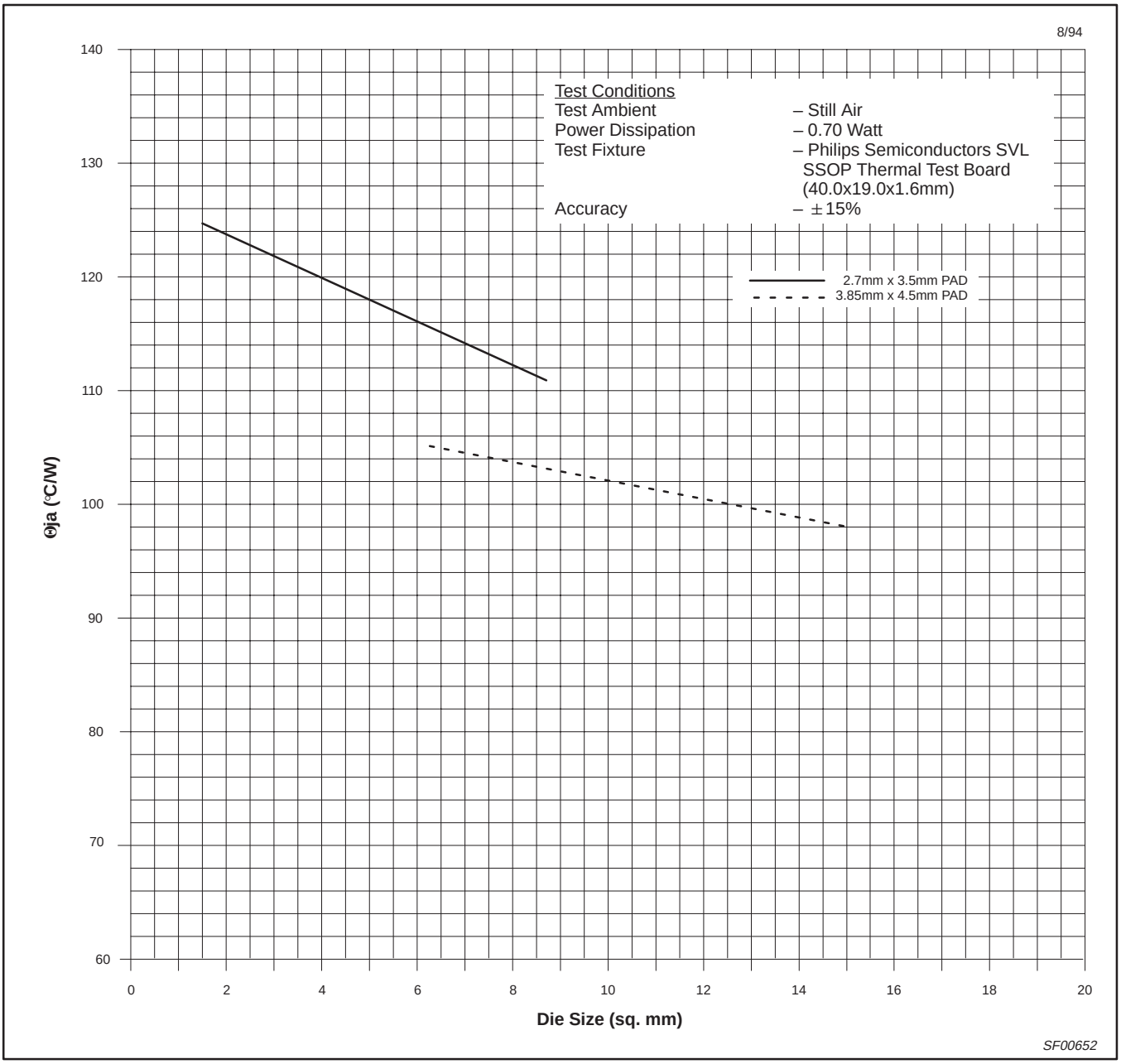

Figure 3.

SSOP24 Θja vs Airflow

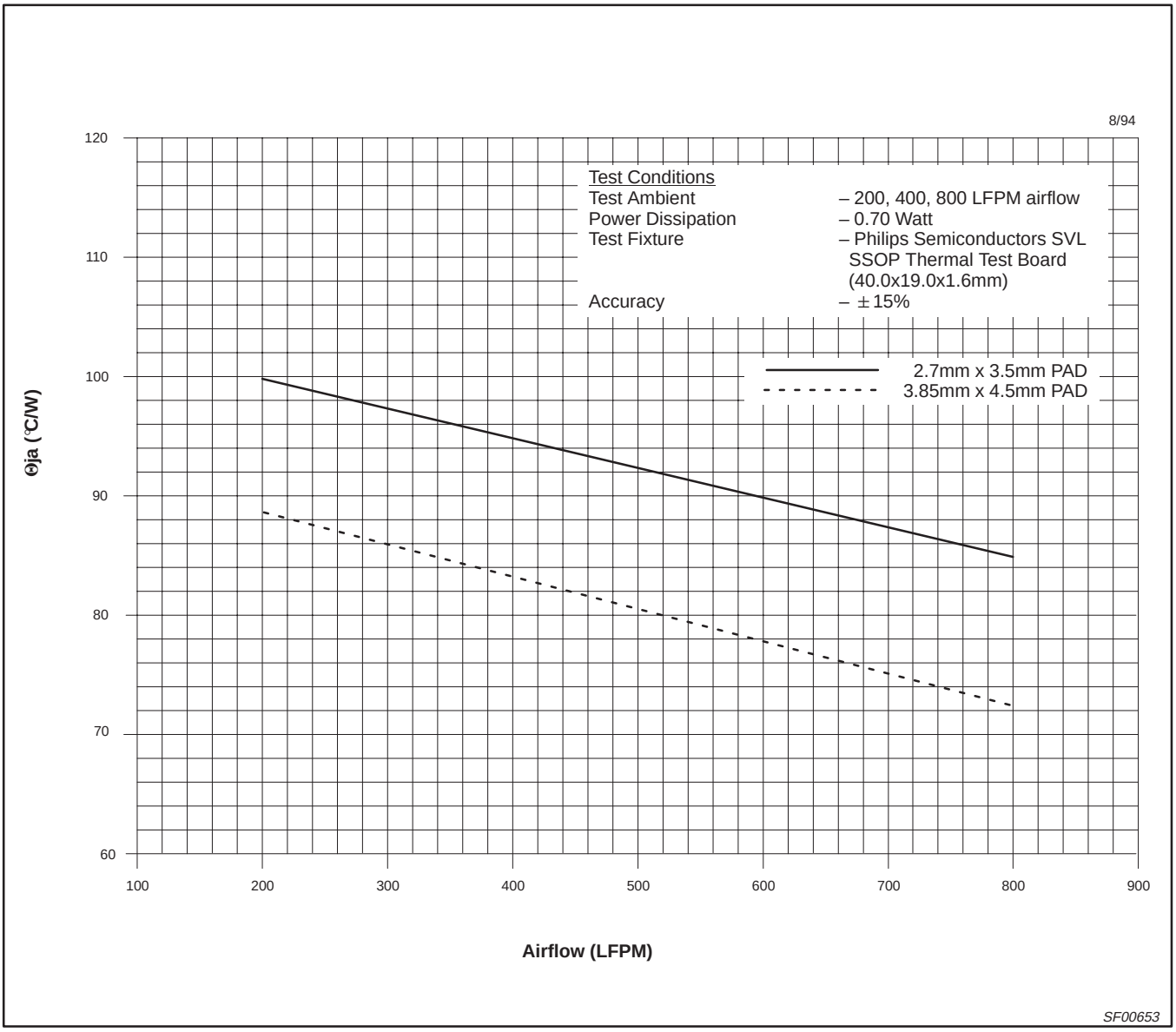

Figure 4.

Effect of Trace Length on Θja

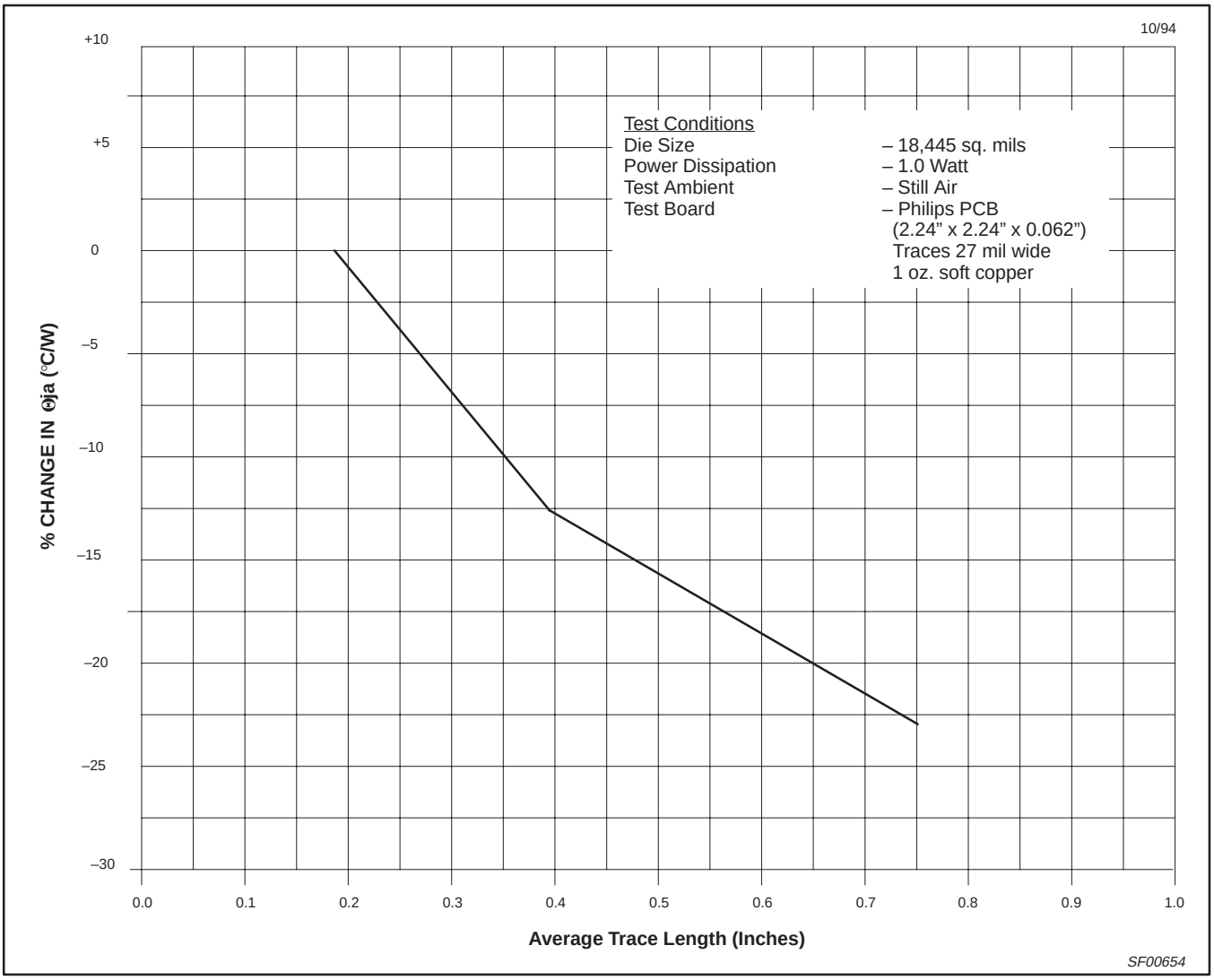

Figure 5.

FAST IN SSOP – ESTIMATED ONSET TO FAILURE (0.1% CUMULATIVE)

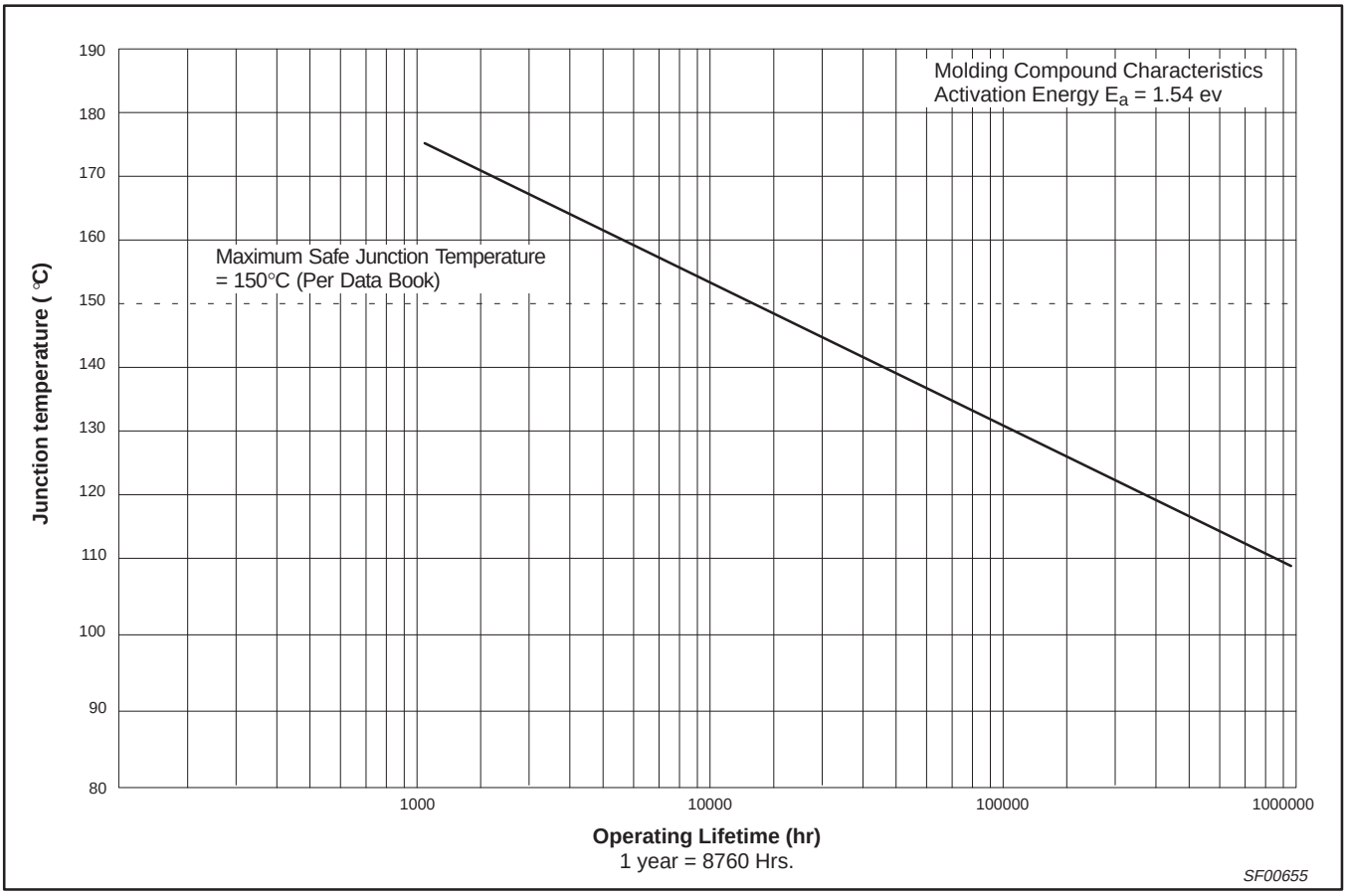

Figure 6.