

## Introduction

The development of LSI A/D converters has carved the pathway for a new category of low cost, accurate digital panel meters (DPM) and digital multimeters (DMM). The ICL7103A and ICL8052A A/D pair represents an excellent example of this new breed of converter products available today. The outstanding attributes of this pair include:

- Accuracy guaranteed to  $\pm 1$  count over the entire conversion range.
- Guaranteed zero reading for 0V input.
- Single reference voltage.
- Over-range and under-range signals available for auto-ranging.
- TTL compatible outputs.
- Six auxiliary outputs for enhanced interfacing capability.

In effect, the user has available a near perfect system. The key to a successful design depends, almost exclusively, on the individual's ability to prevent adding errors to the system.

The purpose of this application note is to describe the operation and potential pitfalls of a  $10\mu\text{V}$  resolution ( $V_{\text{REF}} = 100\text{mV}$ ) 4 1/2 digit autoranging scheme using the ICL7103A/ICL8052A pair. Two auto-ranging circuits are included within the text. Each is discussed in terms of its advantages and disadvantages. The following section, Basic Circuitry is intended to familiarize the reader with the circuitry common to both designs.

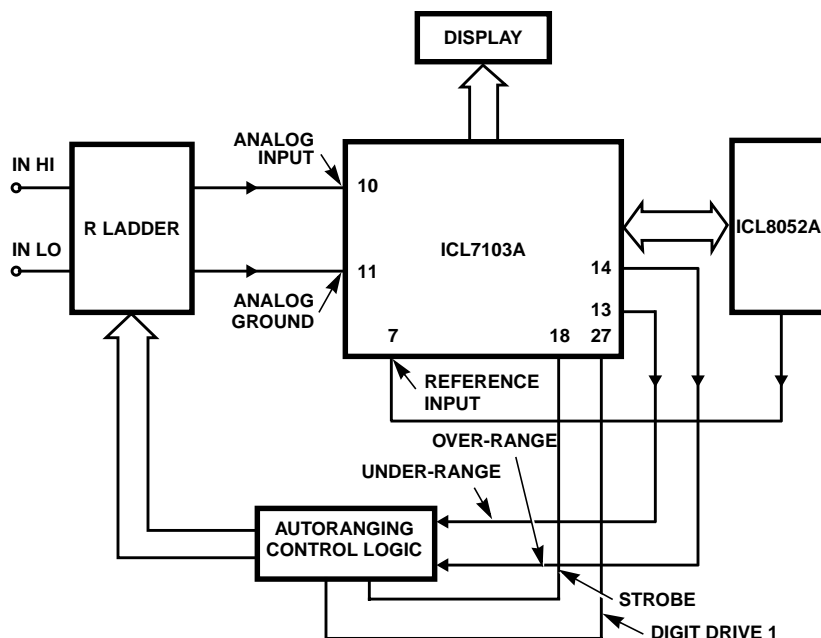


FIGURE 1. FUNCTION DIAGRAM

## Basic Circuitry

The basic circuit for the ICL7103A/ICL8052A A/D converter remains unchanged. However, a few modifications are necessary to accommodate a 100mV reference. First, the reference voltage divider network (5.1k, 1k) is modified for greater resolution. Second, the integrator resistor is reduced to 10k $\Omega$  to facilitate an approximate 8V integrator swing with  $V_{IN} = 200\text{mV}$ . Third, a 300k potentiometer should replace the 300k $\Omega$  fixed resistor in the comparator translation network. With  $V_{IN} = 0\text{V}$ , this pot should be adjusted until the display reads equal intervals of positive and negative signs. This network brings the comparator output up to the threshold of the ICL7103A logic during auto-zero. The two JFETs connected across the integrator cap maintain the integrity of the integrator and autozero cap during a gross over-range condition.

## Input Divider

Many auto-ranging systems use a resistive divider network of some kind. The particular type of network used is important and requires some thought. Shown in Figure 2 are two conventional divider networks.

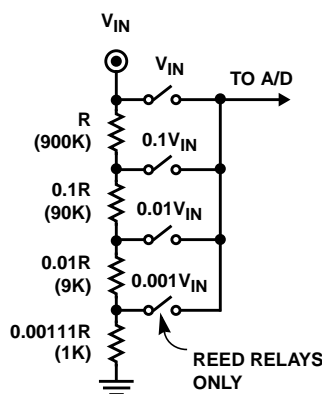


FIGURE 2A. TYPE A

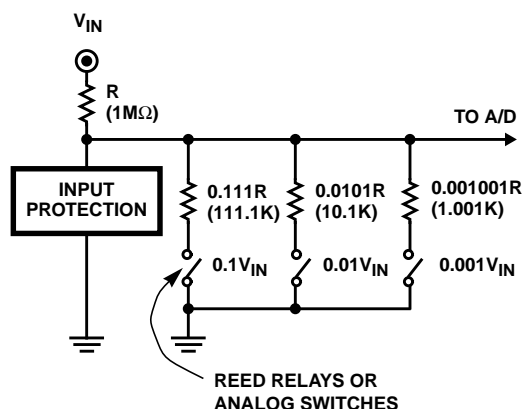


FIGURE 2B. TYPE B

Each of these dividers has advantages and disadvantages. For example, type B can be implemented with analog gating, whereas, type A cannot. However, type B requires some form of input protection to prevent destructive breakdown when high voltage is applied.

The designer must also consider the potential hazards of four additional sources of leakage current (3 switches plus input protection). For 10 $\mu\text{V}$  resolution, these leakage currents must be less than 10pA for the resistor values shown above.

A major advantage to type A is its versatility. It can easily be used to measure current and resistance as well as voltage. Type A was chosen for this application primarily for this reason. The absence of potential leakage current problems was also an important factor in favor of type A.

## Ohm's Converter (See Main Schematics)

Measuring an unknown resistance relies on the basic fundamentals of ohm's law. The ohm's converter produces a constant voltage (adjustable) which is applied to the ladder network. A constant current is generated and the voltage developed across the resistor in question is measured. Four decades of resistance can be measured by connecting the ohm's converter to the four points on the resistor ladder. The op amp used should be a FET input device to eliminate constant current source errors.

## AC Converter

With the addition of a precision rectifier and a low pass filter, AC measurements can be made. The precision rectifier shown in Figure 3 is a conventional circuit used for this application. Tolerances can be reduced below  $\pm 1\%$  by adjusting a single potentiometer. The user can expect dependable accuracy over a frequency range of 40Hz to 40kHz.

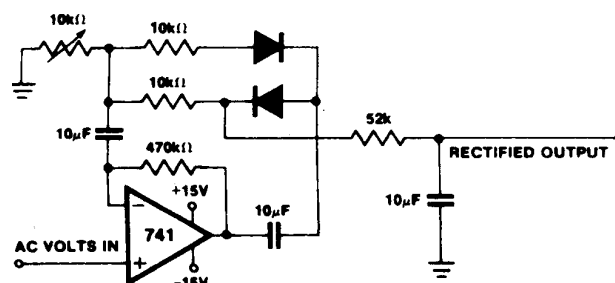


FIGURE 3. PRECISION RECTIFIER AND LOW PASS FILTER

## Clock Circuit

The actual clock frequency is not of first order importance, assuming it does not vary during a conversion cycle and is within the limits dictated by the integrating resistor and capacitor. However, some problems can result if the clock waveform contains severe ringing or spikes. The 311 clock generator shown in each schematic proved to be excellent

for this application. It did not generate current spikes on the 5V supply line and it remained stable during supply fluctuations due to variations in LED current.

### Decimal Point Logic

The anode of each decimal point used, (DP5, DP4, DP3) is connected to the common anode pin of its respective 7 segment display. The position of the zero bit in the shift register and the operating mode (kΩ or Volts) of the auto-ranging system determines which decimal point will be on.



FIGURE 4. PRECISION RECTIFIER AND LOW PASS FILTER

The table below defines when each decimal point should be on.

OPERATING MODE	D.P.5	D.P.4	D.P.3
DCV, ACV	2V Scale (B)	20V Scale (C)	200mV Scale (A) 200V Scale (D)
kΩ	2kΩ (D) 2MΩ (A)	20kΩ (C)	200kΩ (B)

NOTE: The letter in parenthesis indicates the location of the zero bit in the shift register.

The two rotary switches (SW1, SW2) and the two transistors (Q1, Q2) provide the necessary switching. The only addition to this circuitry is a single LED and a 180Ω resistor. Connect the anode to 5V and the cathode (through 180Ω resistor) to register A, and the LED will differentiate between the 200mV and 200V scales or the 2kΩ and 2MΩ scales.

### SN74195 Shift Register

The 74195 shift left/shift right shift register is the heart of the auto-ranging logic. The location of a single zero bit determines which relay is closed and which decimal point is on. Auto-ranging is accomplished by shifting the active bit either left or right until a non-over-range (or under-range) condition exists. The digital section associated with the 74195 varies between the two designs and will be discussed later.

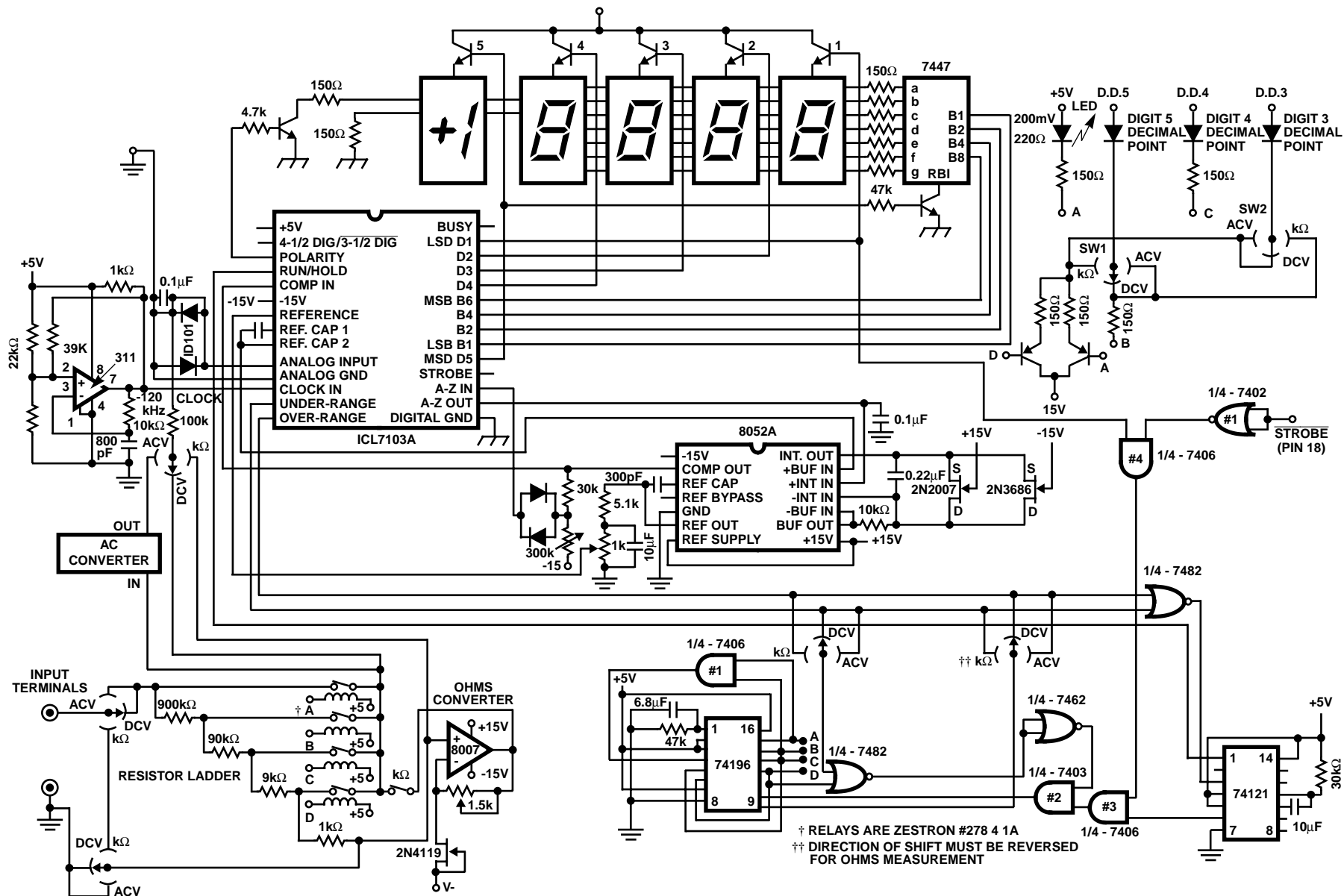


FIGURE 5. AUTO-RANGING SCHEMATIC #1

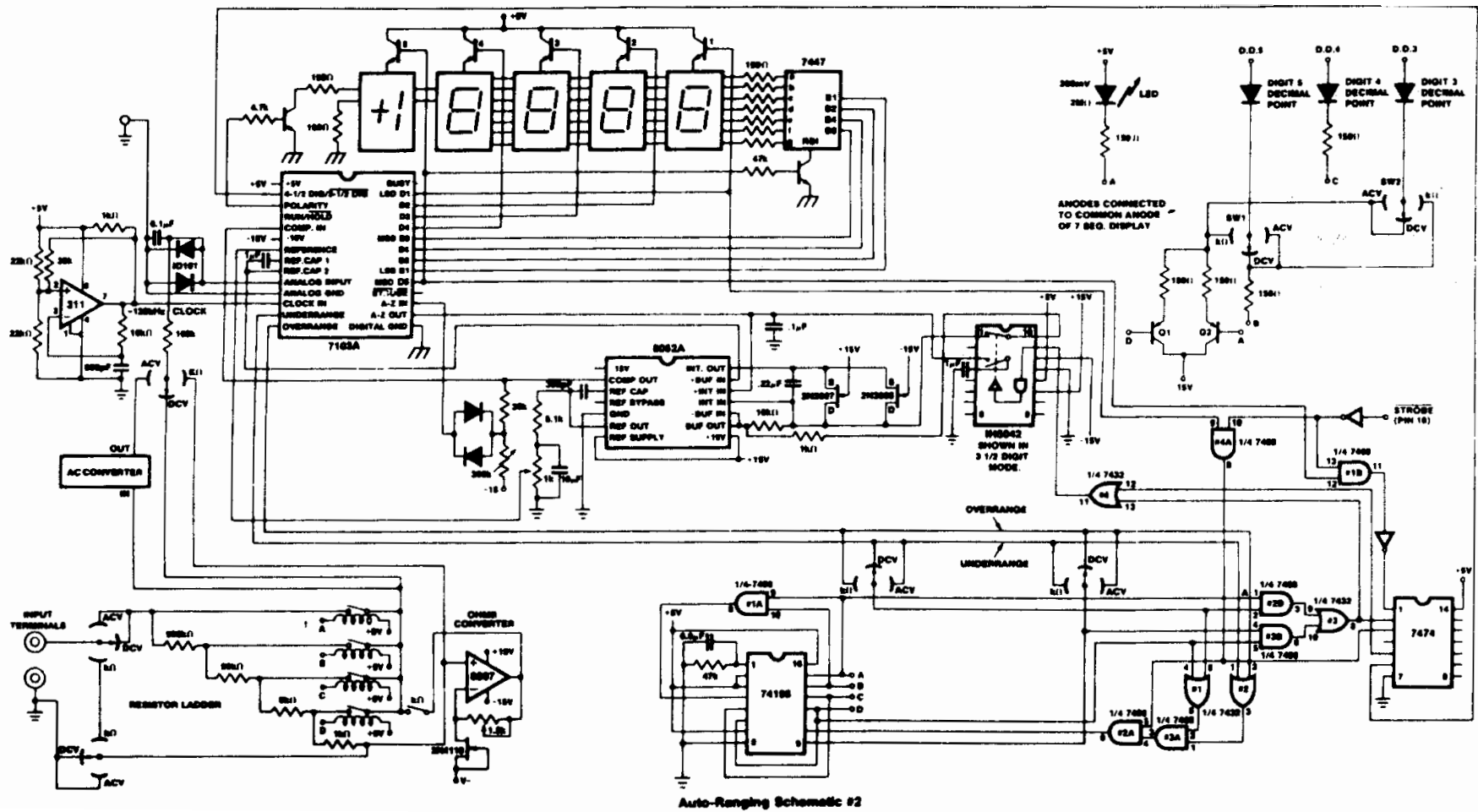


FIGURE 6. AUTO-RANGING SCHEMATIC #2

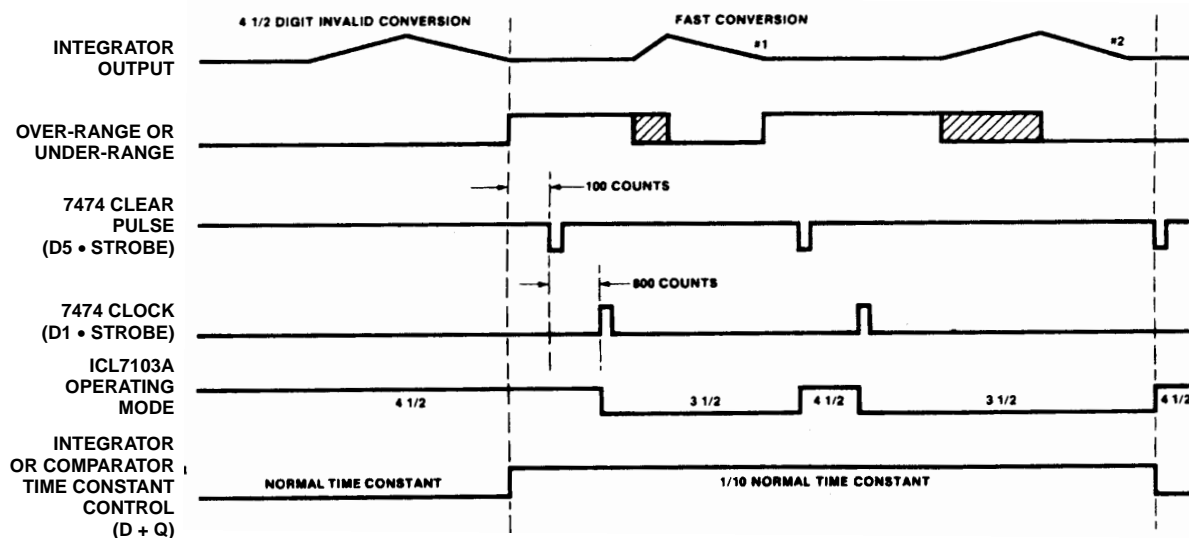


FIGURE 7. TIMING DIAGRAM FOR CIRCUIT #2

## Design Characteristics

This section is intended to familiarize the reader with individual characteristics of each design.

### Auto-Ranging

The basic idea behind Circuit #1 (Figure 5) is to extend the auto-zero time whenever an over-range or under-range condition exists. If the auto-zero time is not long enough, it is possible for the auto-ranging circuitry to continuously rock between two adjacent scales. Basically, this phenomenon is due to a residual deintegrate charge stored on the auto-zero cap after an over-range condition has occurred. The scale will increment up one decade but an under-range may result on the next conversion ( $V_{IN\ NET} = V_{IN\ ACTUAL} - V_{RESIDUAL}$ ). The 74121 extends auto-zero to 250ms whenever an under-range or over-range occurs. This time extension should enable the auto-zero loop to behave properly.

When an under-range or over-range occurs, several things happen. First, the true output of the 74121 goes high, enabling a shift pulse. At the same time the  $\bar{Q}$  output goes low, causing the ICL7103A to hold in auto-zero. Nine hundred clock pulses after the beginning of auto-zero, the coincidence between D1 and strobe generates the clock pulse that shifts the active bit in the register. Approximately 250ms after the beginning of auto-zero, the single shot will clear and another integrate/deintegrate cycle begins. The process will repeat on subsequent under-range/over-range conversions. One auto-range cycle requires approximately 450ms (200ms of integrate/deintegrate and 250ms of auto-zero).

Circuit #2 (Figure 6) utilizes the 3 1/2 - 4 1/2 digit mode of the ICL7103A to auto-range in approximately one-tenth the normal conversion time. The system is designed to operate in a normal 4 1/2 digit mode until auto-ranging is necessary.

The 7474 D flip-flop controls the 3 1/2 - 4 1/2 digit mode of the ICL7103A, but it has a rather interesting twist to insure sufficient auto-zero time.

The integrator and comparator time constants are each reduced by a factor of 10 at the beginning of auto-zero if auto-ranging is required. However, the ICL7103A doesn't enter the 3 1/2 digit mode until the input data to the 7474 is clocked into the register. This occurs 900 counts after auto-zero begins ( $D_1 \text{ strobe}$ ). The system completes the remainder of auto-zero and the subsequent conversion in the 3 1/2 digit mode at 10 times the normal conversion rate (approximately 33ms). The 7474 is then cleared 100 counts after the next auto-zero begins ( $D_5 \text{ • strobe}$ ) and a 4 1/2 digit mode is resumed. If subsequent auto-scaling is not necessary, the system continues to operate in the 4 1/2 digit mode and, if it is necessary, the integrator and comparator time constraints remain in a 3 1/2 digit mode but the ICL7103A returns to a 4 1/2 digit mode when the 7474 is cleared. Eight hundred counts later the data is strobed into the register and the ICL7103A once again enters the 3 1/2 digit mode and another 3 1/2 digit conversion cycle begins. The integrator and comparator will remain in the 3 1/2 digit mode and the ICL7103A will switch to the 4 1/2 digit mode for only 800 counts of auto-zero (900 counts for the first auto-zero after over-range or under-range) extends the effective auto-zero time to 1720 counts instead of 1000 (1810 for the first auto-zero after over-range or under-range). The faster time constants of the integrator and comparator, in addition to the extended auto-zero, ensures proper operation of the auto-zero loop and eliminates the possibility of oscillating between adjacent ranges.

	OPERATING MODE	CONTENTS OF DECADE COUNTERS					COMMENTS
		MOST SIGNIFICANT DECADE	DECADE 4	DECADE 3	DECADE 2	LEAST SIGNIFICANT DECADE	
1st AZ After Invalid Conversion	4 1/2 Digit	0	0	9	0	0	900 counts after auto-zero begins, data is strobed into 7474
	3 1/2	0	9	1	0	X	Total clock periods needed to fill counters with 1,000 equals 1810
Int. Deint.	3 1/2	1	0	0	0	X	Next integrate cycle
	3 1/2	2	0	0	0	X	Max counts for deintegrate
Subsequent Auto-Zero's	3 1/2	0	1	0	0	X	7474 cleared
	4 1/2	0	0	8	0	0	Total counts of 4 1/2 digit auto-zero
	3 1/2	0	8	2	0	X	Remaining auto-zero counts

## NOTES:

1. Counts required for first auto-zero = 1810 ( $\approx 15\text{ms}$ )
2. Counts required for next conversion = 3000 max ( $\approx 25\text{ms}$ )
3. Counts required for second, third or fourth auto-zero = 1720 ( $\approx 14.3\text{ms}$ )
4. Total time required to auto-range through four decades  $\approx 300\text{ms}$  (170ms are required for the initial integrate/deintegrate cycle).

The status of the ICL7103A/ICL8052A is determined by 5 decade counters in the ICL7103A. The least significant counter is cleared and bypassed in the 3 1/2 digit mode. A closer look at these counters, with respect to the auto-ranging circuitry, will clearly show the time available for auto-zero and individual conversion periods.

The shift pulse to the 74195 is enabled by AND gate #2A. If an over-range or under-range occurs and register D contains a logic 1, the shift clock is enabled; if D is a logic 0 and a shift right condition exists, the clock is disabled. AND gate #1A insures the active bit will not shift out of the register when  $V_{IN} \leq 18.00\text{mV}$ .

The 3 1/2 digit mode is disabled when register A is a logic 0 and a shift left occurs, or if register D is a logic 0 and a shift right occurs. Basically, this means the ICL7103A/ICL8052A will convert small inputs ( $V_{IN} \leq 18.00\text{mV}$ ) and signals greater than 200V in a 4 1/2 digit mode. This is accomplished with AND gates #2B and #3B and OR gate #3.

The integrator and comparator time constants are controlled by OR gate #4. Short time constants are enabled as soon as an over-range or under-range occurs and they remain enabled until a non-over-range/under-range condition exists and the 7474 is cleared.

## Caution

Using the ICL7103A/ICL8052A solves a great number of conventional A/D design problems; however the user must pay special attention to the components and the board layout for the specific application. Following are some application notes. If the user spends some time reviewing these, fewer problems will result.

## Symptoms/Solutions

It is very easy to build a system containing several error terms, and if the user is unfamiliar with integrating A/D converters, a specific troubleshooting sequence may not be apparent. This section is intended to identify specific errors and suggest solutions.

- With  $V_{IN} = 0\text{V}$ , the display flashes zeros indication an over-range.
  - Check power supplies. If the  $\pm 15\text{V}$  supply is not working properly the ICL7103A/8052A may over-range.
  - Check all component connections corresponding to the integrator, comparator, and analog switch network.
- With  $V_{IN} = 0\text{V}$ , display reads something other than zero (offset error)
  - This symptom is typically a result of grounding problems or digital signals coupled to analog lines. Connect pin 11 (analog ground) to the 100k $\Omega$  resistor at signal input. If the offset disappears, the problem is a result of IR drops in the ground line. Reconnect ground lines similar to Figure 8.

If the offset remains the same, check the proximity of digital lines (digit drive, busy, under-range) to analog lines. They should be separated as far as possible.

If the offset reduces but is not completely eliminated. The problem is most likely due to both types of errors.

- Unusually large rollover error.
  - Rollover is a result of the voltage drop on the auto-zero capacitor during the reference integrate phase, and stray capacitance present while charging  $C_{REF}$  to the reference voltage. For a 1V reference, the ICL7103A/8052A pair is guaranteed to have less than one count of rollover. With a 100mV reference, the rollover should be less than 2 counts. If larger rollover

errors are present, clean the PC board, as any leakage current path must be removed. Also be sure the auto-zero and reference capacitors are high quality, low leakage capacitors.

- Unusually large amount of count instability.
  - Check noise on the power supplies. If large current spikes or 60 cycle noise are present, the converter will appear noisy. Also, if the comparator translation network (36k, 300k) is way out of the adjustment, the comparator will not respond consistently to a zero crossing.

### Generally Speaking

- Minimize stray capacitance
- Keep analog lines short
- Build system around a stable analog ground

### References

For Intersil documents available on the internet, see web site <http://www.intersil.com/>

Intersil AnswerFAX ( 321) 724-7800.

- [1] *A016 Application Note*, Intersil Corporation Communications Division, "Selecting A/D Converters," AnswerFAX Doc. No. 99016.
- [2] *A017 Application Note*, Intersil Corporation Communications Division, "The Integrating A/D Converters," AnswerFAX Doc. No. 99017.
- [3] *A018 Application Note*, Intersil Corporation Communications Division, "Do's and Don'ts of Applying A/D Converters," AnswerFAX Doc. No. 99018.
- [4] *A019 Application Note*, Intersil Corporation Communications Division, "4 1/2 Digit Panel Meter Demonstrator/Instrumentation Boards," AnswerFAX Doc. No. 99019.
- [5] *A023 Application Note*, Intersil Corporation Communications Division, "Low Cost Digital Panel Meter Designs," AnswerFAX Doc. No. 99023.

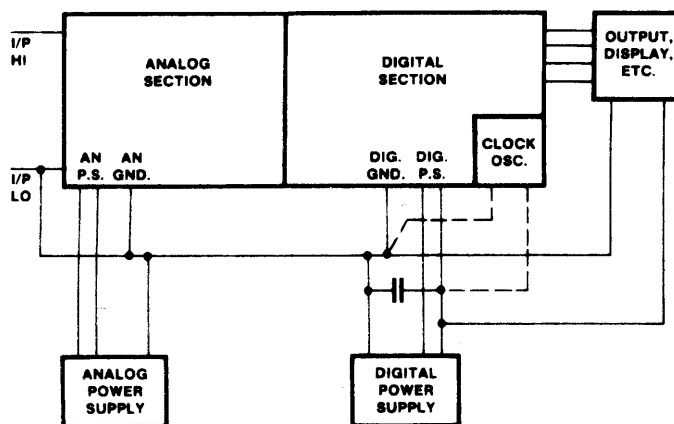


FIGURE 8.

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