AP-707

APPLICATION NOTE

3 Volt Intel® StrataFlash™ Memory CPU Interface Design Guide

July 1999

Order Number: 298105-001

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 80217-9808

or call 1-800-879-4683
or visit Intel's Website at http://www.intel.com

COPYRIGHT © INTEL CORPORATION 1999 CG-041493

*Third-party brands and names are the property of their respective owners.

StrongARM is a registered trademark of ARM, Ltd.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
07/02/99	-001	Original version

1.0. INTRODUCTION

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to various microprocessors including:

- ARM7TDMI
- StrongARM® SA-110, SA-1100 and SA-1110
- PowerPC* MPC603e (PPC603e)
- Intel® i960® HA/HD/HT
- Hitachi 7708 (SH-3)
- Hitachi 7750 (SH-4)
- Philips MIPS-based PR31700 Poseidon processor
- Motorola MC68060

These interfaces were written for the specific processors mentioned, but could be modified to meet any other processor in that family.

This application note was written with preliminary information about 3 Volt Intel StrataFlash memory, and preliminary information about some of the processors. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0. HARDWARE INTERFACE

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more

information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

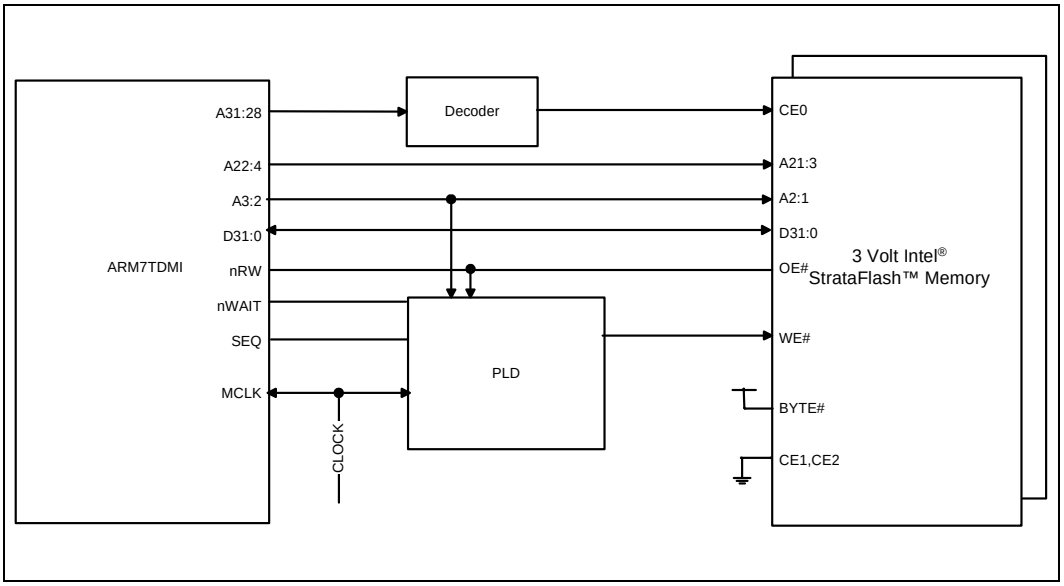


Figure 1. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI Interface

3.0. INTERFACING 3 Volt Intel® StrataFlash™ Memory

These sections contain the interfaces between the 3 Volt Intel StrataFlash memory and the processors included in this document.

3.1. Interfacing 3 Volt Intel® StrataFlash™ Memory to ARM7TDMI at 33 MHz

The ARM7TDMI microprocessor by Advanced RISC Machines, Ltd. uses both a 32-bit ARM instruction set and a 16-bit THUMB instruction set. This allows for 16-bit instructions on a 32-bit architecture. This interface uses two 3 Volt Intel StrataFlash components to match the 32-bit data bus on the ARM7TDMI. Figure 1 is a block diagram of the interface between the 3 Volt Intel StrataFlash memory and ARM7TDMI.

3.1.1. INTERFACE CONSIDERATIONS

In addition to the two 3 Volt Intel StrataFlash memory components, this interface uses address decoding to generate a chip enable signal and a PLD to aid in generating other signals. The additional hardware may be integrated into an ASIC. All components can operate with a power supply between 2.7 V and 3.6 V. RCR.16 should be set to enable page-mode before page-mode timings are used.

Device	Min	Max
Decoder	0 ns	14 ns
PLD	2 ns	12 ns

NOTE:
These delays are for timings as shown in diagrams in this section, not necessarily the only possibilities for an interface.

3.1.2. PROCESSOR INTERFACE SIGNALS

The following signals are provided by the ARM7TDMI.

$A_{31:0}$: The 32-bit address bus transmits addresses to memory from the processor.

$D_{31:0}$: The 32-bit data bus transfers data between the processor and memory.

MCLK: The Memory Clock signal times all memory requests.

nRW: The Not Read/Write indicates whether the current data transfer is a read or a write.

nWAIT: The Not Wait input indicates to the processor that a bus stall is needed. nWAIT can only change when MCLK is low.

SEQ: The Sequential Address signal indicates if the next address will follow the previous one.

APE: Address Pipeline Enable is used to modify the timing of signals put on the bus. In this interface, it is always low.

3.1.3. CONTROL SIGNAL GENERATION

The address decoding generates the chip enable signal from the higher address lines. The PLD generates all other signals that are not directly connected. The 3 Volt Intel StrataFlash memory's OE# can be directly connected to the ARM7TDMI nRW. SEQ, nRW, and the lower address lines are used to generate nWAIT, which is the same as WE# for write operations. Figure 2 is a diagram of the PLD configuration.

For read operations, SEQ and $A_{3:2}$ are used to determine how many wait-states are necessary—the delay of an initial read or the shorter time necessary for a page-mode read. Wait-states for a page-mode read should be inserted when SEQ was asserted in the previous cycle and $A_{3:2}$ do not switch from 11 to 00. If either SEQ was not asserted in the previous cycle or $A_{3:2}$ switch from 11 to 00, wait-states for an initial read should be inserted. Figure 3 is a diagram of the wait-state logic.

Figure 4 is a timing diagram of four reads using page-mode accesses. nWAIT is used to delay the processor for several clock cycles on the initial access and for one clock cycle on subsequent accesses. Note that in Figure 4 it is assumed that the access is the first access in the memory region, so the ARM7TDMI inserts an extra wait-state without being signaled by nWAIT.

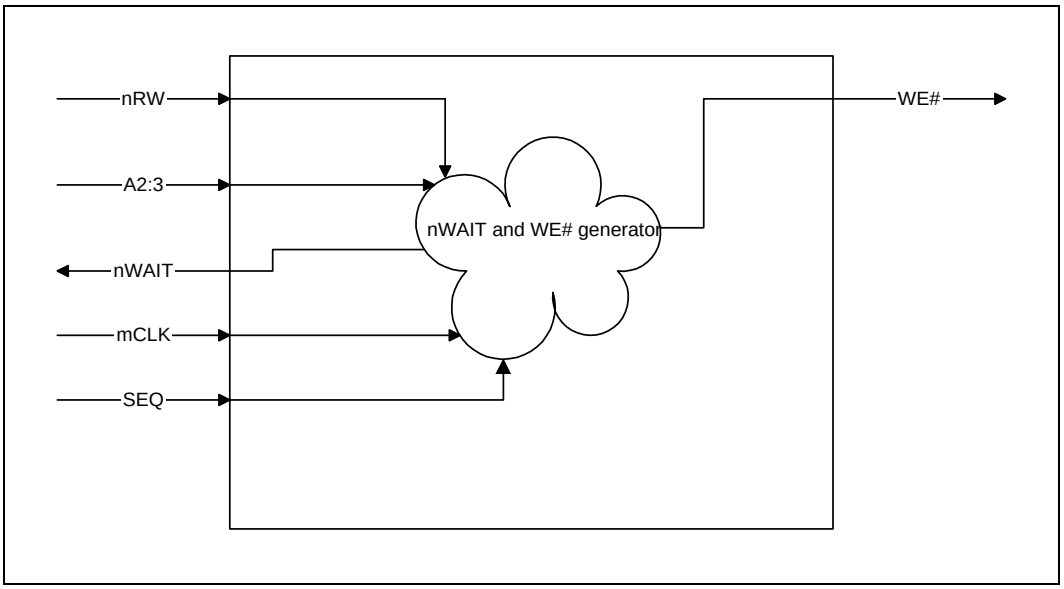
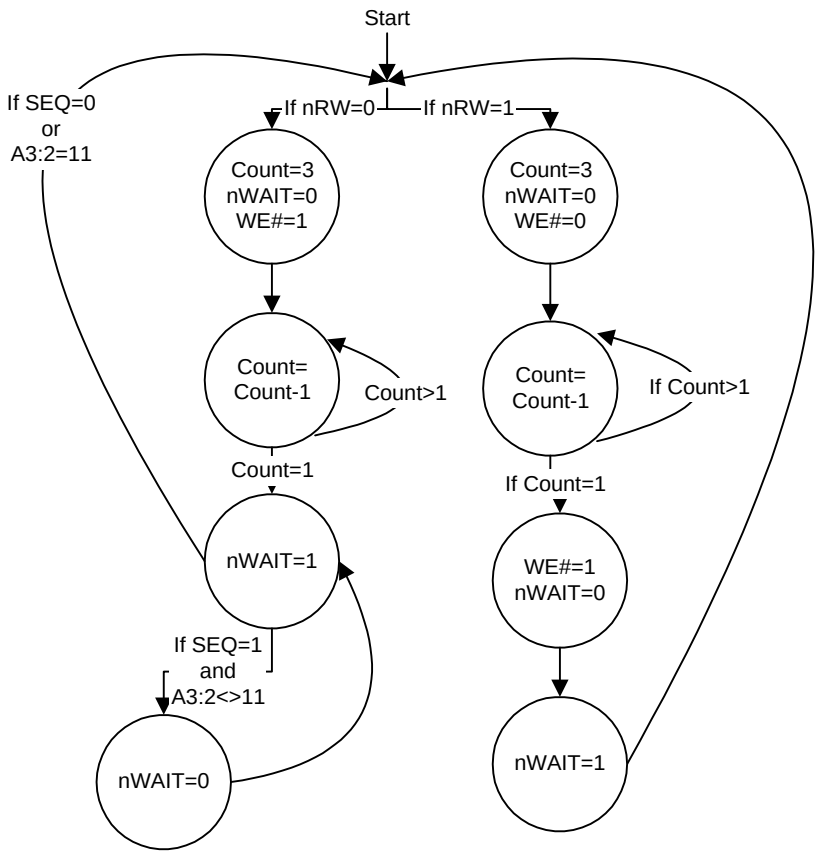


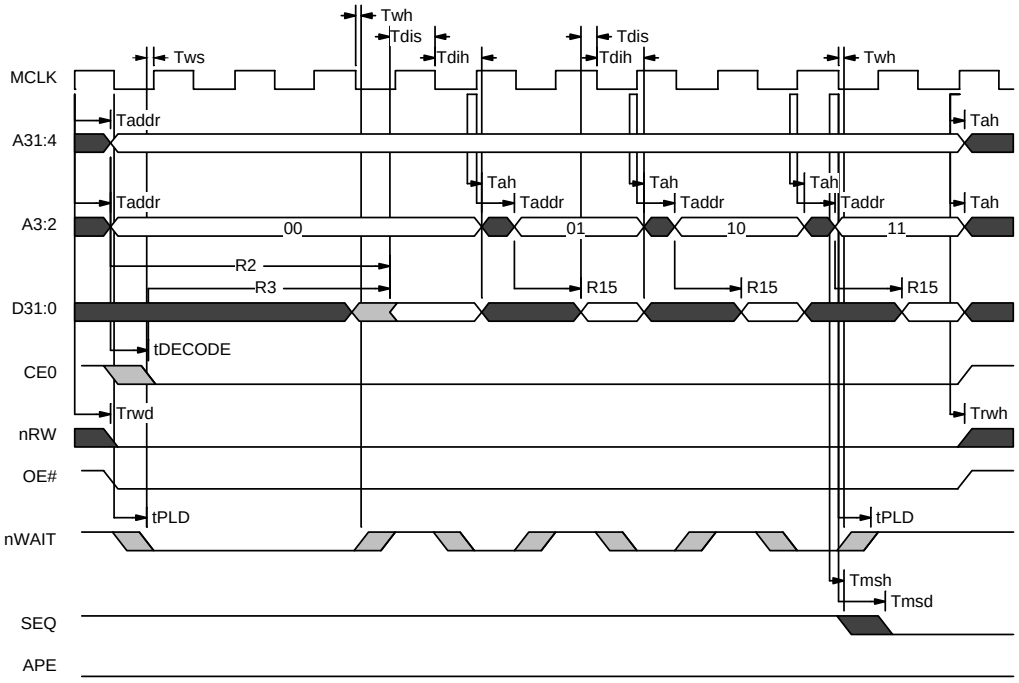
Figure 2. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI PLD Configuration



NOTE:

Diagram assumes page-mode is enabled. Initial wait-states are for 32-Mbit 3 Volt Intel® StrataFlash™ memory.

Figure 3. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI Wait-State Logic



NOTE:

The address line labels in this diagram refer to the labels on the ARM7TDMI. A$_x$ on the ARM7TDMI is A$_{x-1}$ on 3 Volt Intel® StrataFlash™ memory.

Figure 4. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI 4 Word Read at 33 MHz with Page-Mode Enabled

Figure 5 is a timing diagram of two writes followed by a read. WE# and nWAIT should go low at the same time, but WE# should go high one clock cycle before nWAIT. This allows for the WE# pulse high and write recovery before read specifications to be met.

Several considerations must be taken into account when resetting or powering down the system. When block erase, program, or lock-bit configuration is taking place and RP# is asserted low to the 3 Volt Intel StrataFlash memory, RP# must be held low for a time of t_{PLPH} (35 µs). The 3 Volt Intel StrataFlash memory also has a time of 310 ns (t_{PHQV} + t_{PHRH}) before output is valid after RP# goes high. This is longer than a normal initial page access, so if the ARM7TDMI makes its first access from the 3 Volt Intel StrataFlash memory, this must be taken into account. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

Consult the appropriate datasheets for specific information about the individual components in this interface (see Appendix A for a list of additional information).

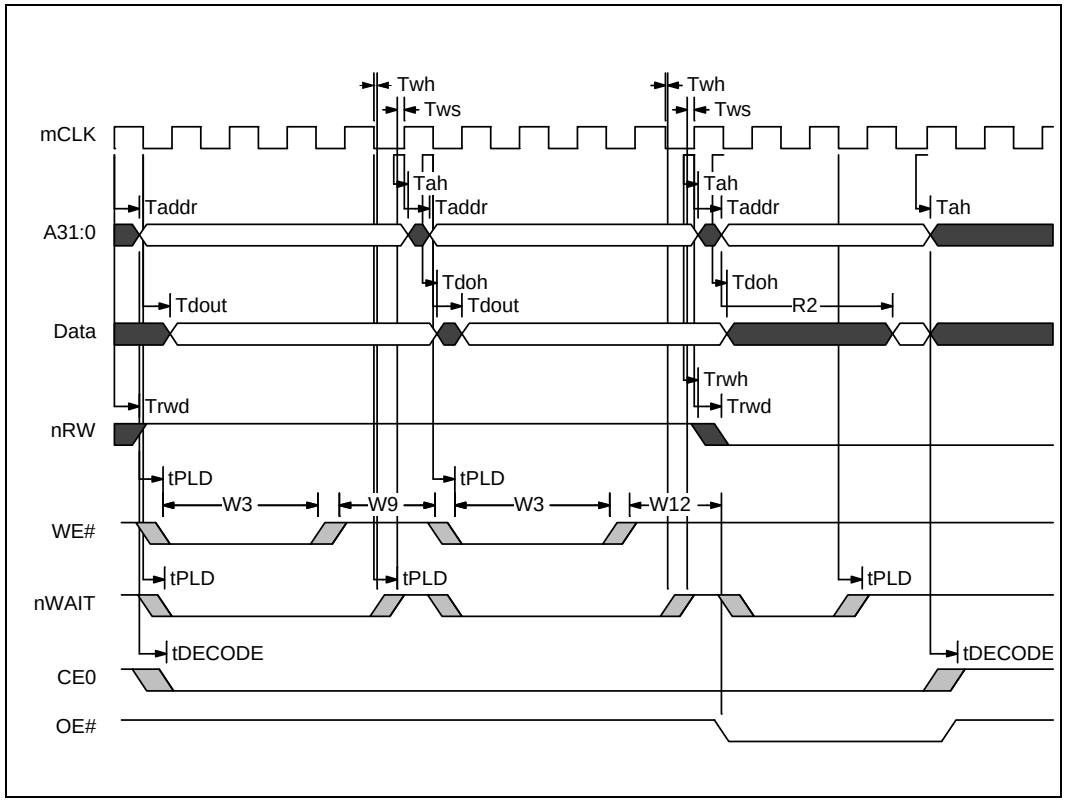


Figure 5. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI Write Cycles Followed by Read

3.2. Interfacing 3 Volt Intel® StrataFlash™ Memory to the StrongARM® SA-110 at 40 MHz

The StrongARM SA-110 microprocessor is capable of bus frequencies between 27 MHz and 66 MHz. This interface was written for a 40 MHz bus and a 32-Mbit 3 Volt Intel StrataFlash memory device, but could be modified to any of the other available processor frequencies or sizes of the 3 Volt Intel StrataFlash memory devices.

3.2.1. INTERFACE CONSIDERATIONS

The interface uses two 3 Volt Intel StrataFlash memory components to match the SA-110's 32-bit data bus width. A PLD and a decoder are used to generate necessary signals for this interface. All components can interface at 3.3 V. The SA-110 runs from a 1.65 V or 2.0 V power supply, and the 3 Volt Intel StrataFlash memory uses a 2.7 V to 3.6 V. Both can interface between 2.7 V and 3.6 V. Minimum and maximum delay specifications for the PLD and decoder are listed in the table below. These minimum and maximum times are those used in Figure 8 and Figure 9.

Device	Min	Max
Decoder	0 ns	9 ns
PLD	2 ns	9 ns

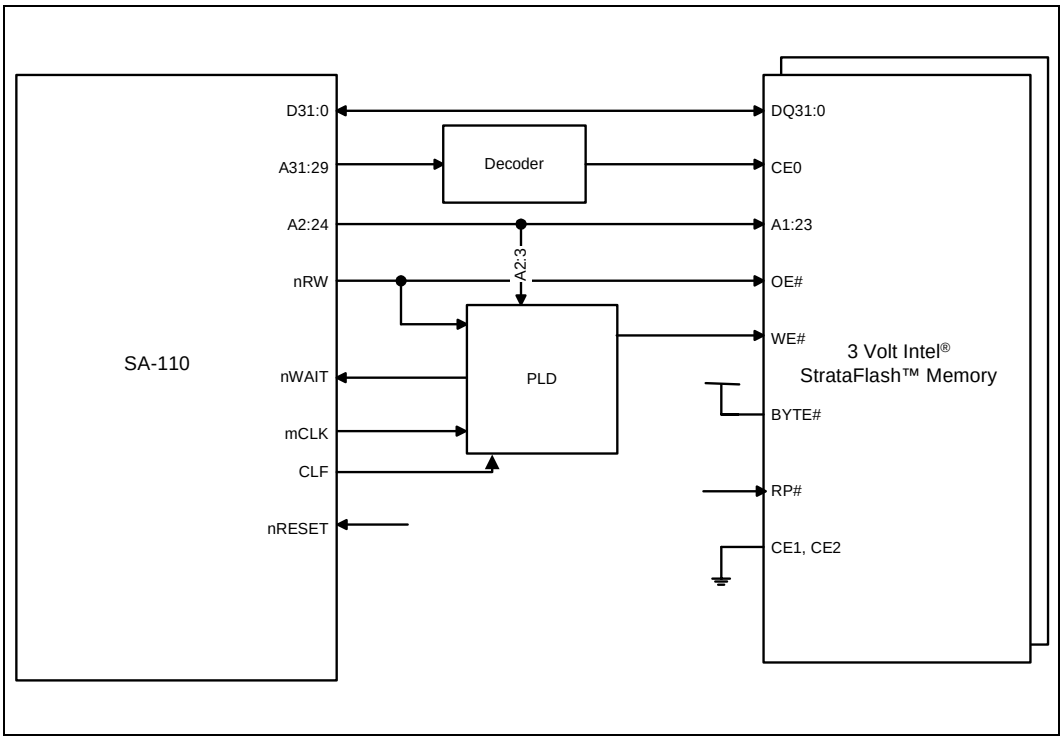


Figure 6. 3 Volt Intel® StrataFlash™ Memory/SA-110 Interface

3.2.2. PROCESSOR INTERFACE SIGNALS

The interface uses the following signals provided by the SA-110:

$A_{31–0}$: The 32-bit address bus transmits instruction and data addresses to memory. Because $A_{1:0}$ are for 16- or 8-bit operation, A_2 on the SA-110 will correspond to A_1 on the 3 Volt Intel StrataFlash memory.

$D_{31–0}$: The bi-directional data bus transfers data between the processor and memory.

nWAIT: The Not Wait pin signals for a bus stall lasting one clock cycle. nWAIT must be changed when MCLK is low.

nRW: The Not Read/Write pin indicates whether the current cycle is a read or a write.

MCLK: The memory clock governs all memory accesses.

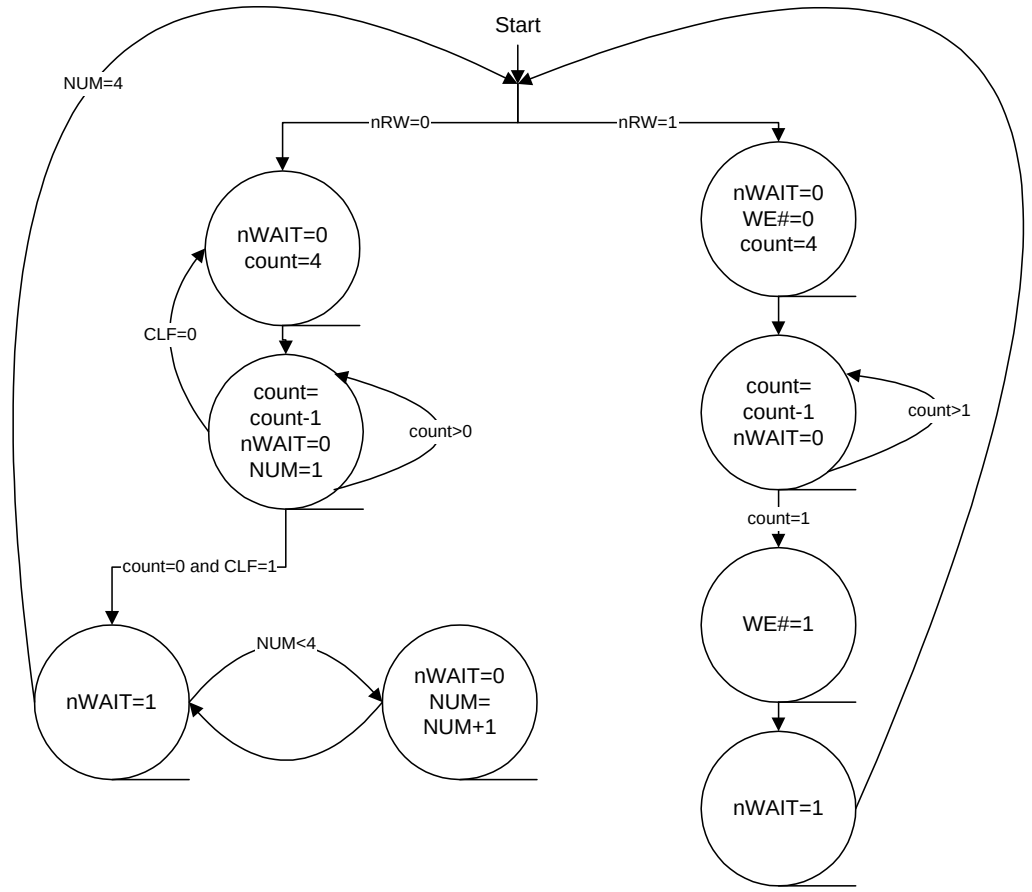
CLF: Cache Line Fill indicates if the current transfer is a burst transfer.

3.2.3. CONTROL SIGNAL GENERATION

In this interface, the SA-110 controls OE# directly with nRW. WE# is the same as nWAIT while nRW is high, and WE# is high at all other times. The decoder uses the upper addresses to generate chip enable signals. NWAIT is generated by a state machine in the PLD. Figure 6 is a block diagram of the interface, and Figure 7 is possible logic that could be used to generate nWAIT and WE#.

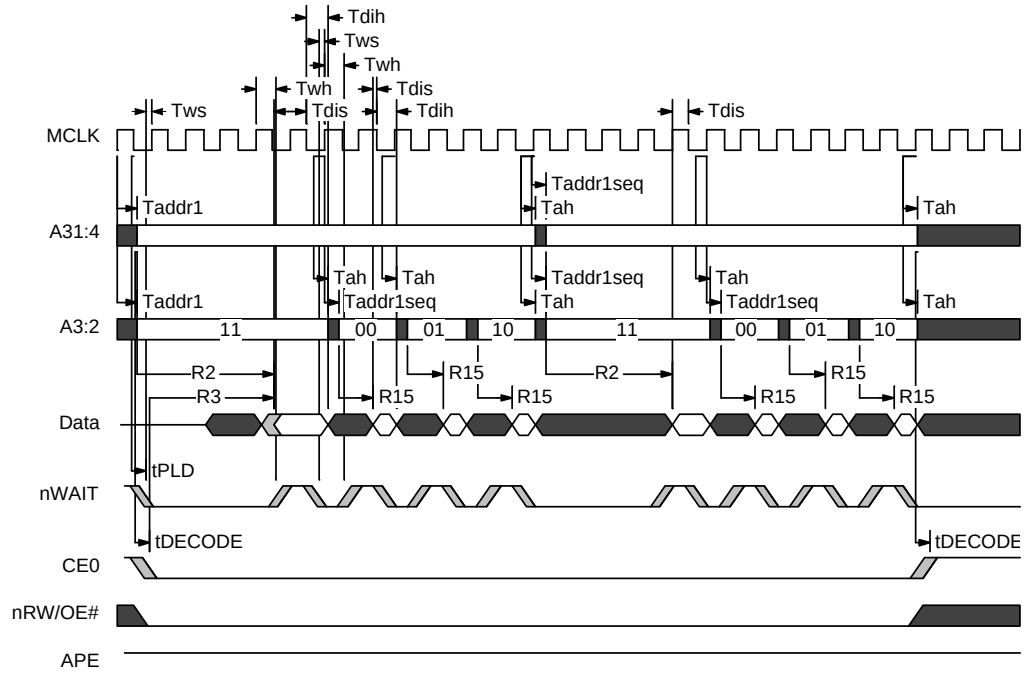
Figure 8 is a timing diagram of an 8-word cache line fill that does not start on a 4-word boundary. This shows the maximum delay that will be found for a cache line fill on the 32-Mbit 3 Volt Intel StrataFlash memory.

Figure 9 is a diagram of two writes followed by a single read. Either WE# or chip enable can be used to start a write. The address and data are latched on either WE# going high or the first chip enable change that disables the device. WE# goes high one clock cycle before nWAIT so that timing specifications for WE# pulse high and write recovery before read can be met.



NOTE:
This diagram assumes page-mode is enabled. Initial read waits assume 32-Mbit 3 Volt Intel ® StrataFlash™ memory.

Figure 7. 3 Volt Intel® StrataFlash™ Memory/SA-110 PLD Wait-State Generator Logic



NOTE:

Address line labels in the diagram refer to address lines on the SA-110. Address A_x on the SA-110 is connected to A_{x-1} on 3 Volt Intel® StrataFlash™ memory.

Figure 8. 3 Volt Intel® StrataFlash™ Memory/SA-110 Cache Line Fill at 40 MHz

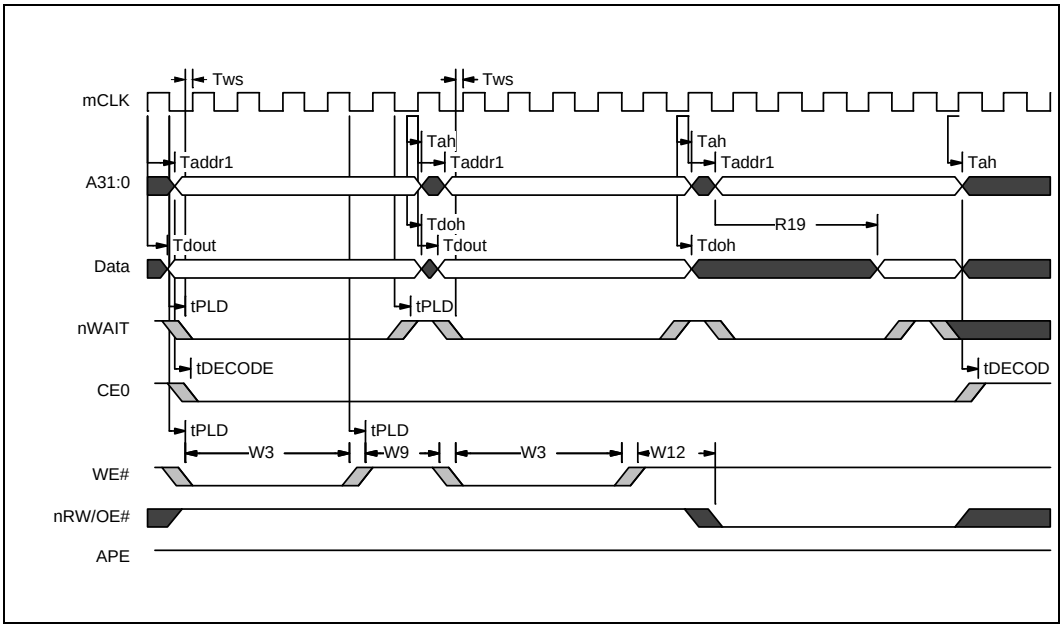


Figure 9. 3 Volt Intel® StrataFlash™ Memory/SA-110 Write Cycles Followed by Read

If a reset occurs when a block erase, program, or lock-bit configuration operation is taking place, RP# must remain low for a time of t_{PLPH} (35 µs). This is less than the time when the SA-110 holds nRESET_OUT low. Therefore, this should not be a concern if RP# is connected to nRESET_OUT. The 3 Volt Intel StrataFlash memory has a longer time between RP# going high to valid data (310 ns = t_{PHQV} + t_{PHRH}) than a normal initial read. This must be taken into account if the 3 Volt Intel StrataFlash memory is the first device to be read from after a reset. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

Consult the appropriate datasheets for specific information about the individual components in the interface (see Appendix A for a list of additional information).

3.3. Interfacing 3 Volt Intel® StrataFlash™ Memory to the StrongARM® SA-1100 at 190 MHz

The SA-1100 microprocessor delivers a combination of high performance and low power that can be useful for emerging portable applications. The SA-1100 incorporates a 32-bit StrongARM® RISC processor core as well as an on-board memory controller.

3.3.1. INTERFACE CONSIDERATIONS

By setting up certain registers, a glueless interface is achieved between 3 Volt Intel StrataFlash memory and the StrongARM SA-1100. The interface described in this application note uses two 32-Mbit Intel StrataFlash memory components to match the 32-bit data bus of the SA-1100 (DE-S1100-Ex). All components can interface at 3.3 V. The SA-1100 runs from a 1.5 V power supply, and the 3 Volt Intel StrataFlash memory uses a 2.7 V to 3.6 V. Both can interface between 3.0 V and 3.6 V. RCR.16 should be set to enable page-mode before page-mode timings are used. Figure 10 is a block diagram of the glueless interface between the two 32-Mbit 3 Volt Intel StrataFlash memory devices and SA-1100.

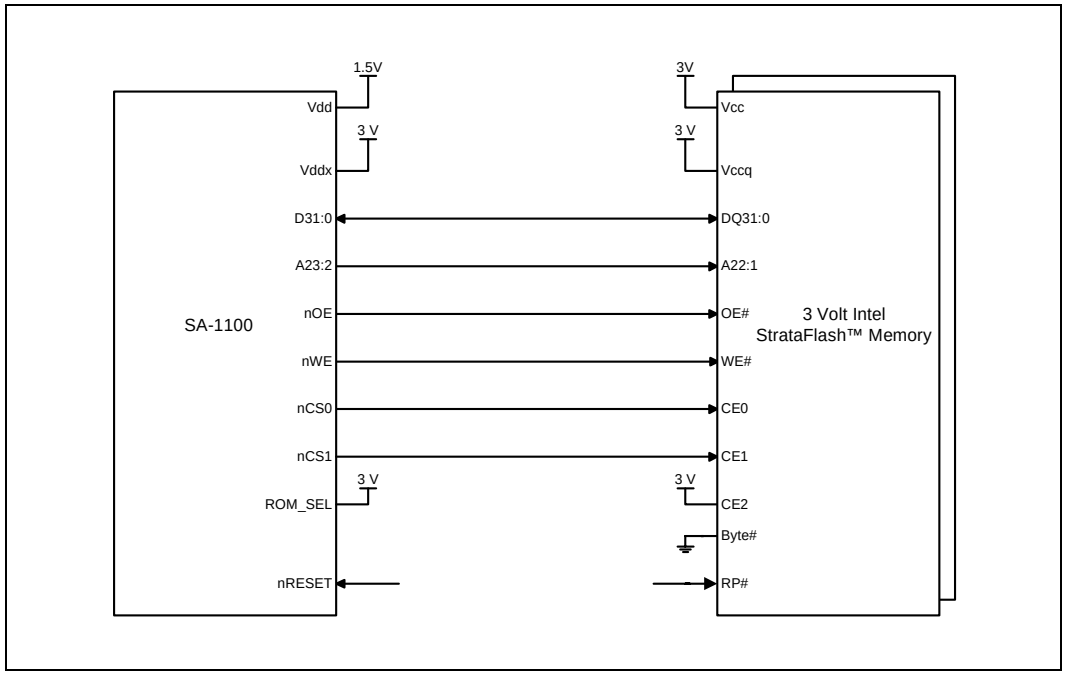


Figure 10. 3 Volt Intel® StrataFlash™ Memory/SA-1100 Interface

3.3.2. PROCESSOR INTERFACE SIGNALS

The following are signal descriptions for the SA-1100 (DE-S1100-Ex version):

$A_{25:0}$: The 26-bit address bus transmits addresses to memory from the processor.

nCS(3:0): Static chip selects. These signals are chip selects to static memory devices. nCS0 corresponds to address 0x00, which is where the boot device is expected to be.

$D_{31:0}$: The 32-bit data bus transfers data between the processor and memory.

nOE: The Not (active-low) Output Enable indicates the memory output enable.

nWE: The Not (active-low) Write Enable indicates to memory that writes are enabled.

ROM_SEL: ROM Select. This pin is used to configure the ROM width. If it is grounded, the ROM width is 16 bits. If it is pulled high, the ROM width is 32 bits.

3.3.3. CONTROL SIGNAL GENERATION

MSC1/MSC0 are SA-1100 memory control registers for configuring the interface to flash. Upon reset these values are forced to their slowest non-burst timings. Timing bits are specified as memory clock cycles. Memory clock cycles are half the rate of the internal CPU cycles. Each memory control register (MSC1/0) contains information for two memory regions as selected by CS3:0.

MSC0 (Bits 31-16) control the CS1 memory region
MSC0 (Bits 15-0) control the CS0 memory region
MSC1 (Bits 31-16) control the CS3 memory region
MSC1 (Bits 15-0) control the CS2 memory region

The following table describes the 32 bits of the first MSC control register (in a 190 MHz SA-1100) as it relates to flash.

Table 1. SA-1100 Memory Control Register Table

Bit	Name	Description	3 Volt Intel® StrataFlash™ Memory Read Region (CS0) Value (2242H)	3 Volt Intel StrataFlash Memory Write Region (CS1) Value (2642H)
1–0	RTx[1:0]	10 – Burst-of-four Flash	10b = 2 decimal	10b = 2 decimal
2	RBWx	Flash Bus Width 0 – 32 bits 1 – 16 bits	0b = 0	0b = 0
7–3	RDFx[4:0]	Flash Delay First Access This determines the read access time or first access of a burst flash. One memory clock cycle is added to this value.	01000b = 8 decimal	01000b = 8 decimal
12–8	RDNx[4:0]	Read: Flash Delay Next Access (Page access) Number of memory clock cycles (minus 1) from address to data valid for subsequent accesses of a burst flash.	00010b = 2 decimal	
		Write: Flash Write Pulse Width Low This determines the write pulse width when writing to flash. One memory clock cycle is added to this value.		00110b = 6 decimal
15–13	RRRx[2:0]	Flash Write Pulse Width High/ Write Recovery Before Read Write pulse width high and write recovery before read is 2*RRR + 1 memory cycle.	001b = 1 decimal	001b = 1 decimal

The parameter RDN is used for both the page-access time during reads and the flash write-pulse-width-low time during writes. Because of this, read performance is impacted (read page access time becomes 74 ns) if the same memory region (e.g., CS0) is used for reading and writing to the flash. To work around this, the flash is read from one memory region (CS0) and written to in another region (CS1). The timings are optimized for each region thus improving read performance. Because of Intel StrataFlash memory's CE logic, no additional glue logic is required.

To configure the 3 Volt Intel StrataFlash memory read region as shown in Figure 10, the MSC0[15:0] register should be set to a value of 2242H. Page mode read timing diagrams for a 190 MHz SA-1100 device are generated using this value. Figure 12 depicts this page-mode read timing diagram.

To configure the 3 Volt Intel StrataFlash memory write region, the MCS1[15:0] register should be set to a value of 2642H. Figure 13 displays the write-timing diagram for a 190 MHz SA-1100 device.

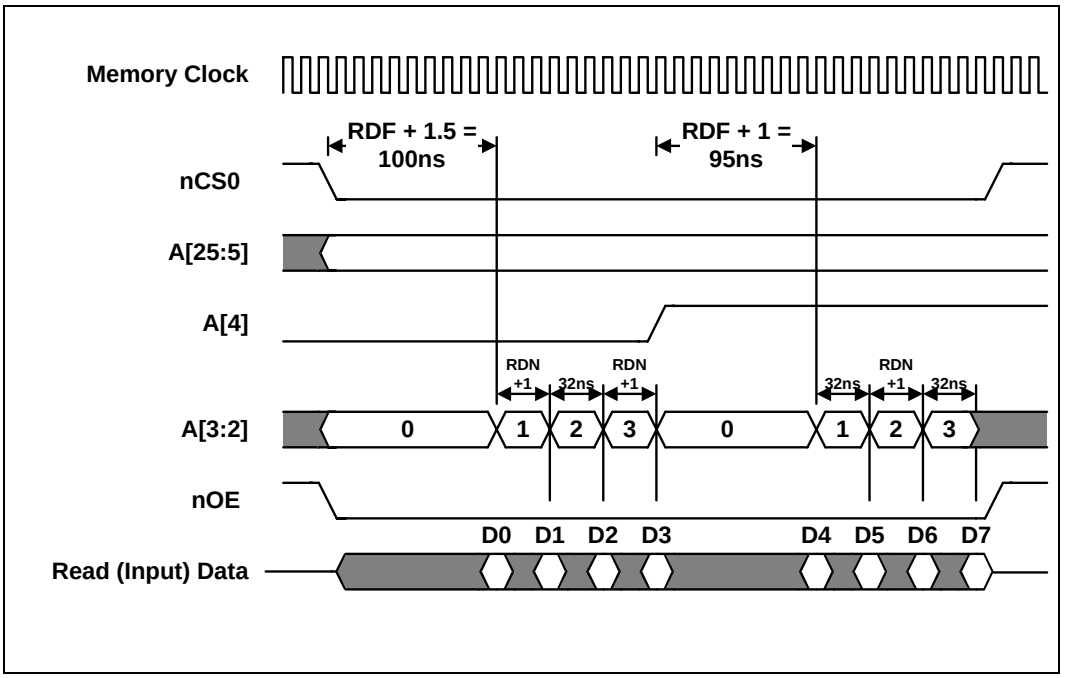


Figure 11. 3 Volt Intel® StrataFlash™ Memory and SA-1100 at 190 MHz Page Mode Read Timing Diagram (CS0 Memory Region)

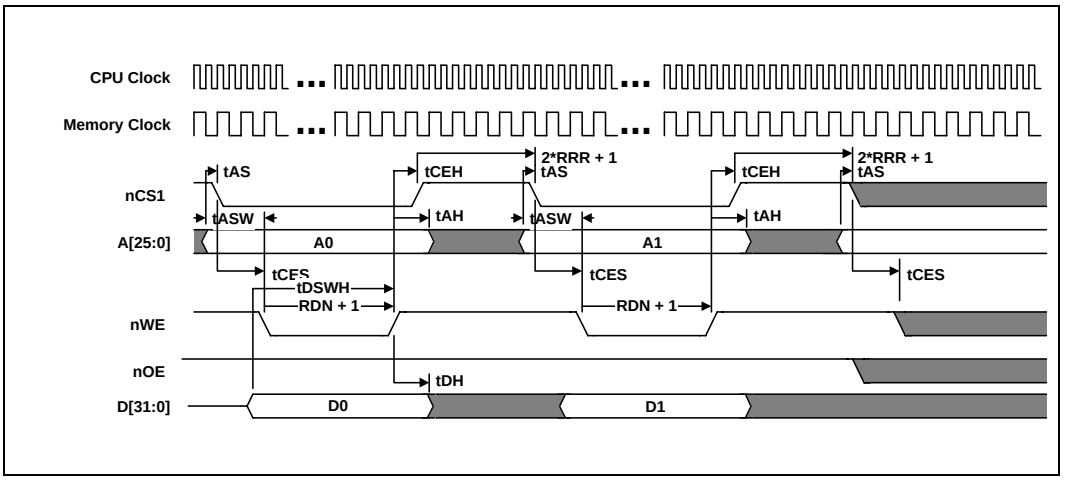


Figure 12. 3 Volt Intel® StrataFlash™ Memory and SA-1100 at 190 MHz Write Timing Diagram (CS1 Memory Region)

The following is a table of write timing values generated by the SA-1100 at 190 MHz and the corresponding 3 Volt Intel StrataFlash memory minimum spec. requirement.

Table 2. Write Timing Table

SA-1100 Variable	SA-1100 Description	SA-1100 at 190 MHz Values	3 Volt Intel® StrataFlash™ Memory Variable	3 Volt Intel StrataFlash Memory Description	3 Volt Intel StrataFlash Memory Min. Spec. Requirement
t_{CES}	nCS setup to nWE low (4 CPU cycles)	21 ns	t_{ELWL}	CEx low to WE# going low	0 ns
	Write pulse width (2*RDN + 2 CPU cycles)	74 ns	t_{WP}	Write pulse width	70 ns
t_{DSWH}	Write data setup to nWE high (2*RDN + 3 CPU cycles)	79 ns	t_{DVWH}	Data setup to WE# going high	50 ns
t_{AS}	Address setup to nCS low (1 CPU cycle)	5 ns			NA
t_{ASW}	Address setup to nWE low (5 CPU cycles)	26 ns			NA
	(t_{AS} + t_{DSWH})	100 ns	t_{AVWH}	Address setup to WE# going high	50 ns
t_{CEH}	nCS held asserted after nWE deasserted (2 CPU cycles)	11 ns	t_{WHEH}	CEx hold from WE# high	10 ns
t_{DH}	Data hold after nWE high (3 CPU cycles)	16 ns	t_{WHDX}	Data hold from WE# high	0 ns
t_{AH}	Address hold after nWE deasserted (3 CPU cycles)	16 ns	t_{WHAX}	Address hold from WE# high	0 ns
	(t_{CES} + 4*RRR+2 + t_{CEH} CPU cycles)	63 ns	t_{WPH}	Write pulse width high	30 ns
	(t_{CEH} + 4*RRR+2 CPU cycles)	42 ns	t_{WHGL}	Write recovery before read	35 ns

NOTE:
All the 3 Volt Intel StrataFlash memory write parameter minimum requirements were met by the SA-1100.

If a reset occurs when a block erase, program, or lock-bit configuration operation is taking place, RP# must remain low for a time of t_{PLPH} (35 µs). This is significantly less than the time the SA-1100 requires nRESET to be held active (150 ms). Therefore, this should not be a concern if RP# is connected to nRESET. After reset, the 3 Volt Intel StrataFlash component has a minimum requirement of 310 ns (t_{PHQV} + t_{PHRH}) between RP# going high to valid data. After power-on or hard reset, the SA-1100 configures the static interface for the boot flash (connected to CS0) for the slowest non-burst flash (RDF=0x1FH). For the 190 MHz device, the first access occurs 342 ns after nRESET goes high. This exceeds the required minimum time of the 3 Volt Intel StrataFlash memory device. For faster versions of the SA-1100 that do not meet this requirement, a delay should be inserted. Reference *AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#* for details about CPU reset and RESET# timing. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

The following is a table of reset timing values for the SA-1100 at 190 MHz and the corresponding 3 Volt Intel StrataFlash memory minimum spec. requirement.

Table 3. Read Timing Table

SA-1100 Variable	SA-1100 Description	SA-1100 at 190 MHz Values	3 Volt Intel® StrataFlash™ Memory Variable	3 Volt Intel StrataFlash Memory Description	3 Volt Intel StrataFlash Memory Min. Spec. Requirement
	nRESET pulse width (min. requirement)	150 ms	t_{PLPH}	RP# pulse low time	35 µs
			t_{PHRH}	RP# high to reset during erase, program, or lock-bit configuration	100 ns
			t_{PHQV}	Reset to output delay	210 ns
	Flash delay first access after nRESET goes high (32.5 memory cycles)	342 ns	$t_{PHRH} + t_{PHQV}$		310 ns

NOTE:
All the 3 Volt Intel StrataFlash memory reset parameter minimum requirements were met.

Consult the appropriate datasheets for specific information about the individual components in the interface (see Appendix A for a list of additional information).

3.4. Interfacing the 3 Volt Intel® StrataFlash™ Memory to Intel® StrongARM® SA-1110 at 66 MHz

By setting certain registers, this reference design is a glueless interface between the 3 Volt Intel StrataFlash and the Intel StrongARM SA-1110. The designers should use two 128-Mbit Intel StrataFlash memory to match the 32-bit data bus of the SA-1110.

Figure 13 illustrates the block diagram of the 3 Volt Intel StrataFlash memory interfaces to the Intel StrongARM SA-1110.

3.4.1. INTERFACE CONSIDERATIONS

By setting certain registers, this reference design is a glueless interface between Eclipse and the Intel StrongARM SA-1110. The designers should use two 128-Mbit Intel StrataFlash memory to match the 32-bit data bus of the SA-1110.

This sample interface uses two 3 Volt Intel StrataFlash memory in 16-bit mode. Timing diagrams were made with the 128-Mbit 3 Volt Intel StrataFlash memory with the memory bus running at 66 MHz. There is no other required logic between the processor and the 3 Volt Intel StrataFlash memory.

This reference interface in this document uses page-mode timings. Before the 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set to b'1 to enable the page-mode.

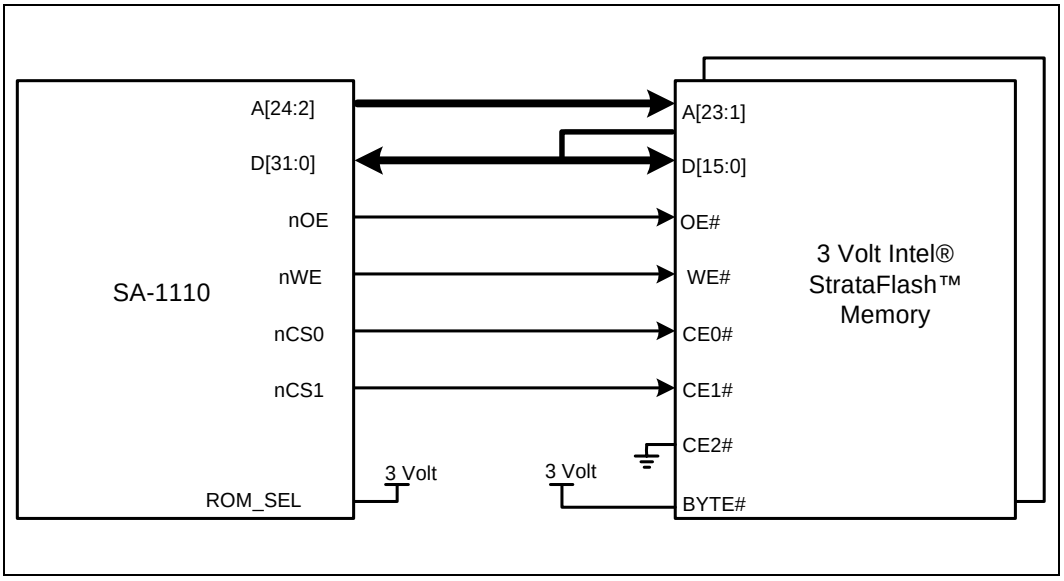


Figure 13. 3 Volt Intel® StrataFlash™ Memory/SA-1110 Microprocessor Interface

3.4.2. PROCESSOR INTERFACE SIGNALS

This interface uses the following signals provided by the SA-1110:

$A_{25:0}$: The 25-bit address bus transmits instruction and data addresses to memory.

$D_{31:0}$: The bi-directional data bus transfers data between the processor and memory.

NCS(3:0): These signals are chip selects to static memory devices.

OE: Output Enable indicates the memory output enable.

WE: Write Enable indicates to memory that writes are enabled.

ROM_SEL: ROM Select. This pin is used to configure the ROM width. If it is grounded, the ROM width is 16 bits. If it is pulled high, the ROM width is 32 bits.

3.4.3. CONTROL SIGNAL GENERATION

Figure 14 shows a four-word page-mode read timing diagram. For this four flash read, the RDF[7:3] should be set h'0A, RDN[12:8] should be set to h'02 and RRR[15:13] should be set h'1 in the MSC0 register.

Figure 15 shows the Write timing diagram. RDN[12:8] should be set to b'0100 in the MSC1 register.

The following signal can be found in the *Intel® StrongARM® SA-1110 Microprocessor Advanced Developer's Manual*: t_{CSD}, t_{MFOV}, t_{MROV}, t_{DS}, t_{DH}, RDF, RDN, RRR.

The following signal can be located in the *3 Volt Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 28F320J3A* datasheet: R2, R3, R9, R15.

Read all appropriate documentation before attempting this interface.

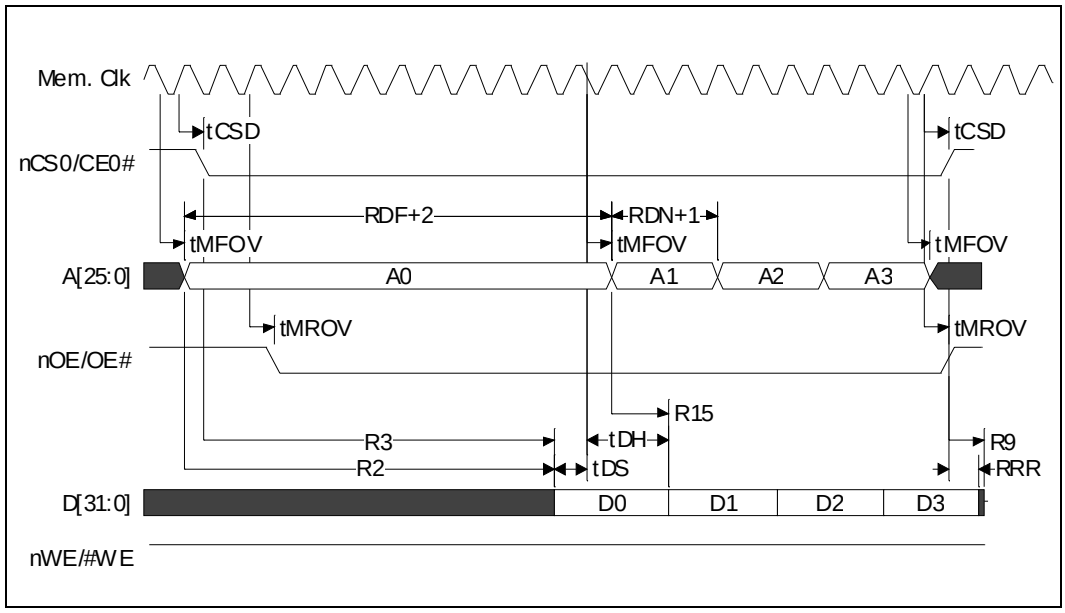


Figure 14. 3 Volt Intel® StrataFlash™ Memory/SA-1110 Four-Word Page-Mode Read Cycle at 66 MHz

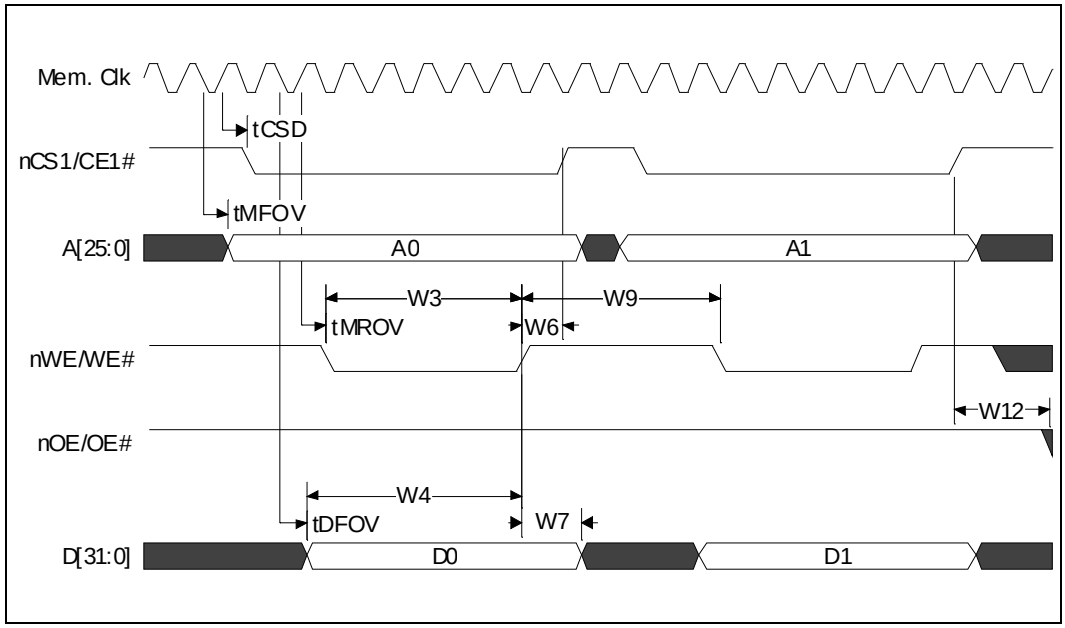


Figure 15. 3 Volt Intel® StrataFlash™ Memory/SA-1110 Write Timing Diagram at 66 MHz

3.5. Interfacing 3 Volt Intel® StrataFlash™ Memory to MC68060 at 66 MHz

The MC68060 series of microprocessors by Motorola offers performance of over 100 MIPS at 66 MHz. The RISC-based processor includes separate 8-kilobyte instruction and data caches. The MC68060 comes with both a floating point unit and a memory management unit, and the MC68LC060 comes with an MMU but no FPU, and the MC68EC060 comes with neither an MMU nor an FPU.

3.5.1. INTERFACE CONSIDERATIONS

This sample interface between the MC68060 and 3 Volt Intel StrataFlash memory uses two 3 Volt Intel StrataFlash memory chips to match the MC68060's 32-bit bus, and standard system logic such as a decoder and a PLD. The timing diagrams and other specifications were made assuming a 66 MHz bus and the 32-Mbit 3 Volt Intel StrataFlash memory. Other bus speeds and memory sizes could be used by modifying this slightly. Both the MC68060 and the 3 Volt Intel StrataFlash memory can interface at 3 V and 5 V. Minimum and Maximum delays for the decoder and PLD are shown in the table below. These min/max numbers are used for the timings shown in Figure 18 and Figure 19. This sample interface does not include information about bus arbitration signals such as BG#, BB#, and BTT#. They should be asserted or negated as necessary for bus control.

Device	Min	Max
Decoder	0 ns	19 ns
PLD	0 ns	9 ns

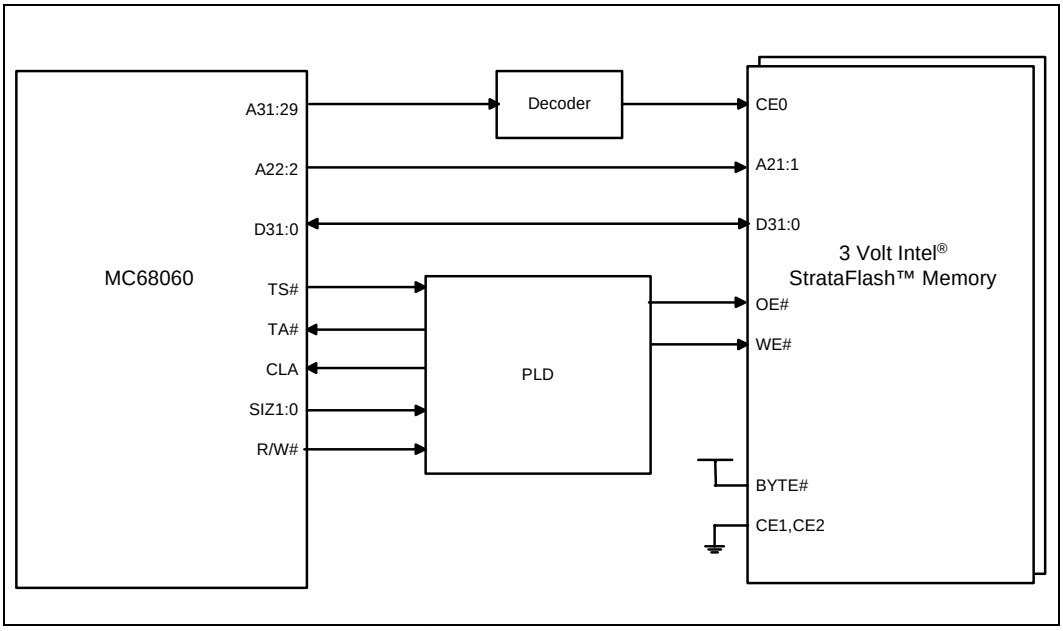


Figure 16. 3 Volt Intel® StrataFlash™ Memory/MC68060 Interface

3.5.2. PROCESSOR INTERFACE SIGNALS

$A_{31:2}$: The address bus transfers address from processor to memory.

$D_{31:0}$: The data bus carries data between the processor and memory.

TS#: Transfer Start is asserted by the processor at the start of a bus cycle.

TA#: Transfer Acknowledge is asserted to the processor to acknowledge a data transfer.

CLA: Cycle Long-Word Address can be toggled to change A3 and A2.

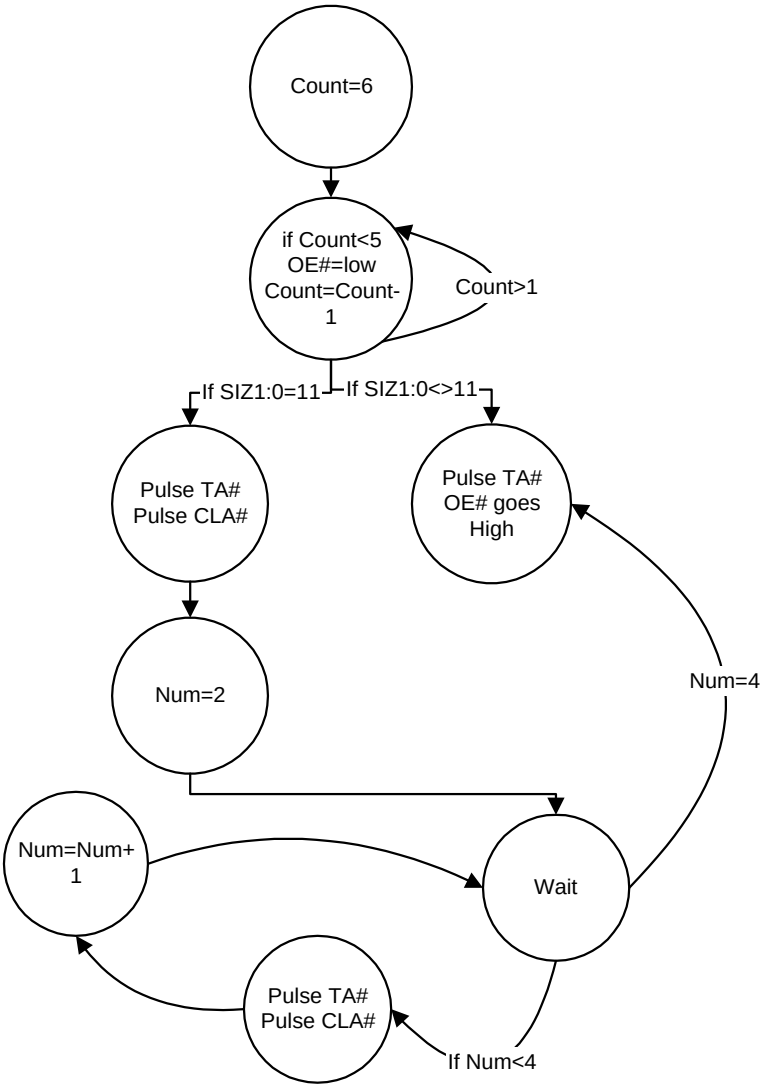
SIZ1:0: Defines the size of the transfer in progress and indicates if the current transfer is a cache line transfer.

R/W#: Indicates if current transfer is a read or a write.

3.5.3. CONTROL SIGNAL GENERATION

Figure 16 is a block diagram of the interface. CE_0 is generated from a decoder; CE_1 and CE_2 are tied to ground. OE# and WE# are generated by the PLD. R/W# is used to determine if the cycle is a read or a write. TS# indicates the start of a transfer cycle. SIZ1:0 are used by the PLD to determine if the transfer is a single transfer or a cache line transfer. TA# is used to indicate the completion of a transfer and can be used to create wait-states. CLA is used to control the changing of the lower addresses on cache line transfers.

The PLD logic used to generate TA#, CLA, and OE# for read operations is outlined in Figure 17. TS# is used to initiate all data transfers. If R/W# indicates a write, WE# should be asserted. If R/W# indicates a read, the PLD should wait several cycles before asserting OE#. This is to make certain that the specified time from WE# high to OE# low (t_{WHGL}) has elapsed before the assertion of OE# in case the previous transaction was a write. TA# should be asserted when the 3 Volt Intel StrataFlash memory has placed valid data on the bus. If SIZ1:0 is 11b, CLA should also be asserted with TA#, and if the cycle is a read, page-mode timings should be used.



NOTE:
Diagram assumes page-mode is enabled and accesses are sequential. Initial wait-states are for 32-Mbit 3 Volt Intel® StrataFlash™ memory.

Figure 17. 3 Volt Intel® StrataFlash™ Memory/MC68060 Wait-State Generator Logic Diagram for Read Operations

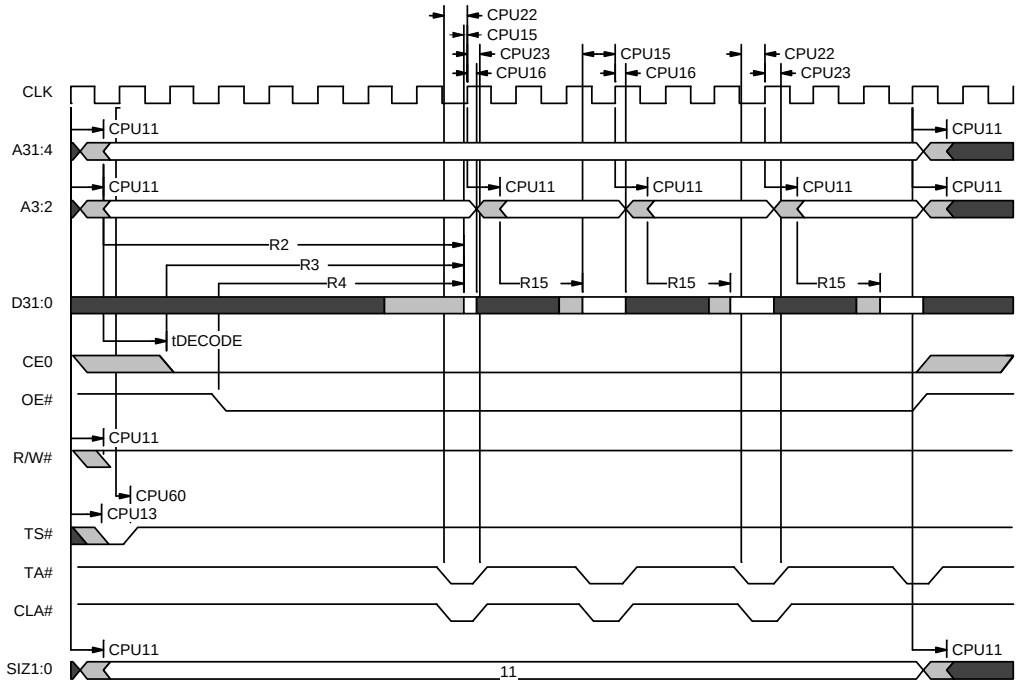
Figure 18 is a timing diagram of a line read transfer. The transfer is initiated when TS# is pulsed low by the processor. In the same clock cycle, address and other information is placed on the bus. OE# is asserted later, and when the data becomes valid, TA# is pulsed to complete the first word transfer and CLA# is pulsed to change the lower addresses. In the case of a line read transfer, the next three addresses are inside the page, so page-mode timings can be used. The processor does not pulse TS# a second time, but TA# and CLA# are asserted like the first transfer.

Figure 19 is a timing diagram of two writes followed by a single read. The PLD asserts WE# low the cycle after TS# is asserted. It then must wait for WE# pulse low (t_{WP}) to elapse before making WE# high. After WE# is high, TA# can be pulsed low so the next cycle can begin. For consecutive writes or reads following writes, the WE# pulse high and write recovery before read times must be met.

Several considerations must be taken into account for reset. If a block erase, program, or lock-bit configuration is taking place when RP# is asserted, RP# must be held low for a period of t_{PLPH} (35 µs). After RP# is high, there is a time of 310 ns (t_{PHQV} + t_{PHRH}) before data from a read can be returned. For external resets to the MC68060, after RSTI# goes high, the processor is held in reset internally for 27 clock cycles, which is enough to meet t_{PHQV} + t_{PHRH}. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

The only portion of the MC68060 processor's memory map that is fixed is the initial reset vector. All other addresses can be translated using the MC68060 processor's internal Memory Management Unit. The initial reset vector is located at 000h, so to boot from the 3 Volt Intel StrataFlash memory, it should be placed at that address. For purposes other than initial reset, the 3 Volt Intel StrataFlash memory may be placed in the portion of the memory map that makes it most convenient for the user.

Read all appropriate datasheets before attempting an interface (see Appendix A for a list of additional information).



NOTE:

The address line labels in this diagram refer to the labels on the 68060. A_x on the 68060 is A_{x-1} on 3 Volt Intel® StrataFlash™ memory

Figure 18. 3 Volt Intel® StrataFlash™ Memory/MC68060 Page-Mode Reads at 66 MHz

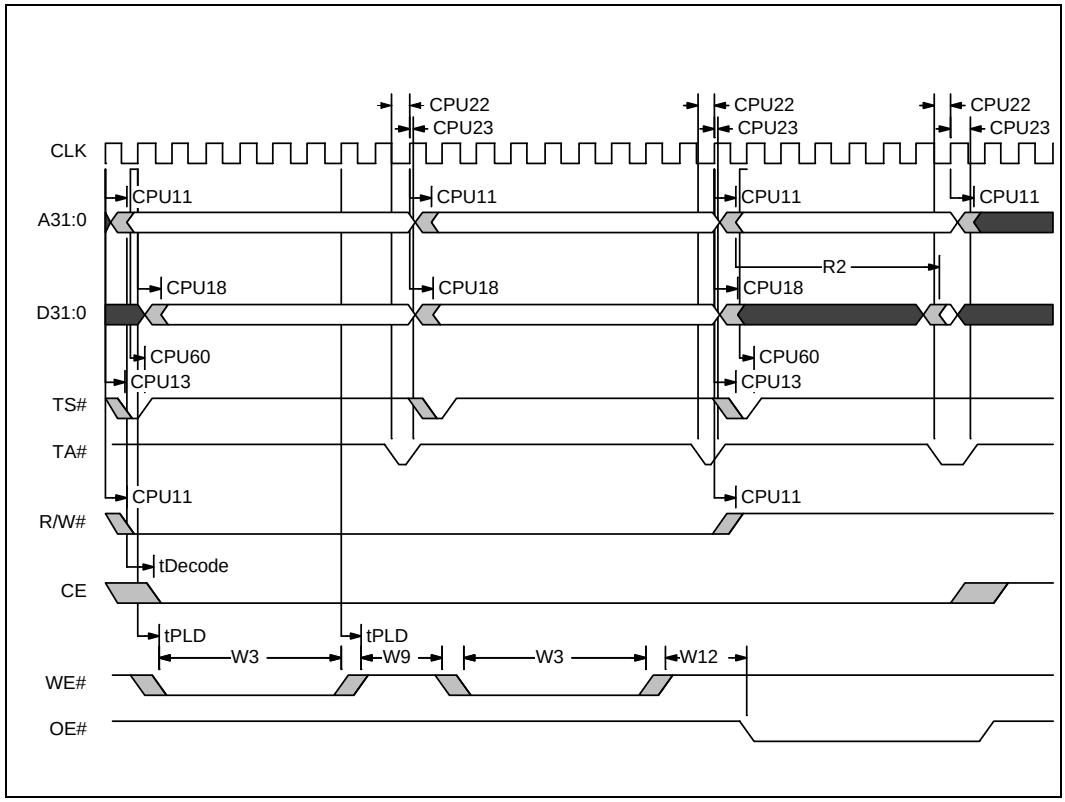


Figure 19. 3 Volt Intel® StrataFlash™ Memory/ MC68068 Write Cycles Followed by Read Cycle at 66 MHz

3.6. Interfacing 3 Volt Intel® StrataFlash™ Memory to MPC603e at 66 MHz

The MPC603 (PPC603e) PowerPC microprocessor by IBM and Motorola is a low power implementation of the PowerPC family of RISC microprocessors. This superscalar processor can issue and retire as many as three instructions at once. It supports bus speeds between 25 MHz and 66 MHz. This interface was written with a 66 MHz bus. All examples and diagrams were made with the 32-Mbit 3 Volt Intel StrataFlash memory device as a reference. Figure 20 is a block diagram of the interface between the MPC603e and the 3 Volt Intel StrataFlash memory.

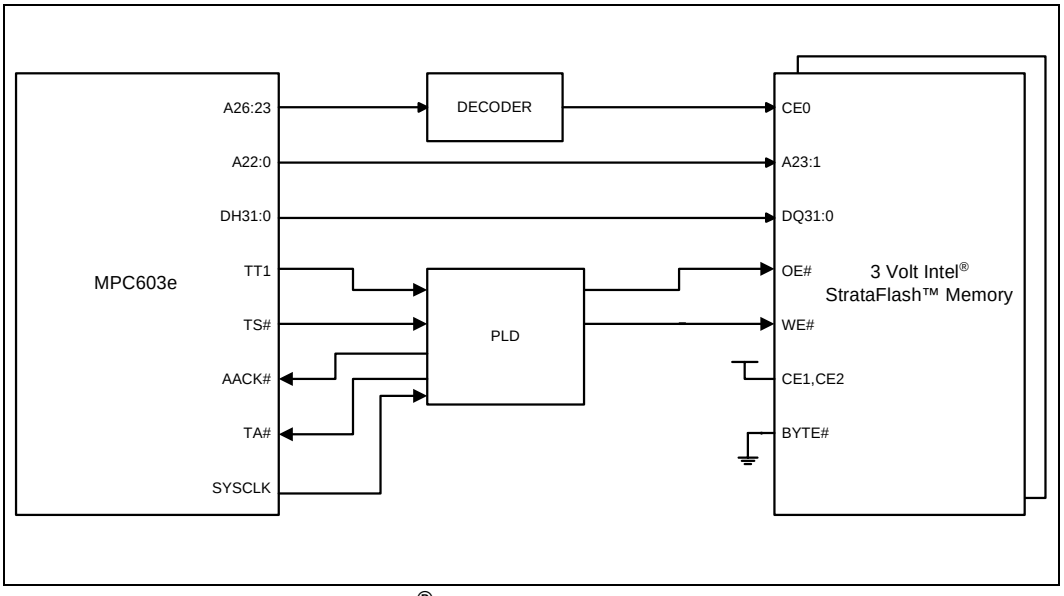


Figure 20. 3 Volt Intel® StrataFlash™ Memory/MPC603e Interface

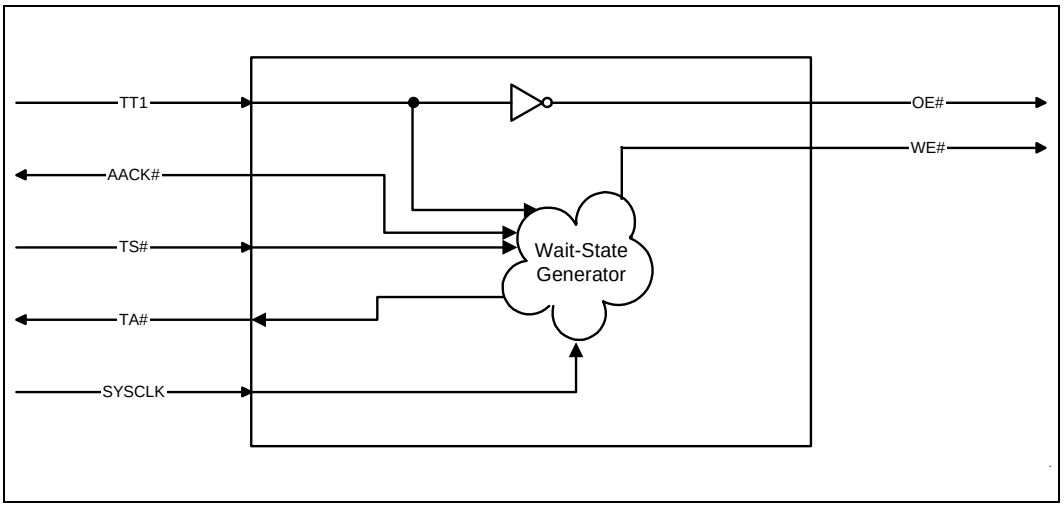


Figure 21. 3 Volt Intel® StrataFlash™ Memory/MPC603e PLD Configuration

3.6.1. INTERFACE CONSIDERATIONS

The interface uses two of the 3 Volt Intel StrataFlash memory components to match the MPC603e's data bus in 32-bit mode. It also uses a PLD and a decoder. These may be integrated into an ASIC. Connecting address lines directly to the 3 Volt Intel StrataFlash memory's three chip enable pins could eliminate the need for a decoder and decrease the time for the initial memory access. All components can run on a 2.7 V–3.6 V power supply. The minimum and maximum delay specifications for the PLD and decoder as shown in Figure 23 and Figure 24 are in the table below. This interface assumes that all bus arbitration signals have been used so that the MPC603e is the bus master.

Device	Min	Max
PLD	0	11
Decoder	0	18

3.6.2. PROCESSOR INTERFACE SIGNALS

This interface uses the following signals provided by the MPC603e:

$A_{31:0}$: The 32-bit address bus transfers addresses from the processor to memory.

$DH_{31:0}$: The half of the 64-bit data bus that is used in 32-bit mode. Transfers information between processor and memory.

TS#: The Transfer Start indicates that a transfer is will start in the next clock cycle.

AACK#: The Address Acknowledge is received by the processor after memory no longer needs the address on the bus.

TA#: The Transfer Acknowledge is received by the processor when the data has been placed on the bus.

TT1: The Transfer Type 1 signal is part of an encoding about the transfer in progress.

3.6.3. CONTROL SIGNAL GENERATION

The 3 Volt Intel StrataFlash memory's CE_0 signal is taken directly from the decoder. CE_1 and CE_2 are tied low. Inverting TT1 in the PLD gives OE#. TA# and AACK# are generated by a wait-state generator in the PLD. In read operations with a 32-Mbit part, they are high for five clock cycles after TS# is asserted, then go low for one clock cycle. AACK# must always go low before TA#. Figure 20 is a block diagram of the interface. Figure 21 is a diagram of the internal PLD configuration.

Figure 23 is a timing diagram of a single read. At the start of the transfer, the processor asserts TS# low. AACK# is used to make the processor hold the address until the 3 Volt Intel StrataFlash memory has output the data. Several clock cycles after TS# is asserted, the PLD forces AACK# and TA# low. For subsequent accesses within the page, AACK# and TA# can be asserted one full clock cycle after TS# is pulsed low. If the 3 Volt Intel StrataFlash memory is being accessed sequentially, the lower two address lines can be used by the PLD to tell when the memory access is off the page. Figure 22 is possible logic for the PLD wait-state generator.

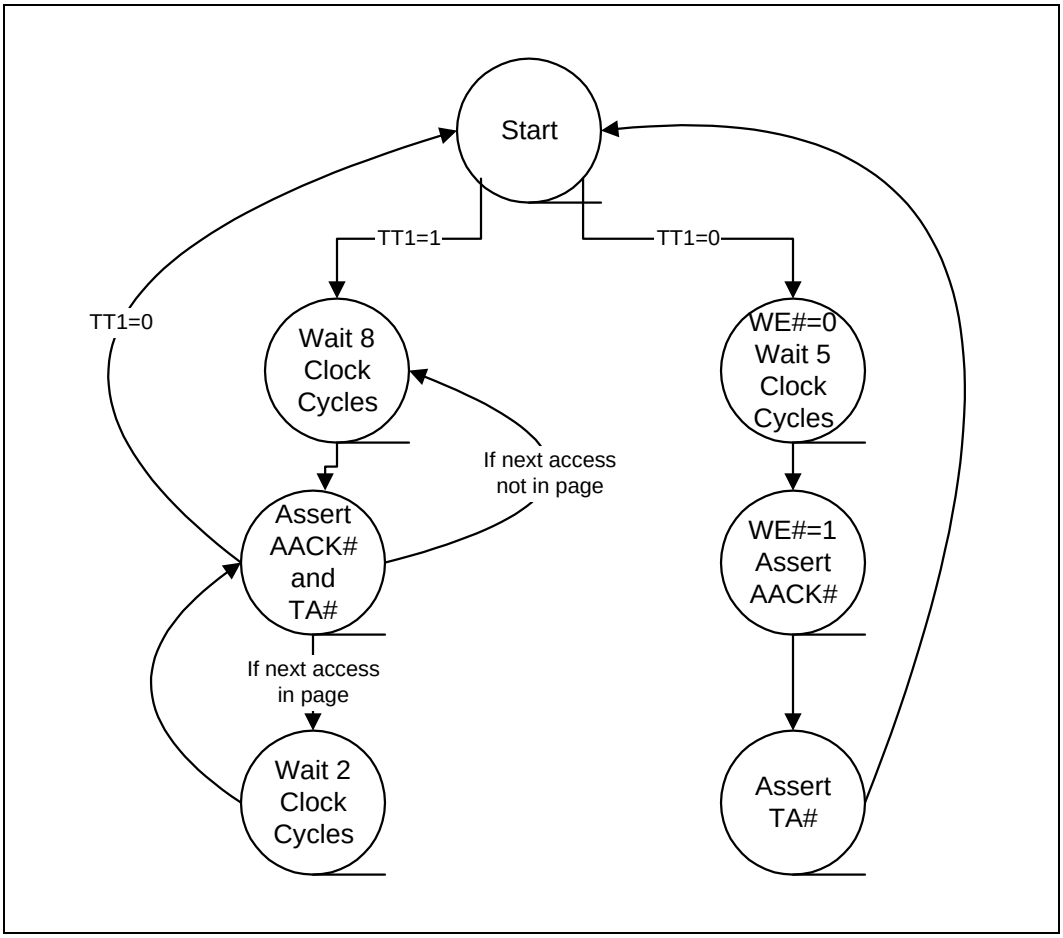


Figure 22. 3 Volt Intel® StrataFlash™ Memory/MPC603e Wait-State Logic

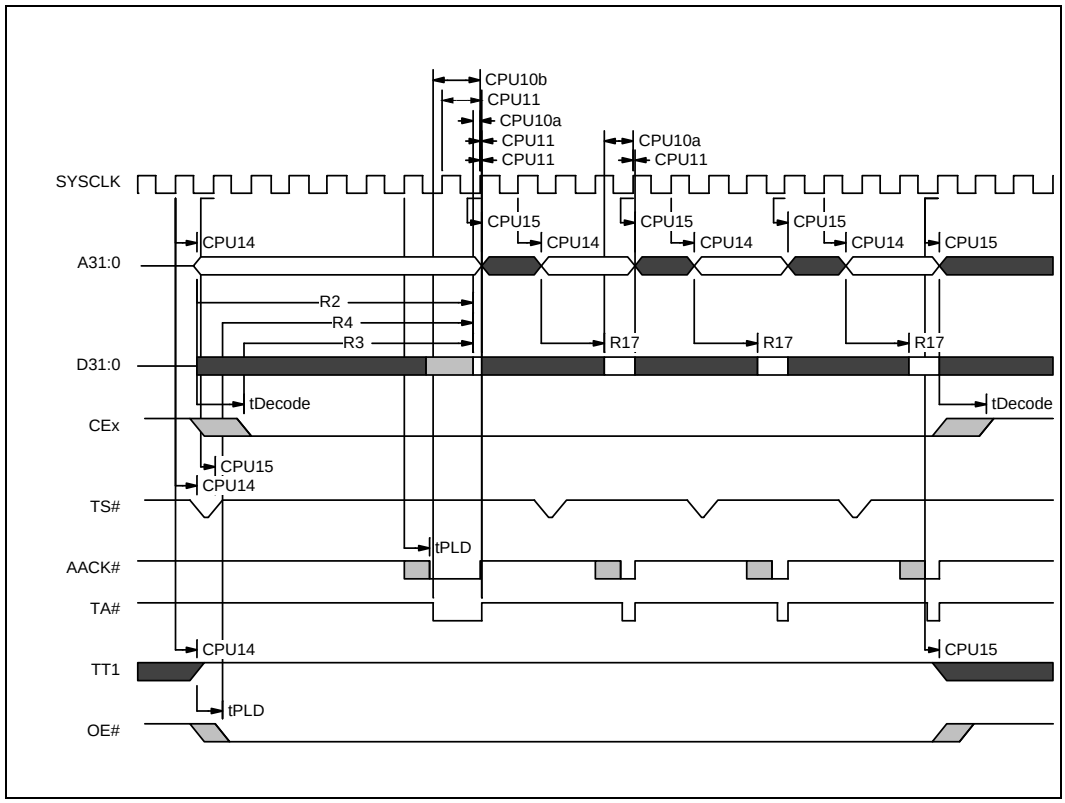


Figure 23. 3 Volt Intel® StrataFlash™ Memory/MPC603e Page-Mode Reads at 66 MHz

Figure 24 shows two writes followed by a read. In write operations, the PLD must generate WE# in addition to pulsing AACK# and TA#. TT1 is used to trigger WE# low, which must be deasserted in the fifth clock cycle after TS# pulses with 66 MHz clock. AACK# should be pulsed low on the same clock cycle WE# goes high, and TA# pulsed low one clock cycle after that.

Several timing considerations must be taken into account for reset. When asserted, RP# on the 3 Volt Intel StrataFlash memory must be held low for a time of at least t_{PLPH} (35 µs) when block erase, program, or lock-bit configuration commands are being executed. When HRESET# is used to reset the MPC603e, the processor requires it to be held low for at least 255 clock cycles, which at 66 MHz is 3.8 µs. If RP# is connected directly to HRESET# or SRESET#, the time t_{PLPH} (35 µs) must be taken into account. In addition, the 3 Volt Intel StrataFlash memory has a delay of 310 ns (t_{PHQV} + t_{PHRH}) after RP# becomes high until the first output is available. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

Read all pertinent datasheets before attempting an interface.

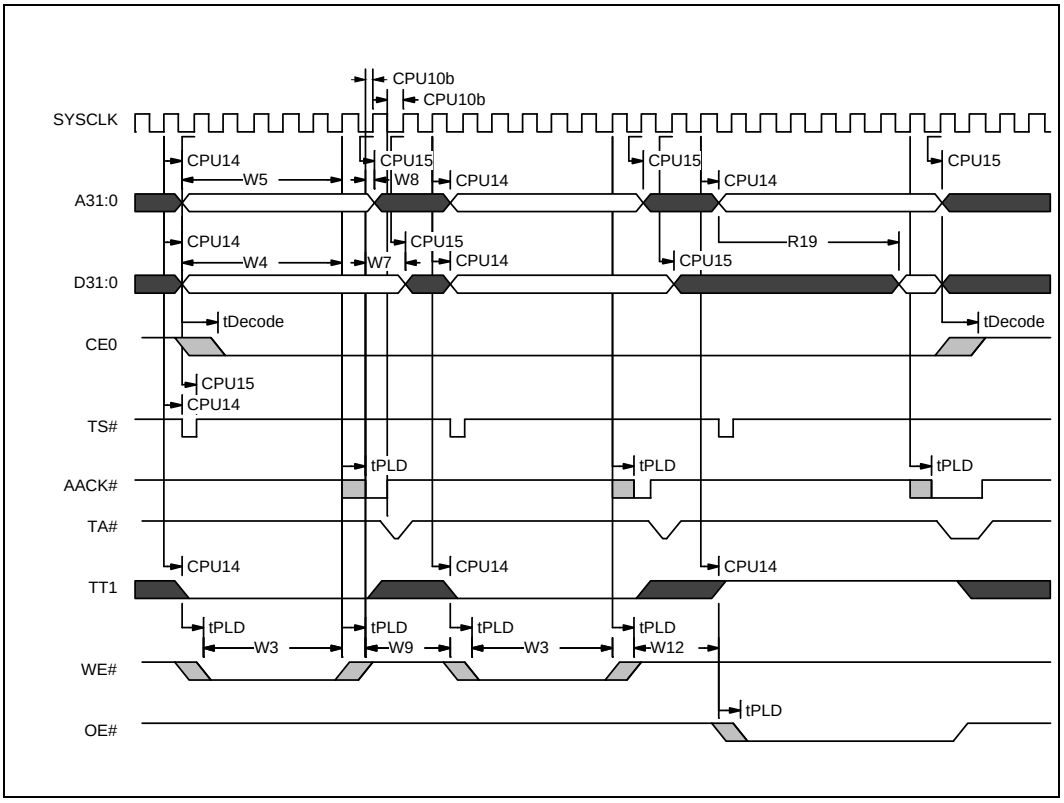


Figure 24. 3 Volt Intel® StrataFlash™ Memory/MPC603e Write Cycles Followed by Read Cycle

3.7. Interfacing 3 Volt Intel® StrataFlash™ Memory to i960® H Processor at 40 MHz

The Intel® i960® HA/HD/HT processor series provides higher performance levels while maintaining backward compatibility with the i960® CA/CF processors. The i960 HA/HD/HT processors can run at 1x, 2x, or 3x bus speed, and execute up to 150 million instructions per second. This sample interface with the 3 Volt Intel StrataFlash memory device is written with a bus speed of 40 MHz, and timings use the 32-Mb flash component.

3.7.1. INTERFACE CONSIDERATIONS

The interface uses two 3 Volt Intel StrataFlash memory components to match the i960 H processor's 32-bit data bus, a decoder to generate CE_0, and a PLD to generate WE#. The decoder for this interface should have a delay no greater than 22 ns. The i960 Hx processor and the 3 Volt Intel StrataFlash memory can both have power supplies and input/outputs of 3.3 V. The i960 processor has an internal wait-state generator with programmable wait-states and other attributes. The address space that the 3 Volt Intel StrataFlash memory occupies should be set for non-pipeline, burstable (for page-mode accesses), nonparity, with READY# enabled, a 32-bit data bus width, and N_{RAD}=4, N_{RDD}=1, N_{WAD}=4, N_{WDD}=3, and N_{XDA}=0.

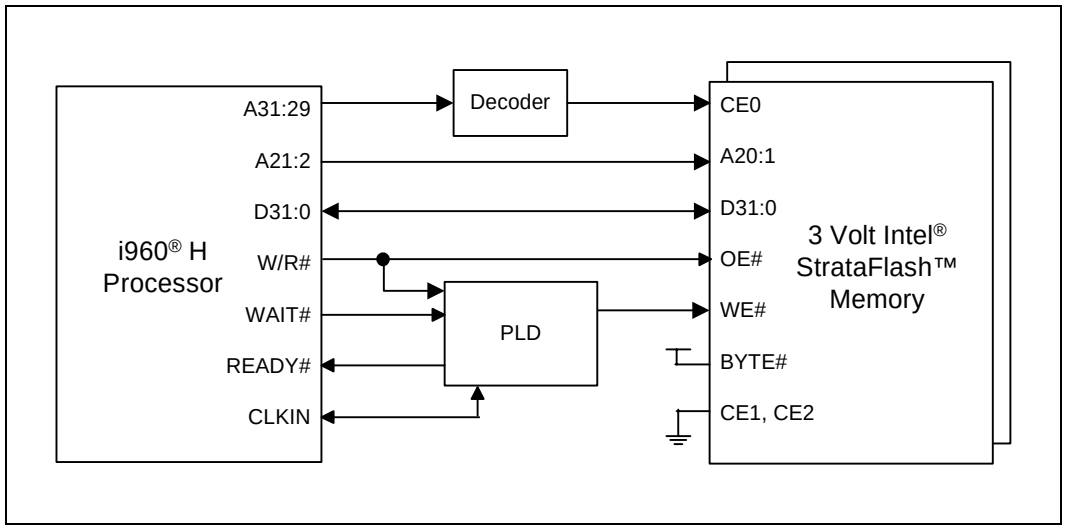


Figure 25. 3 Volt Intel® StrataFlash™ Memory/i960® H Processor Interface

3.7.2. PROCESSOR INTERFACE SIGNALS

The interface uses the following signals provided by the i960 H processor:

$A_{31:2}$: The upper 30 bits of the address. Used to identify all addresses within a 4-byte boundary.

$D_{31:0}$: The 32-bit data bus.

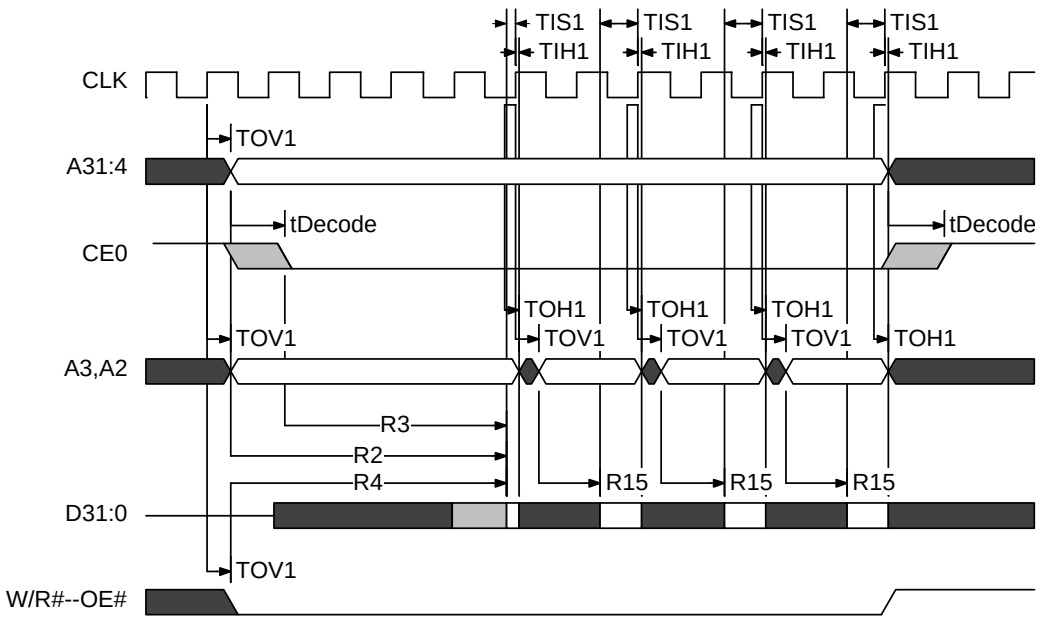
W/R#: Write/Read indicates whether the current transfer is a read or a write. It is low for read and high for write.

WAIT#: Output from the i960 processor indicates the status of the i960 H processor's internal wait-state generator.

READY#: Input to the i960 processor to indicate if wait-states are needed in addition to those programmed in the processor's wait-state generator.

3.7.3. CONTROL SIGNAL GENERATION

Figure 25 is a block diagram of the interface. CE_0 is taken directly from the decoder. CE_1 and CE_2 are tied low. OE# is taken from W/R#. WE# and READY# are generated inside the PLD from W/R# and WAIT#. The PLD asserts WE# and READY# for write cycles. For read cycles, READY# does not need to be asserted because the i960 H processor's internal wait-state generator can create the necessary wait-states.



NOTE:

The address line labels in this diagram refer to the labels on the i960 H CPU. A_x on the i960 H CPUis connected to A_{x-1} on 3 Volt Intel® StrataFlash™ memory.

Figure 26. 3 Volt Intel® StrataFlash™ Memory/i960® H Processor Page-Mode Reads

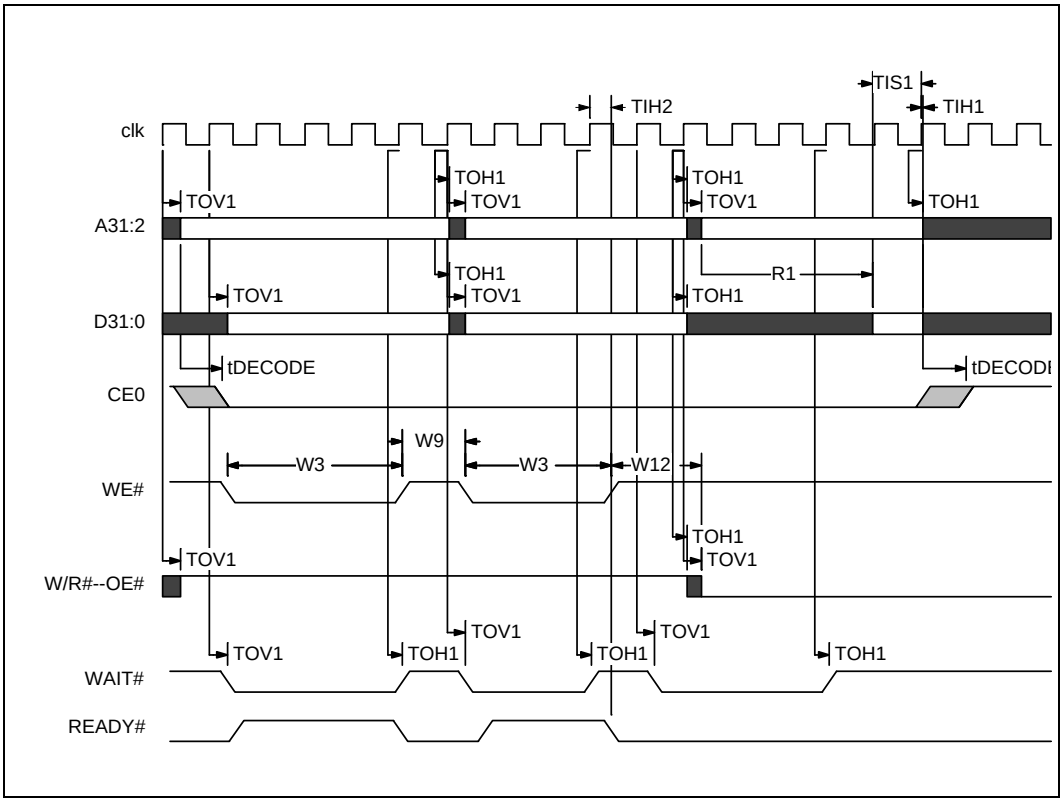


Figure 27. 3 Volt Intel® StrataFlash™ Memory/i960® H Processor Write Cycles Followed by Read

Figure 26 is a timing diagram of four reads. Burst mode is enabled on the i960 H CPU so that all four addresses in the page can be read in the minimum amount of time. The initial read must be at a page boundary for the timing in this figure. If not all accesses are within a page boundary, additional wait-states must be added for the first access in another page.

Figure 27 shows two writes followed by a single read. Either WE# or chip enable may be used to start a write. In this case, WE# is used to latch the address and data. It is generated from WAIT# and W/R# in the PLD. The i960 H processor generates a maximum of three wait-states for sequential writes, so READY# is only needed to add one additional wait-state after WAIT# goes high for the second and subsequent write accesses to the 3 Volt Intel StrataFlash memory.

Several considerations must be taken into account when resetting. If a block erase, program, or lock-bit configuration command is executing, RP# must be held low for a minimum of time of t_{PLPH} (35 µs). When returning from reset, the i960 H processor takes 23 to 67 CLKIN cycles until the first bus activity. At 40 MHz, 23 clock cycles is 575 ns. This is greater than the min. time required from RP# high to output delay (310 ns = t_{PHQV} + t_{PHRH}) on the 3 Volt Intel StrataFlash memory device. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

Certain areas of the i960 H processor's memory map may not be used by flash memory. These include 00000000h to 000007FFh and FF000000 to FFFFFFFFh which is used for accesses internal to the processor such as registers. Most other areas can be configured for use by the 3 Volt Intel StrataFlash memory.

Read all appropriate datasheets before attempting this interface (see Appendix A for a list of additional information).

3.8. Interfacing 3 Volt Intel® StrataFlash™ Memory to Hitachi SH7708 (SH-3) at 60 MHz

The SH7708 (SH-3) series of 32-bit RISC microprocessors include an 8-Kbyte cache and an on-chip Bus State Controller including a wait-state generator that allows for a near glueless interface to the 3 Volt Intel StrataFlash memory.

3.8.1. INTERFACE CONSIDERATIONS

This sample interface uses one 3 Volt Intel StrataFlash memory in 16-bit mode. Timing diagrams were made with the 32-Mbit 3 Volt Intel StrataFlash memory and a 60 MHz bus. This interface requires two inverters, two OR gates, an AND gate, and six flip-flops. These may be integrated into an ASIC or a PLD. All parts can run from and interface at 3.0 V–3.6 V. The bus width settings on the SH-3 for the area the 3 Volt Intel StrataFlash memory occupies should be 16 bits.

3.8.2. PROCESSOR INTERFACE SIGNALS

The interface uses the following signals provided by the SH7708:

A_{25-0}: The address bus signals the memory which piece of information is to be accessed.

D_{31-0}: The 32-bit data bus. The 3 Volt Intel StrataFlash memory is connected to D_{31}–D_0.

CSn#: The Chip Select signal generated by the SH-3 for the memory region the 3 Volt Intel StrataFlash memory is placed in.

RD/WR#: Read/Write indicates the direction of the current data transfer.

WEn#: A Write Enable signal is generated for each 8-bit portion of the bus.

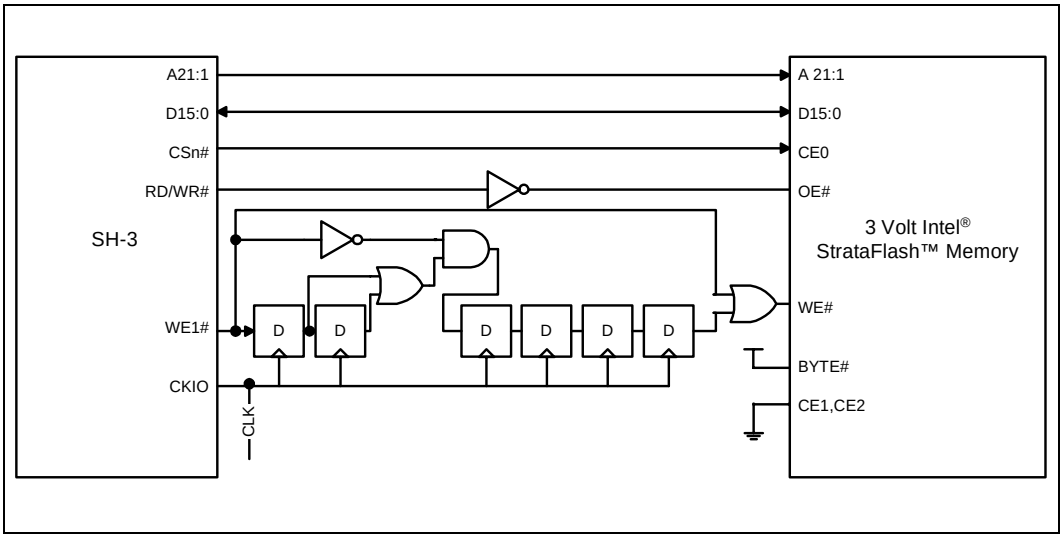


Figure 28. 3 Volt Intel® StrataFlash™ Memory/SH-3 Interface

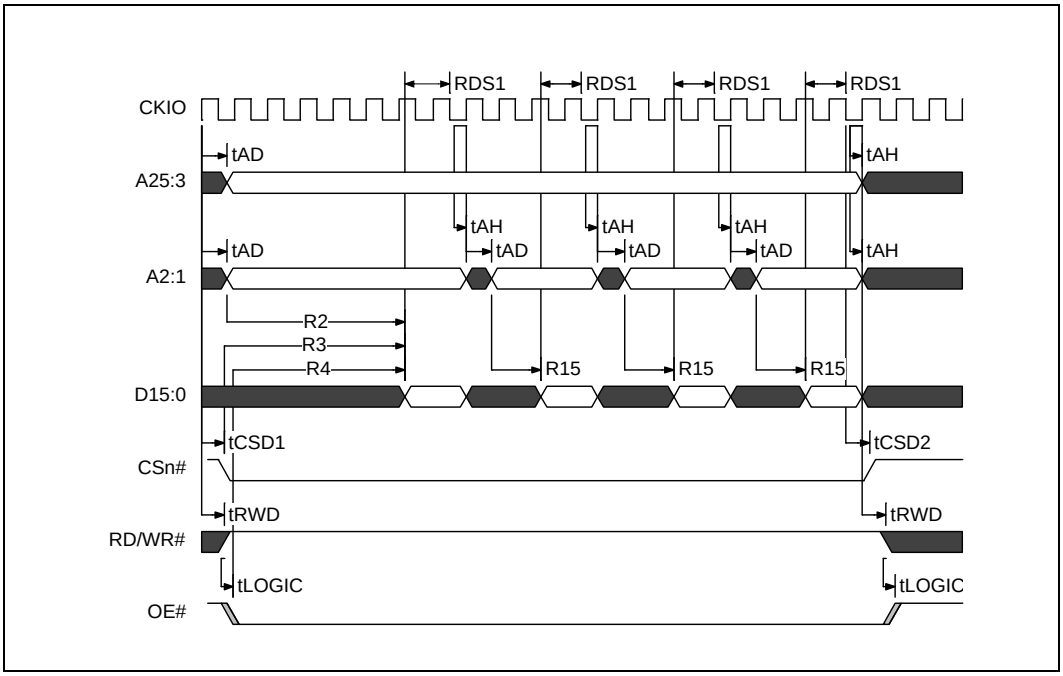


Figure 29. 3 Volt Intel® StrataFlash™ Memory/SH-3 Page-Mode Reads

3.8.3. CONTROL SIGNAL GENERATION

The only 3 Volt Intel StrataFlash memory signals not directly to the SH-3 connected are OE# and WE#. RD/WR# is inverted to generate OE#. The logic between WE1# on the SH-3 and WE# on the 3 Volt Intel StrataFlash memory is meant to allow WE# to go low on the 3 Volt Intel StrataFlash memory at nearly the same time as WE1# goes low, but making it go high earlier so WE# pulse high times can be met. Figure 28 is a block diagram of the interface.

The SH-3 can internally generate wait-states based on register settings. Figure 29 is a timing diagram of a four-word read with page-mode enabled. This diagram assumes the wait-states have been configured by setting the appropriate registers.

Figure 30 is a timing diagram of two write cycles followed by a read cycle. Note that the 3 Volt Intel StrataFlash memory's WE# signal goes high earlier than the WE1# signal from the SH-3. This signal is generated to meet WE# pulse high and write recovery before read timing requirements. The six flipflops allow the signal to be low long enough to meet WE# pulse low time before going high again.

Several considerations must be taken into account when resetting the 3 Volt Intel StrataFlash memory. If a block erase, program, or lock-bit configuration command is executing, RP# must be held low for a minimum of time of t_{PLPH} (35 µs). When returning from reset, the 3 Volt Intel StrataFlash memory the RP# high to output delay (310 ns = t_{PHQV} + t_{PHRH}) must be met. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

The 3 Volt Intel StrataFlash memory may only be mapped to certain areas of the processor's memory. Certain areas may not be used for flash or other static memories. If the 3 Volt Intel StrataFlash memory is to be used as the booting memory, it should be placed in area 0 and located so that it can be accessed by the initial Program Counter value of A000000h. A complete address map of the SH7708 processor is available in the user's manual for that processor.

Read all appropriate documentation before attempting this interface.

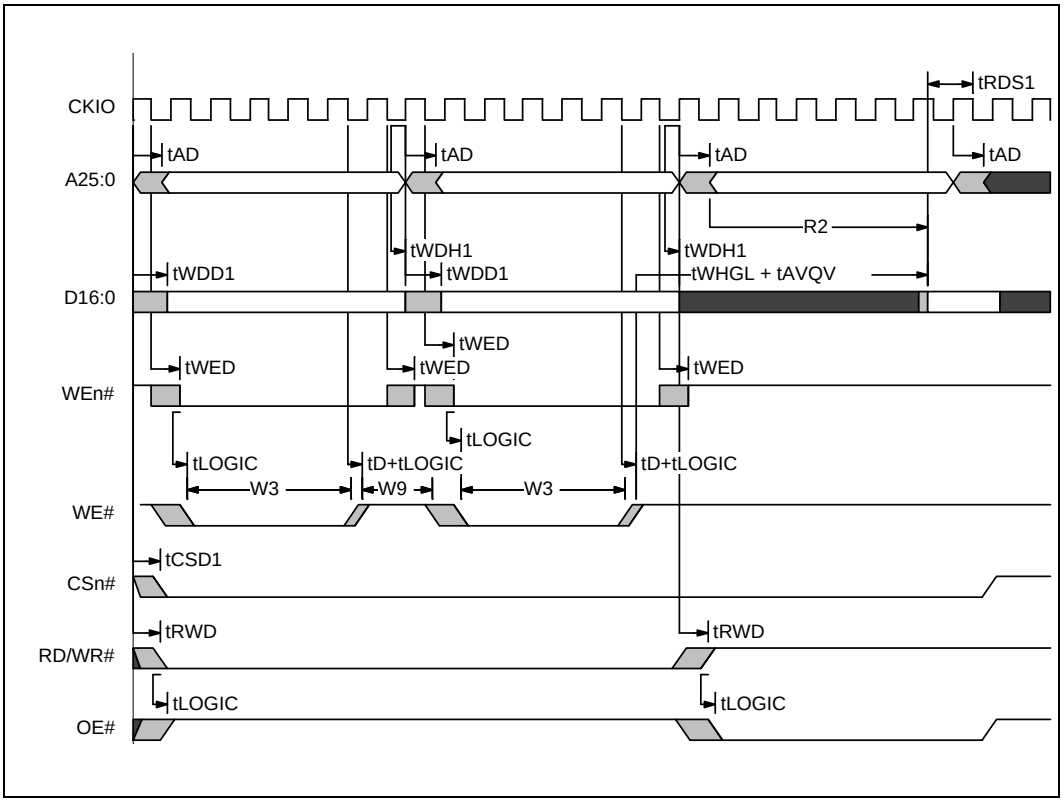


Figure 30. 3 Volt Intel® StrataFlash™ Memory/SH-3 Write Cycles followed by a Read

3.9. Interfacing the 3 Volt Intel® StrataFlash™ Memory to SH7750 (SH-4) at 66 MHz

The SH7750 (SH-4) embedded microprocessor produced by Hitachi employs a 32-bit RISC architecture which features object code upward-compatible with the SH-1, SH-2, and SH-3 microprocessors. The SH-4 uses a 16-bit fixed-length instruction set, which enables program code size to be reduced by about 50%. Figure 31 illustrates the block diagram of the 3 Volt Intel StrataFlash memory interfaces to the SH7750.

The SH7750 allows the designer to choose the bus clock that 1/3 of the main clock (200 MHz).

3.9.1. INTERFACE CONSIDERATIONS

This sample interface uses two 3 Volt Intel StrataFlash memory in 16-bit mode. Timing diagrams were made with the 128-Mbit 3 Volt Intel StrataFlash memory with the memory bus running at 66 MHz. There is no other required logic between the processor and the 3 Volt Intel StrataFlash memory. The bus width setting of the processor should be set at area 0, 5 or 6 for high speed read access. A pull-down resistor is required in this interface to control the Ready (RDY#) pin of the CPU. RDY# needs to be pulled low by CE# during flash accesses to indicate the use of the CPU's internal programmable wait-states.

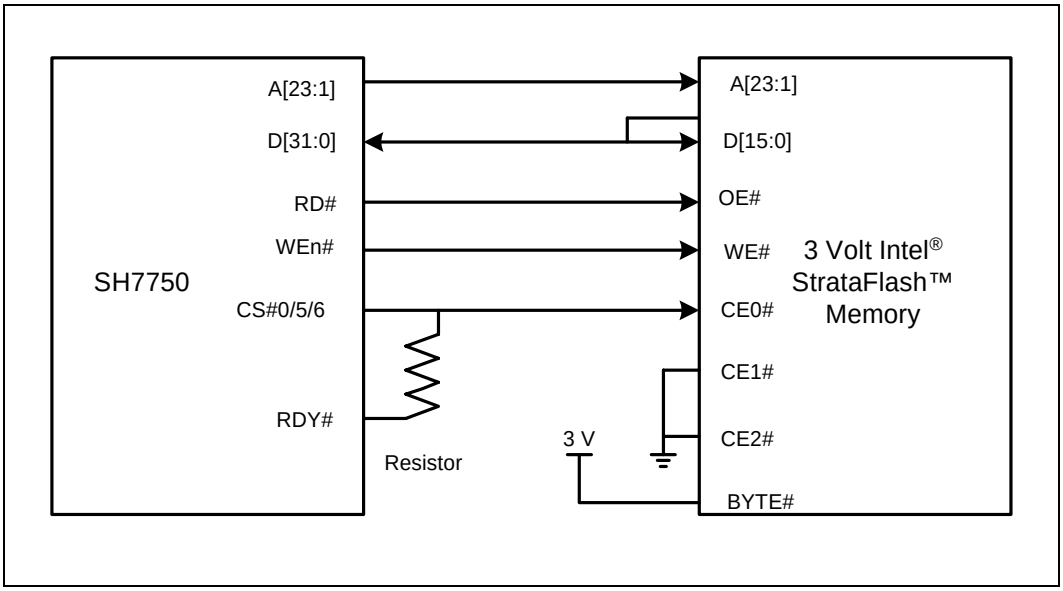


Figure 31. 3 Volt Intel® StrataFlash™ Memory/SH7750 Microprocessor Interface

This reference interface in this document uses page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set to b'1 to enable the page-mode.

3.9.2. PROCESSOR INTERFACE SIGNALS

The sample reference uses the following main signals provided by the SH7750:

$A_{23:0}$: The address bus signals the memory which piece of information is to be accessed.

$D_{31:0}$: The data bus contains bi-directional data paths to transfer data between the processor and the flash memory.

CSn#: The Chip Select signal indicates which memory bank the processor is accessing.

RD#/WEn#: Read/Write indicates the direction of the current data transfer.

RDY#: The Ready pin is driven by external devices to insert external wait-states.

3.9.3. CONTROL SIGNAL GENERATION

Figure 32 shows a four-word page-mode read timing diagram. The wait-states are generated internally by programming the CPU's Wait Control Registers (WCR). These registers should be set to 9 for the first page-mode read cycle to insert wait-states. The subsequence Burst Pitch is 1 wait-state. If the designer selects area 6, bits 31:29 of the WCR2 should be set to b'101. If the designer selects area 5, bits 25:23 should be set to b'101. Similarly, bits 5:3 should be set to b'101 for the area 0.

Figure 33 shows a write timing diagram. The designer needs to have four wait-states inserted. A pull-down register is connected between CSn# and RDY# to pull RDY# low during flash accesses and to allow other devices to drive RDY# low during flash accesses and to allow other devices to drive RDY# during other memory accesses. The specific value of the resistor will depend on the specific system design.

In the Bus Control Register 1 (BCR1), bits 13:11 should be set b'001 for the 4 consecutive accesses if the designer selects the area 0. The bits 10:8 of the BCR1 should be set to b'001 if the designer selects area 5. Similarly, bits 7:5 should be set b'001 to enable area 6.
In register BCR2, if the designer selects area 5, bit 11 (bit: 2n+1 = 2*5+1 = 11) should be set to b'1 and bit 10

(2*n = 2*5 = 10) should be set to b'1. If the designer selects area 6, bit 13 (2*n+1 = 2*6+1 = 13) should be set b'1 and bit 12 (2*n = 2*6 = 12) should be set to b'1.

The following signal can be found in the Hitachi *SH-4 Hardware Manual*: t_{AD}, t_{CSD}, t_{RSD}, t_{WED1}, t_{RDS}, t_{RDH}.

The following signal can be located in the *3 Volt Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 28F320J3A* datasheet: R2, R3, R15.

Read all appropriate documentation before attempting this interface.

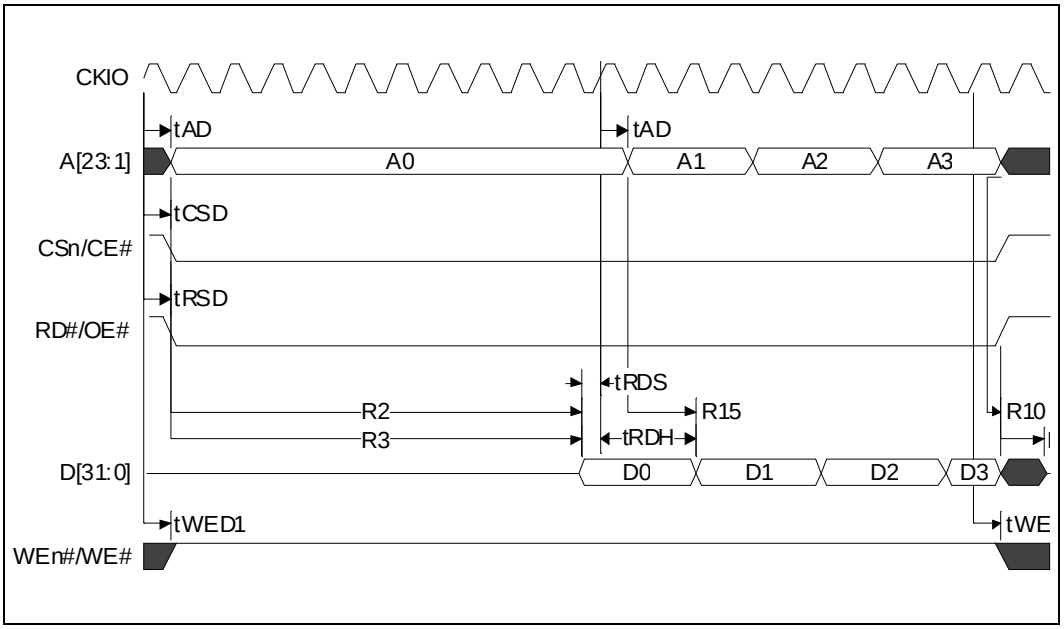


Figure 32. 3 Volt Intel® StrataFlash™ Memory/SH7750 Four Word Page-Mode Read Cycle at 66 MHz

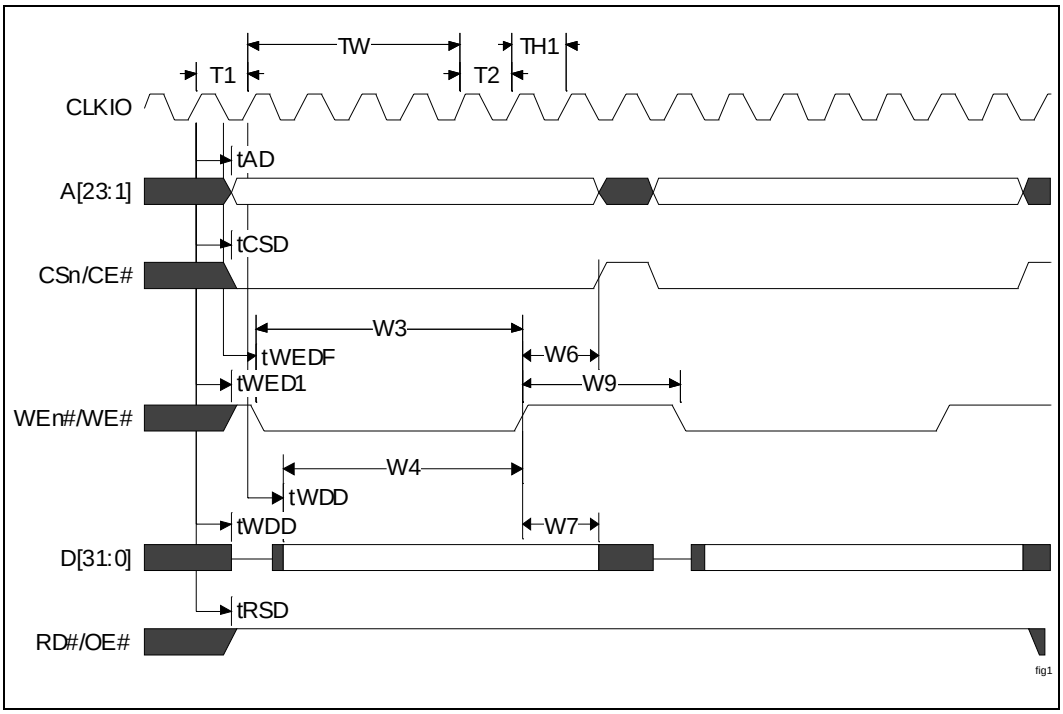


Figure 33. 3 Volt Intel® StrataFlash™ Memory/SH7750 Write Cycle at 66 MHz

3.10. Interfacing 3 Volt Intel® StrataFlash™ to MIPS PR31700 Poseidon Processor by Philips

The Poseidon processor by Philips is based on a MIPS R3000 core. The PR31700 core runs at a speed of 74 MHz, and is pin to pin compatible to the PR31500. The Poseidon Processor includes such features as 4 KB of instruction cache, 1 KB of data cache, and a built-in memory controller.

3.10.1. INTERFACE CONSIDERATIONS

The Philips PR31700 processor and the 3 Volt Intel StrataFlash memory can interface with only an address latch. The Philips PR31700 processor can be programmed to generate wait-states, eliminating the need for external wait-state logic. It also internally decodes the address bus to generate chip select signals, which can be directly connected to the 3 Volt Intel StrataFlash memory's chip enable signal. Both the processor and the flash can be powered from and interface at 3.3 V. Figure 34 is a block diagram of the interface.

3.10.2. PROCESSOR INTERFACE SIGNALS

This interface uses the following signals provided by the Toshiba TMPR3904F processor:

A12:0: The multiplexed address bus provides addresses to memory. It must be latched to generate the full address.

D15:0: The upper half of the 32-bit data bus. This is the portion used for connections to 16-bit memory.

ALE: Address Latch Enable is used as the latch control to generate the upper address bits.

(M)CSx#: CSx# and MCSx# are chip select signals generated by the Philips PR31700 processor.

WE#: Indicates writes from the processor to the system.

RD#: Indicates reads from the processor to the system.

Documentation on the Poseidon processor indicate active low signals with a "/" or a "*." For consistency within this document, the active low signals from the Poseidon processor are indicated with a "#" symbol.

3.10.3. CONTROLLING THE INTERFACE

The memory configuration registers in the Poseidon processor should be set as necessary for proper operation. This includes setting the bus width, the access time for the flash, and enabling page-mode for the memory region containing the 3 Volt Intel StrataFlash memory. Page-mode should be enabled on the 3 Volt Intel StrataFlash memory before it is enabled on the Poseidon Processor so that invalid data is not read.

The Poseidon processor and the 3 Volt Intel StrataFlash memory both use a four word page. During bursts, the Poseidon processor always makes consecutive accesses starting on a 16-byte boundary. This means that the Poseidon processor will not cross a page boundary on the 3 Volt Intel StrataFlash memory without inserting necessary wait-states.

NOTE:

The PR31700 processor datasheet does not give abbreviated names for timing specifications. Table 4 shows the symbols used in Figure 35 and Figure 36 and their description from the datasheet.

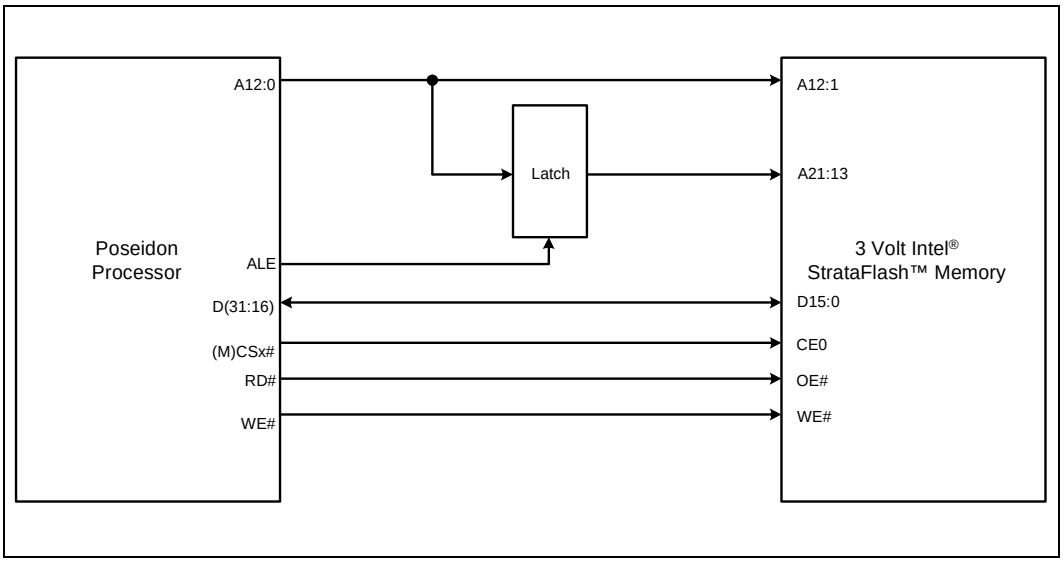


Figure 34. 0.25 µm 3 Volt Intel® StrataFlash™ Memory/Poseidon Interface

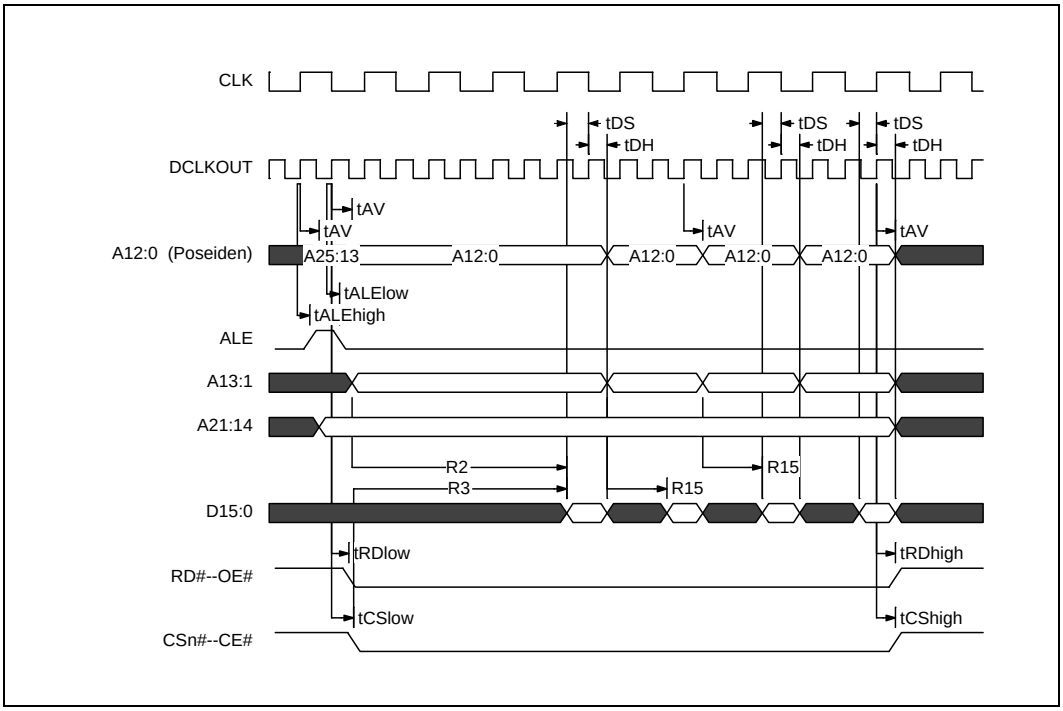


Figure 35. 3 Volt Intel® StrataFlash™ Memory/Poseidon Processor Page-Mode Reads

Table 4. Poseidon Processor Bus Timing Names

Symbol	Description
t_{AV}	Delay DCLKOUT to A[12:0]
t_{DS}	D[31:16] to DCLKIN Setup time
t_{DH}	D[31:16] to DCLKIN Hold time
t_{ALE}low	Delay DCLKOUT to ALE (Rising)
t_{ALE}high	Delay DCLKOUT to ALE (falling)
t_{RD}low	Delay DCLKOUT to RD# (falling)
t_{RD}high	Delay DCLKOUT to RD# (rising)
t_{CS}low	Delay DCLKOUT to CS3-0# (falling)
t_{CS}high	Delay DCLKOUT to CS3-0# (rising)
t_{DV}	Delay DCLKOUT to D[31:16]
t_{WE}low	Delay DCLKOUT to WE# (falling)
t_{WE}high	Delay DCLKOUT to WE# (rising)

Figure 35 is a timing diagram of the 3 Volt Intel StrataFlash memory and the Poseidon processor with page-mode reads. DCLKOUT runs at 73.728 MHz, and is what all timing specifications from the PR31700 processor are given off of. The number of wait-states to be used is counted as one less than the number of CLK cycles that an access takes. The diagram shows ALE pulsing high so that the upper addresses can be latched. After the upper addresses are latched and $A_{12:0}$ become valid, the time t_{AVQV} must pass before data is valid. For the second, third and fourth accesses, the time t_{APA} passes before data from the 3 Volt Intel StrataFlash memory is valid.

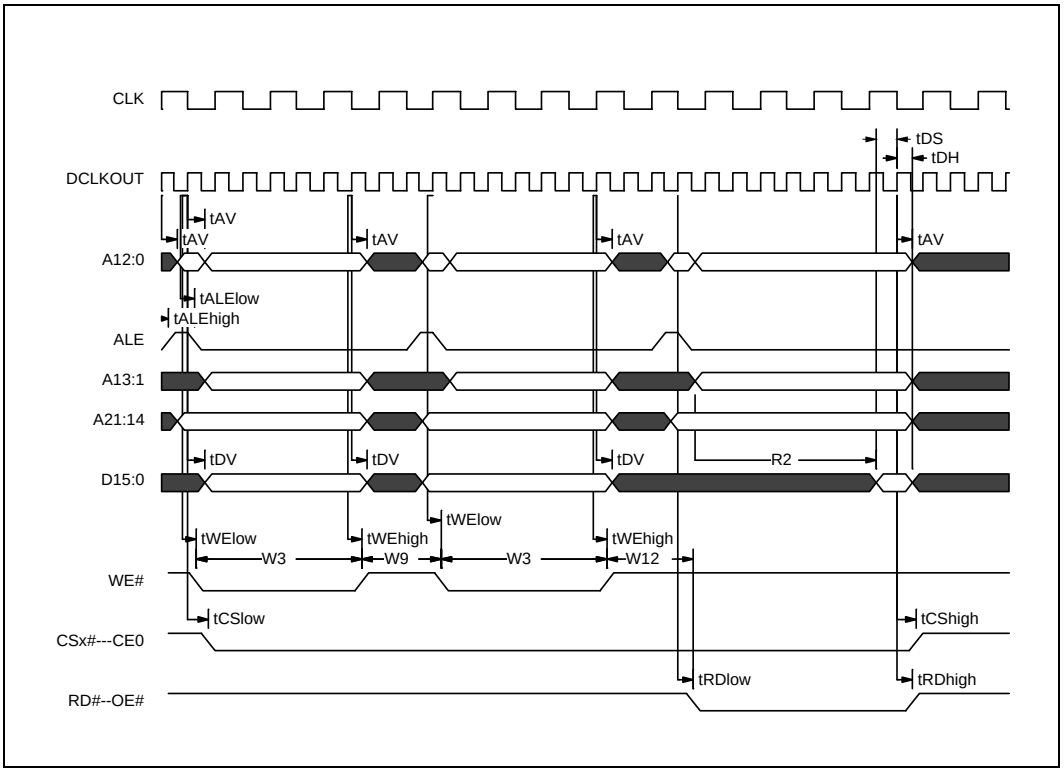


Figure 36. 3 Volt Intel® StrataFlash™ Memory/Poseidon Write Cycles Followed by Read

NOTE:

The PR31700 processor datasheet does not give abbreviated names for timing specifications. Table 4 shows the symbols used in Figure 35 and Figure 36 and their description from the datasheet.

Figure 36 is a timing diagram of two writes followed by a read. WE# is held low long enough to meet the Write Pulse Width time (t_{WP}). When it goes high, the address and data is latched. In between write cycles, WE# must remain high for at least t_{WPH}. This is the reason a clock cycle is left between the writes. For a similar reason, a clock cycle is left between the read and the write. This is to meet the write recovery before read time, t_{WHGL}.

Several considerations must be taken into account when resetting or powering on the 3 Volt Intel StrataFlash memory. When resetting, RP# must remain low for at least a time of t_{PLPH} (35 µs). In addition, the first output is not valid until 310ns (t_{PHQV} + t_{PHRH}) after RP# goes high. The PR31700 processor has many power management features, and depending on how these are used with the 3 Volt Intel StrataFlash memory, t_{PLPH} (35 µs) and t_{PHQV} + t_{PHRH} (310 ns) may need to be taken into consideration. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

The 3 Volt Intel StrataFlash memory can only be used in certain regions of the Poseidon processor's memory map. Regions designated for memory not compatible with flash should not be used to interface with the 3 Volt Intel StrataFlash memory. A memory map of is available in Poseidon processor user's manual. If it is desirable to boot from the 3 Volt Intel StrataFlash memory, then it should be placed in the CS0 region, which is designated for boot ROM. It is mapped starting at address 11000000h in kernel space, while the boot vector location is mapped at address 1FC00000h.

Consult all appropriate datasheets and manuals before attempting this interface (see Appendix A for a list of additional information).

4.0. SUMMARY

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. Interfaces between 3 Volt Intel StrataFlash components and various processors can generally be accomplished with a PLD to generate wait-states and WE#, and a decoder to generate chip enable signals. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. It is an excellent option for code and data applications where high density and low cost are required.

APPENDIX A
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
290667	*3 Volt Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 28F320J3A*
210830	*Flash Memory Databook*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#*
278088	*SA-1100 Microprocessor Technical Reference Manual*
278240	*SA-1110 Microprocessor Technical Reference Manual*
Note 4	Hitachi *SH-4 Hardware Manual, v1.1*

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.
4. This manual can be located at the following URL: http://semiconductor.hitachi.com/products/h_micon/1_sh/4_sh4/H14TH002D2/pdf/h1402.pdf