Integrated Device Technology, Inc.

IDT79RV4700 SyncOut to SyncIn Design Considerations

TECHNICAL NOTE TN-29

By Salahuddin Ameer

Introduction

The purpose of this technical note is to provide important data to board designers using the IDT79RV4700 processor. The information presented here will assist a designer using the processor's **SyncOut** and **SyncIn** signals to minimize the skew between I/O signals and clocks and ensure the proper functioning of the on-chip PLL in their design.

IDT79R4700 PLL Clock Interface Signals

The Clock interface uses two input signals: **MasterClock** and **SyncIn** and four output signals: **MasterOut**, **SyncOut**, **Rclock(1:0)**[1], and **Tclock(1:0)**[2].

All processor timings are based on the single **MasterClock** input signal. By multiplying **MasterClock** two times, the processor generates the pipeline clock, **Pclock**. To generate **Sclock**[3]**,** which determines the processor's bus frequency, **Pclock** is divided by the number (2 through 8) that is programmed during the boot-mode initialization sequence. The processor drives both **Rclock** and **Tclock**.

The **Tclock** and **Rclock** signals are identical to **Sclock** in frequency. In phase, however, **Rclock** leads by 25% of **Sclock**'s cycle time. Two interface signals, **SyncIn** and **SyncOut** (refer to Chapter 10 of the *IDT79RV4700 Hardware User's Manual,* for more details and timing diagrams***)***, provide a delay between **Tclock** and **Rclock** and the I/O signals (SysAd, SysCmd and Control signals), to compensate for buffer and board external clock delays.

The Need for Compensation

Buffers add delays to **Tclock** and **Rclock** and are required to increase the fanout of these signals. To compensate for these delays, a delay must also be added between **SyncOut** and **SyncIn**. Buffer placement for these signals is illustrated in Figure 1.

How much delay time between SyncOut and SyncIn is required?

When determining delay time requirements, the following four conditions should be taken into account:

1. The same delay of the clock buffers D.

2. The delay should not exceed one MasterClock period of 2ns, which is used to accommodate any mismatch in the internal buffer delays between MasterClock and SyncIn.

3. The SyncIn signal must be clean and jitter free to ensure the proper working of the PLL.

4. The rise and fall time of the SyncIn signal must match that of **MasterClock**. Otherwise, a delta time phase shift could occur between MasterClock and SyncIn at 1.5V level (trigger point of the R4700 input buffer). The result is Tclock will appear delta time earlier than it should.

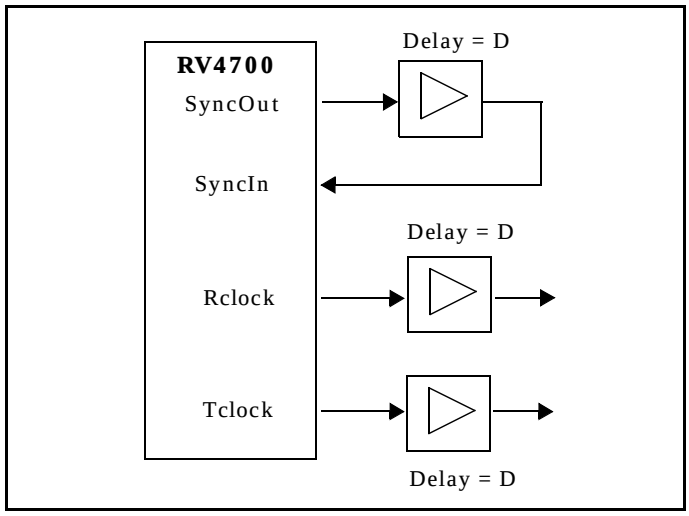

Figure 1. Illustration of Delays between RV4700 Processor Signals

Are there other precautions?

Besides the **SyncOut** and **SyncIn** delay issue, careful attention to other signals must also be given when connecting loads. It is important to try and not exceed two loads, to allow maximum design margin.

Conclusion

Through this technical note, details regarding the relationship between the PLL clocks and synchronization with the external interface circuitry, using **SyncOut** and **SyncIn,** have been presented. This data will assist board designers who are using the R4700's **SyncOut** and **SyncIn** signals to minimize the skew between I/O signals and clocks and ensure the proper functioning of the on-chip PLL in their designs.

More details on the IDT79RV4700 processor can be obtained in both the *IDT79RV4700 Hardware User's Manual* and in the IDT79R4700/IDT79RV4700 64-Bit RISC Microprocessor data sheet.

1. Two identical receive clocks that are at the interface frequency.

2. Two identical transmit clocks that are at the interface frequency.

3. An internal clock used by the processor to sample data at the system interface and to clock data into the processor system interface output registers.