PRELIMINARY INFORMATION

# ICS387
# Quad PLL Quick Turn Clock Synthesizer

## Description

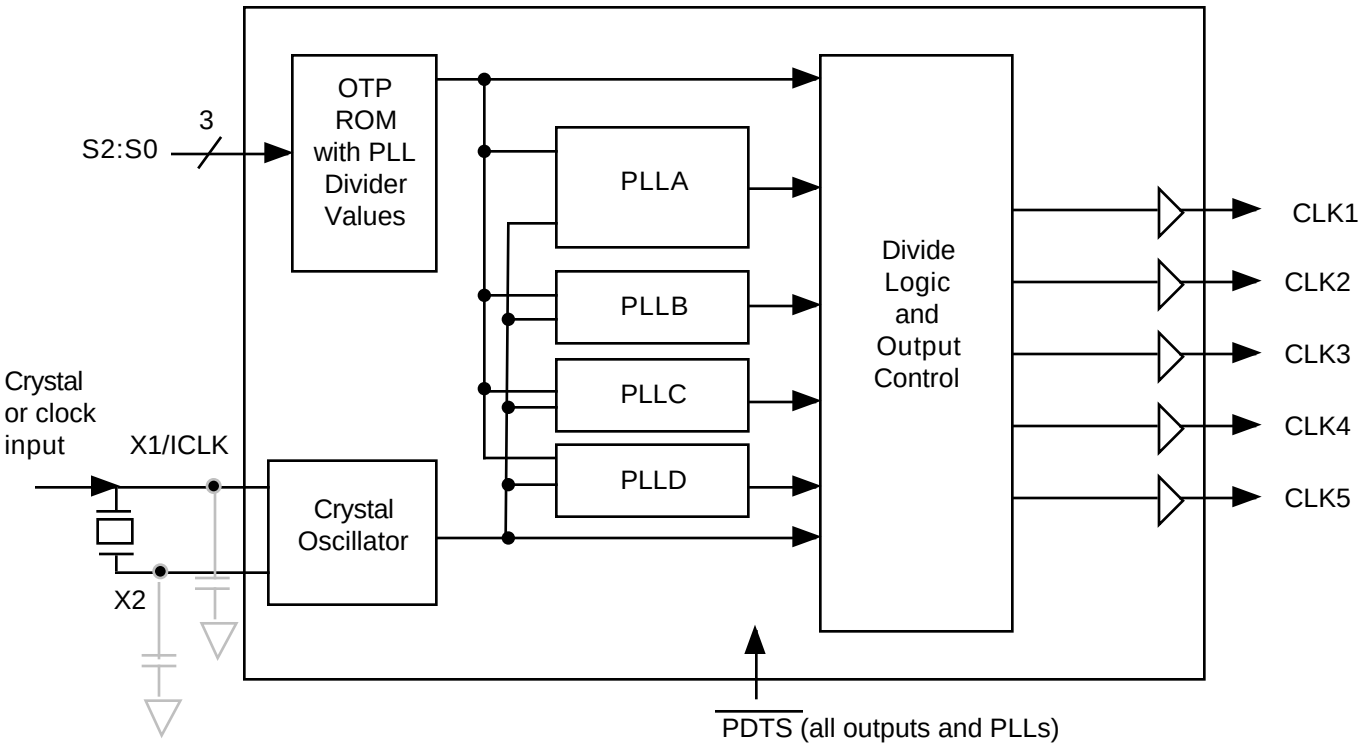
The ICS387 QTClock™ generates up to 5 high quality, high frequency clock outputs including a reference from a low frequency crystal or clock input. It is designed to replace crystals and crystal oscillators in most electronic systems. The ICS387 contains a One Time Programmable (OTP) ROM which is factory programmed with PLL divider values to output a broad range of frequencies up to 200 MHz, allowing customer requests for different frequencies to be shipped in 1-3 days. Programming features include a selectable frequency table and up to 2 low-skew outputs.

Using Phase-Locked-Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving board space and cost.

## Features

- Packaged as 16 pin TSSOP
- Quick turn frequency programming allows samples as quickly as one day
- Up to 2 outputs can be low-skew
- Can include 8 selectable output frequencies
- Up to 3 reference outputs
- Replaces multiple crystals and oscillators
- Output frequencies up to 200 MHz at 3.3V
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Duty cycle of 45/55
- Operating voltages of 3.3 V or 5 V
- Advanced, low power CMOS process

## Block Diagram




Capacitors are required with a crystal input.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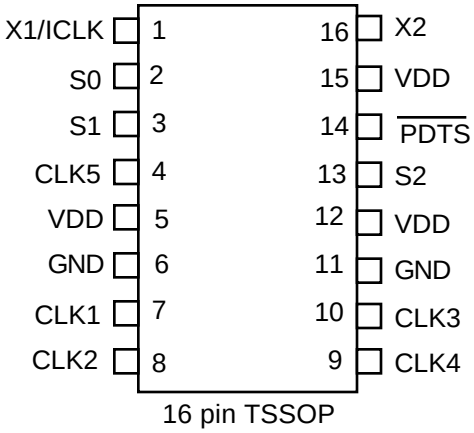
## Pin Assignments



16 pin TSSOP

## Pin Descriptions

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | X1/ICLK | XI | Crystal connection. Connect to fundamental mode crystal or clock input. |
| 2 | S0 | I | Select pin 0 for frequency table/chip control. Internal pull-up resistor. |
| 3 | S1 | I | Select pin 1 for frequency table/chip control. Internal pull-up resistor. |
| 4 | CLK5 | O | Clock output. |
| 5 | VDD | P | Connect to +3.3V or +5V. Must be same voltage as pins 12 and 15. |
| 6 | GND | P | Connect to ground. |
| 7 | CLK1 | O | Clock output. |
| 8 | CLK2 | O | Clock output. |
| 9 | CLK4 | O | Clock output. |
| 10 | CLK3 | O | Clock output. |
| 11 | GND | P | Connect to ground. |
| 12 | VDD | P | Connect to +3.3V or +5V. Must be same voltage as pins 5 and 15. |
| 13 | S2 | I | Select pin 2 for frequency table/chip control. Internal pull-up resistor. |
| 14 | $\overline{\text{PDTS}}$ | I | All-chip Power Down when low. Note 1. |
| 15 | VDD | P | Connect to +3.3V or +5V. Must be same voltage as pins 5 and 12. |
| 16 | X2 | XO | Crystal connection. Leave unconnected for clock input. |

Key: XI, XO = crystal connections, I = input, O = output, P = power supply connection

Note 1: All outputs are internally high impedance with a weak internal pull-down resistor. When $\overline{\text{PDTS}}$ is active, it is possible to overdrive the output pins for board-level testing.

## Device Configuration

The ICS387 QTClock provides the facility for up to 5 clock outputs. The outputs are derived from either the reference input or from one of the 4 PLLs. All chip functions are controlled from an OTP ROM which has 3 input control lines (S2, S1, S0), giving a total of 8 address locations. Each address location gives control of the following:

1) Each output can be turned off individually
2) The internal dividers for each PLL are controlled to generate any required frequency.
3) Each PLL can be turned off (powered down) individually.
4) The output divide and control logic can be configured to bring the appropriate clock to the correct pin.
5) Up to four low skew copies of the same clock can be enabled.

This chip architecture provides the user with unrivaled flexibility. For example, one of the input pins could be used to control the power of the chip by shutting down PLLs and outputs when not used. The second and third could be used to change the output clock frequencies.

The specification is complete when the ICS387 QTClock Order Form accompanies this data sheet. The order form lists the input  and CLK actual frequencies, as well as any other available options. This unique configuration is given a two character alphanumeric programming code (ICS387-xx), which must be specified when referring to samples or ordering parts.

## Frequency Select Table

The ICS387 can be configured so that one PLL provides up to 8 frequency selections.  For example, CPU frequencies of 66.7 MHz, 100.0 MHz, 133.3 MHz, and 166.7 MHz could be included.  This information should be indicated on the Order Form when the ICS387 is initially defined.

### External Components / Crystal Selection

The ICS387 requires a 0.01µF decoupling capacitor to be connected between VDD and GND on pins 5 and 6, and another between pins 12 and 11. These must be connected close to the ICS387 to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω series terminating resistor can be used next to each CLK pin. For a crystal input, a parallel resonant, fundamental mode crystal should be used. Crystal capacitors must be connected from each of the pins X1 and X2 to Ground.  The value (in pF) of these crystal caps should equal ($C_L$-6pf)*2, where $C_L$ is the crystal load capacitance in pF. As an example, for a crystal with 16 pF load capacitance, each crystal capacitor would be 20 pF [(16 - 6pf)*2 = 20].

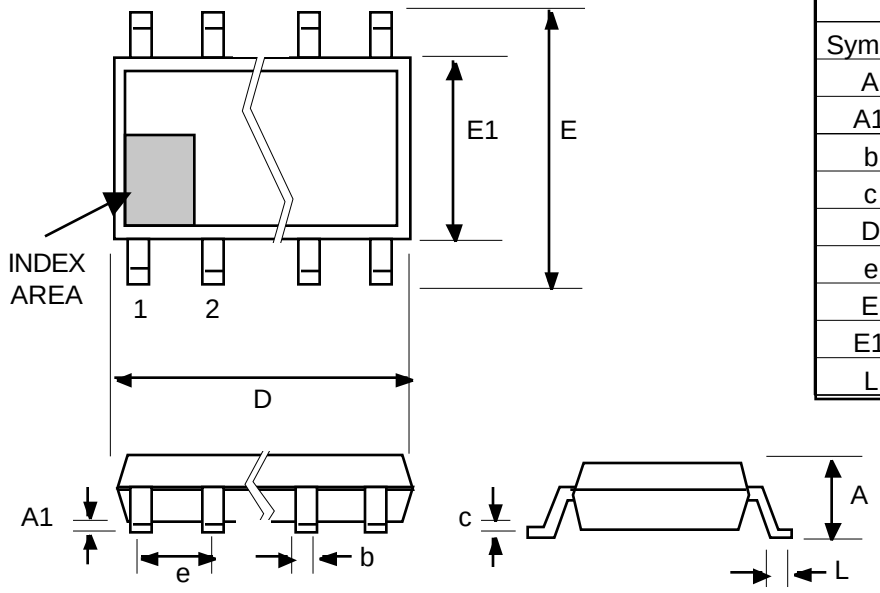
For a clock input, connect to X1/ICLK and leave X2 unconnected (no capacitors on either X1 or X2).

## Electrical Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| **ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)** | | | | | |
| Supply Voltage, VDD | Referenced to GND | | | 7 | V |
| Inputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Clock Output | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Ambient Operating Temperature | Commercial version | 0 | | 70 | ºC |
| Ambient Operating Temperature | Industrial version | -40 | | 85 | ºC |
| Soldering Temperature | Max of 10 seconds | | | 260 | ºC |
| Storage temperature | | -65 | | 150 | ºC |
| **DC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)** | | | | | |
| Operating Voltage, VDD | | 3.13 | | 5.5 | V |
| Input High Voltage, VIH, ICLK only | ICLK (Pin 1) | (VDD/2)+1 | | | V |
| Input Low Voltage, VIL, ICLK only | ICLK (Pin 1) | | | (VDD/2)-1 | V |
| Input High Voltage, VIH | $\overline{\text{PDTS}}$, S0, S1, S2 | 2 | | | V |
| Input Low Voltage, VIL | $\overline{\text{PDTS}}$, S0, S1, S2 | | | 0.8 | V |
| Output High Voltage, VOH | IOH=-4mA | VDD-0.4 | | | V |
| Output High Voltage, VOH | IOH=-25mA | 2.4 | | | V |
| Output Low Voltage, VOL | IOL=25mA | | | 0.4 | V |
| IDD Operating Supply Current, 20 MHz crysta | No Load, 100MHz | | 20 | | mA |
| Short Circuit Current | CLK output | | ±70 | | mA |
| On-Chip Pull-up Resistor, inputs | | | TBD | | kΩ |
| On-Chip Pull-down Resistor, outputs | | | TBD | | Ω |
| Input Capacitance, inputs | | | 4 | | pF |
| **AC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)** | | | | | |
| Input Frequency, crystal input | | 5 | | 27 | MHz |
| Input Frequency, clock input | | 2 | | 50 | MHz |
| Output Frequency | | 2 | | 200 | MHz |
| Output Clock Rise Time | 0.8 to 2.0V | | 1 | | ns |
| Output Clock Fall Time | 2.0 to 0.8V | | 1 | | ns |
| Output Clock Duty Cycle (Note 1) | at VDD/2 | 45 | 49 to 51 | 55 | % |
| Absolute Clock Period Jitter | Deviation from mean | | ±TBD | | ps |
| One Sigma Clock Period Jitter | | | TBD | | ps |
| Pin to Pin Skew | Low skew outputs | -250 | | 250 | ps |
| Power-up time, $\overline{\text{PDTS}}$ goes high until CLK out | | | 8 | 20 | ms |

Note 1: These are typical values. The actual minimum and maximum duty cycle limits are shown on the ICS387 QTClock Order Form for each programmed version.

**Package Outline and Package Dimensions**
**(For current dimensional specifications, see JEDEC Publication No. 95.)**




**16 pin TSSOP**

| | Inches | | Millimeters | |
|---|---|---|---|---|
| Symbol | Min | Max | Min | Max |
| A | -- | 0.047 | -- | 1.20 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| b | 0.007 | 0.012 | 0.19 | 0.30 |
| c | 0.0035 | 0.008 | 0.09 | 0.20 |
| D | 0.193 | 0.201 | 4.90 | 5.10 |
| e | .0256 BSC | | 0.65 BSC | |
| E | .252 BSC | | 6.40 BSC | |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 |
| L | 0.018 | 0.030 | 0.45 | 0.75 |

## Ordering Information

| Part/Order Number | Marking | Package | Shipping | Temperature |
|---|---|---|---|---|
| ICS387G-xx | ICS387G-xx | 16 pin TSSOP | Tubes | 0 to 70 °C |
| ICS387G-xxT | ICS387G-xx | 16 pin TSSOP | Tape and Reel | 0 to 70 °C |
| ICS387G-xxI | ICS387G-xxI | 16 pin TSSOP | Tubes | -40 to 85 °C |
| ICS387G-xxIT | ICS387G-xxI | 16 pin TSSOP | Tape and Reel | -40 to 85 °C |

xx represents a 2 character alphanumeric programming code assigned by the factory, which indicates the output frequencies on all CLKs and other features. All samples are shipped with an ICS387 order form describing the characteristics of the device.