Evaluating the IBM43RF0100 SiGe Low Noise Transistor

Introduction

The IBM43RF0100 SiGe High Dynamic Range Low Noise Transistor is a silicon-germanium (SiGe) NPN transistor designed for high performance, low cost applications.

IBM's SiGe manufacturing and packaging techniques result in a transistor with high gain, low noise, exceptional linearity, and low power consumption in a miniature surface mount package. These characteristics make the IBM43RF0100 ideal for applications such as LNAs, VCOs, and driver amplifiers in pagers, portable telephones, spread spectrum transceivers, and other RF devices.

This application note describes how to use the IBM43RF0100EV Evaluation Boards to evaluate the performance characteristics of the IBM43RF0100 SiGe transistor.

Performance Evaluation

The evaluation boards measure IBM43RF0100 transistor characteristics such as noise, power, distortion, and s-parameters under a variety of operating conditions.

Transistor performance is evaluated using an IBM43RF0100 configured as a single-stage RF amplifier. The amplifier is designed for operation at 1.9 GHz, with a nominal gain of 12dB and a noise figure of 1.5dB at V_{CC} = +3.0 Vdc.

The RF amplifier and associated components are available in two different evaluation board configurations. The IBM43RF0100EV Active Bias Evaluation Board contains an active bias network and requires a V_{CC} supply, but no bias supply. The IBM43RF0100EV External Bias Evaluation Board does not contain a bias network and must be supplied with V_{BB} = +0.823Vdc.

Evaluation Board Theory of Operation

The active bias evaluation board (Figure 1) contains an active bias network consisting of bipolar transistors Q1 and Q2. The Q point of the IBM43RF0100 transistor is set by the network. Although active bias increases component counts, it stabilizes the bias point in the presence of variations in DC characteristics from device to device. Detailed design information is available in chapter 5 of Ralph Carson's *High Frequency Amplifiers, 2nd Edition* (J. Wiley, 1975).

Using the Evaluation Boards

> **Note:** Evaluation boards are sensitive to electrostatic discharge (ESD). Observe normal ESD precautions at all times. Do not apply DC or RF energy to evaluation boards until all connections have been properly made.

As shown in Figures 3 and 4, both evaluation boards have separate terminals for RF input, RF output, DC power, and ground. All RF connections are made through SMA connectors. RF connections must be made to 50 ohm devices using 50 ohm cable.

For the external bias board, DC power and ground are connected through a three-conductor cable with the following leads:

- Red: +3.0Vdc V_{CC}
- Black: DC ground
- White: +0.823Vdc V_{BB}

The active bias evaluation board does not require V_{BB} and is supplied with a two-conductor pin connection that omits the white V_{BB} lead.

Regulated DC power supplies must be used with both evaluation boards. The external bias evaluation board requires a V_{BB} of +0.823Vdc. Because no base current limiting is provided, V_{BB} must remain constant. Small increases in V_{BB} can create large base-emitter current swings that could destroy the IBM43RF0100 transistor. Remote voltage sensing for V_{CC} must be used when making gain expansion measurements with the external bias board.

Before making connections to the evaluation boards, shut off all power supplies and RF test instruments. Set all output levels to zero. When all connections have been made, preset V_{BB} to +0.823Vdc (when using the external bias evaluation board) before applying dc power to the board. This will help protect the transistor base-emitter junction by limiting base-emitter current flow. For both boards, slowly increase V_{CC} to +3.0Vdc. The current draw should rise to around 6mA. If not, turn off all power supplies and recheck all cables and connections.

When using evaluation boards as test fixtures, shut off all power supplies before placing IBM43RF0100 transistors into the fixture. Otherwise, the charge held by decoupling capacitor C4 could destroy the transistor base-emitter junction.

Figure 1. Active Bias Evaluation Board Schematic Diagram

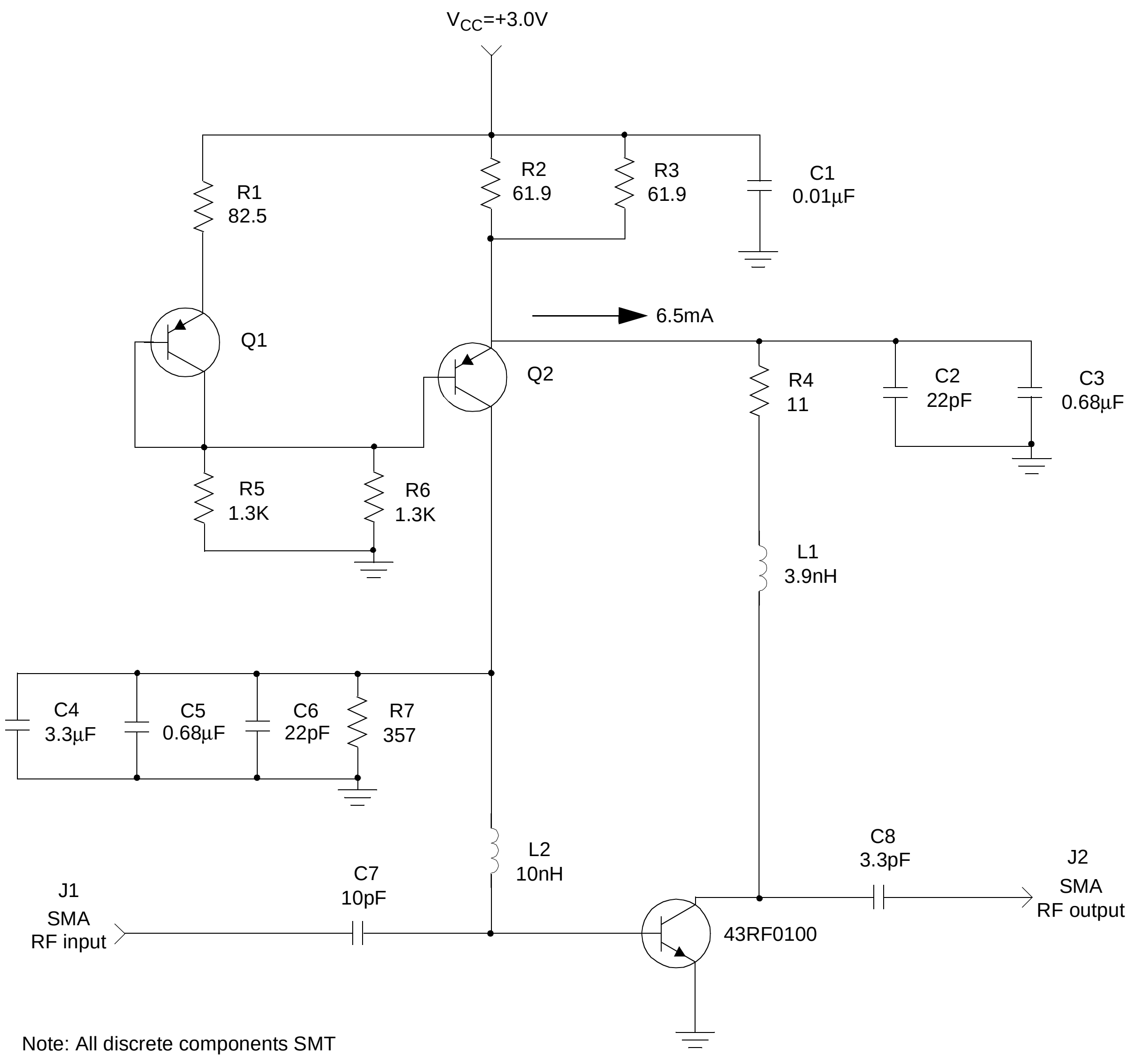
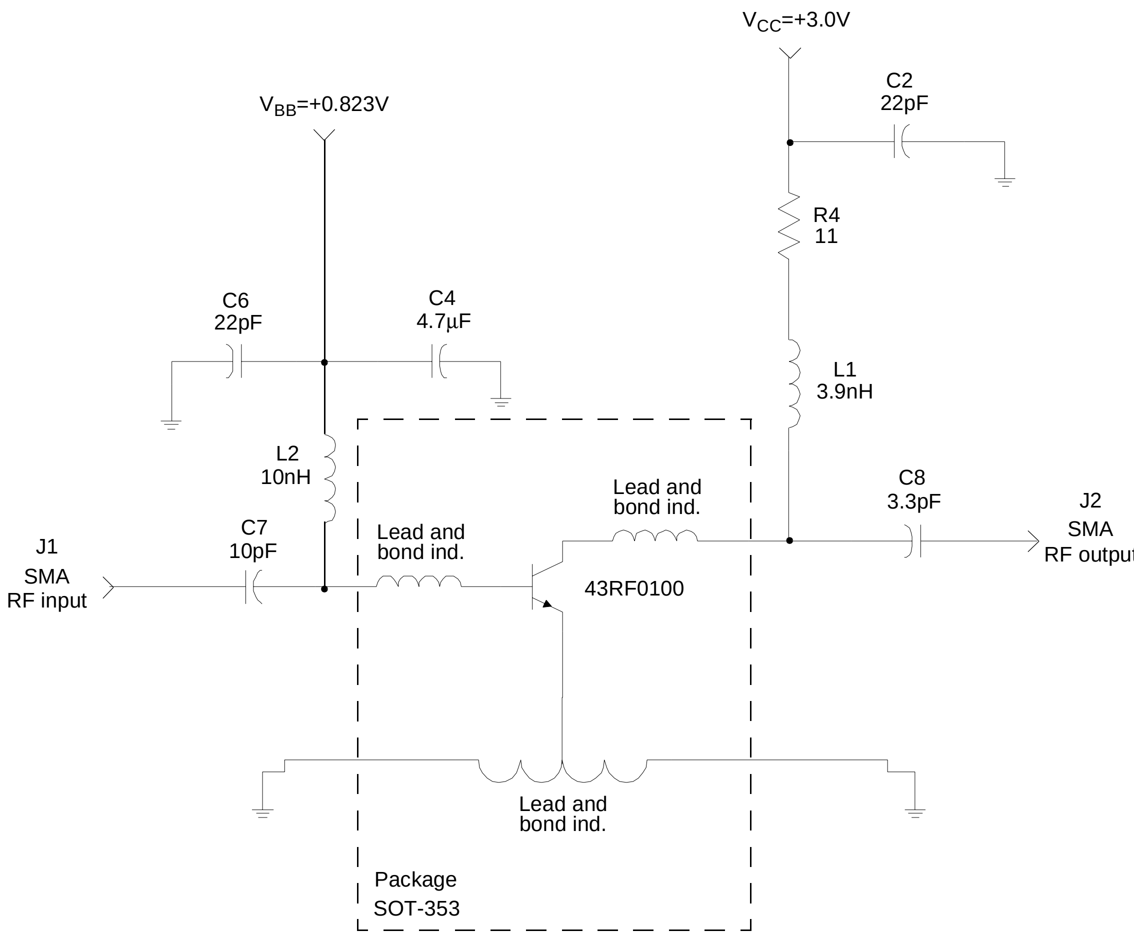


Figure 2. External Bias Evaluation Board Schematic Diagram



Note: All discrete components SMT

Figure 3. Active Bias Evaluation Board Component Locations

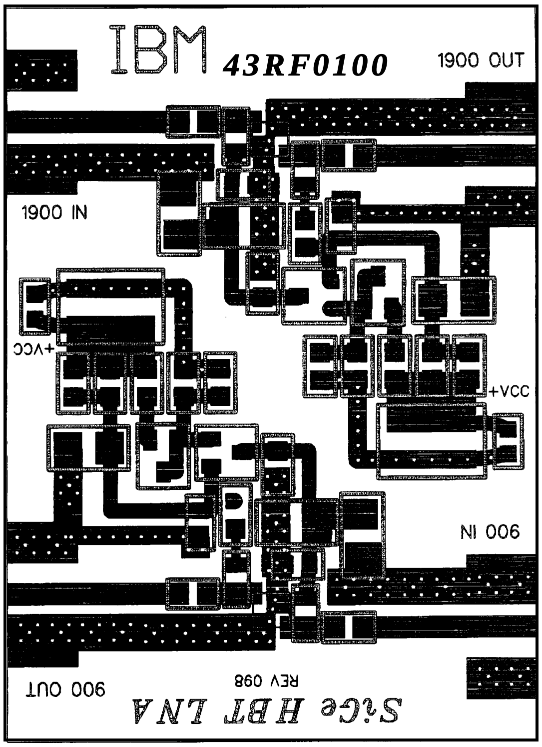


Figure 4. External Bias Evaluation Board Component Locations

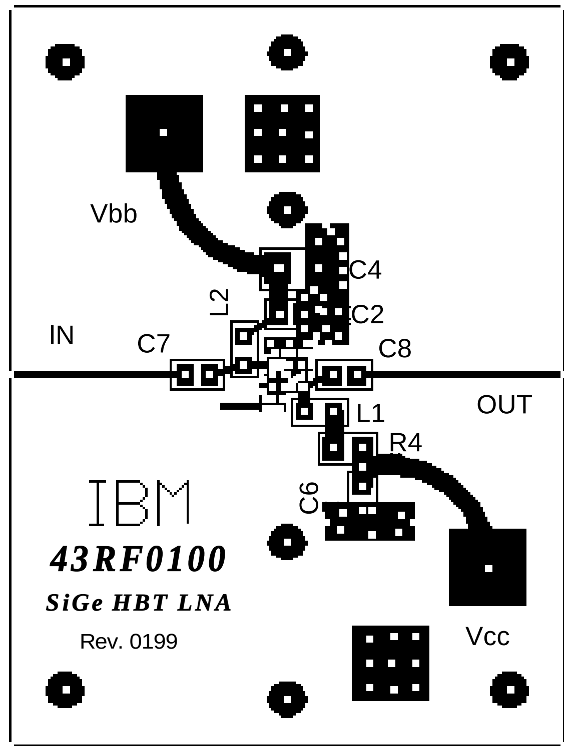
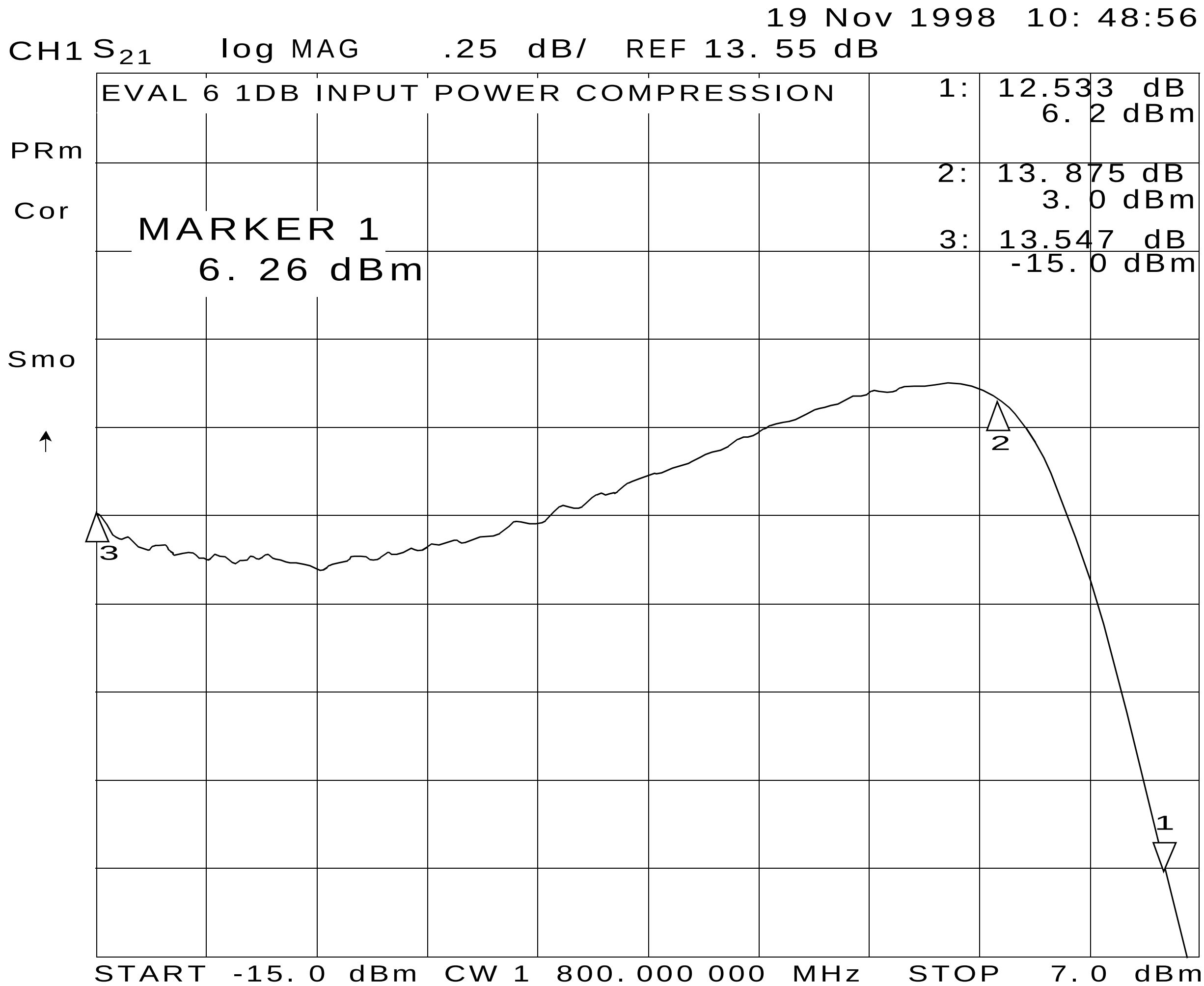


Table 1. Evaluation Board Parts List

Reference Designator	Value	Part Number	Vendor	Notes
C1	0.01µF	06035C103JAT	AVX	1
C2, C6	22pF	06031A220JAT	AVX	
C3, C5	0.68µF	0612ZC684MAT	AVX	1
C4	3.3µF	TPSA335K06R3500	AVX	1
C4	4.7µF	TPSA475K06R3500	AVX	
C7	10pF	06031A100CAT	AVX	
C8	3.3pF	06031A3R3DAT	AVX	
J1, J2	SMA female	142-0701-881	E.F. Johnson	
L1	3.9nH	L08053R9CEW	AVX	
L2	10.0H	L0805100JEW	AVX	
Q1, Q2	GP PNP	FMMT2907ATA	Zetex	1
---	SiGe NPN	IBM43RF0100	IBM	
R1	82.5	ERJ-6ENF82R5	Panasonic	1
R2, R3	61.9	ERJ-6ENF61R9	Panasonic	1
R4	11	ERJ-6ENF11R0	Panasonic	
R5, R6	1.3K	ERJ-6ENF1301	Panasonic	1
R7	357	ERJ-6ENF3570	Panasonic	1

1. Active bias evaluation board only.

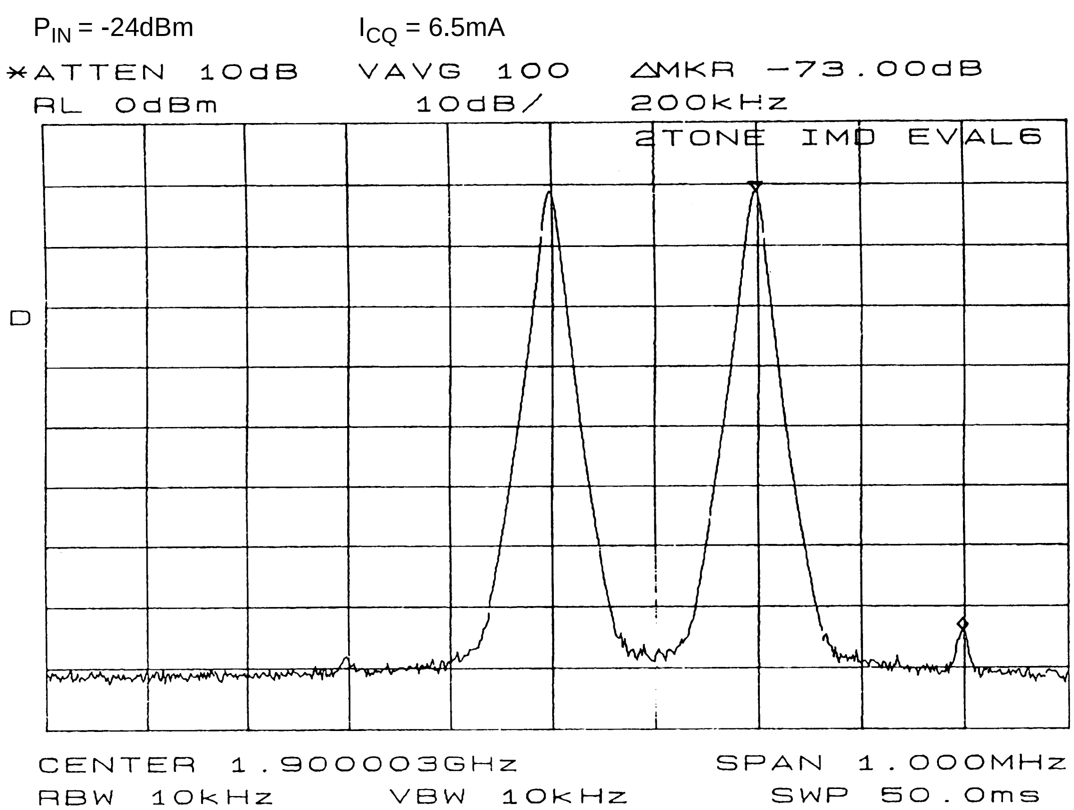
Figure 5. 1dB Input Power Compression



Notes:

1. The V_{BB} bias is adjusted with no input signal for an Idc value of 6.5mA.
2. The 1dB input power compression curves require a constant voltage base bias voltage source of +0.823 volts. This should yield an Idc value of 6.5mA.
3. A device biased Class AB will demonstrate gain expansion at about -6dBm input (see plot). The 1dB input power compression point is at +6dBm.
4. The V_{CC} supply voltage for the unit under test *must* use remote voltage sense. If not, power output slump will occur, not due to the device, but due to iR drop in the power supply bias.

Figure 6. Two-Tone Intermodulation Distortion



Notes:

1. IMD two-tone measurements were conducted at a V_{CC} bias voltage of +3 volts.
2. The plots were conducted at an Idc of 6.5mA with a Pin of -24dBm. This represents an IIP3 of 12.5dBm.

Evaluation Board-Datasheet Differences

The IBM43RF0100EV evaluation boards differ from the descriptions contained in the IBM43RF0100 datasheet. These differences are noted below.

Two evaluation boards for evaluating the performance of the IBM43RF0100 SiGe Low Noise Transistor are available. These boards allow the user to investigate high linearity and low noise performance at 1.9 GHz. Additional design information for 900 MHz will be available in the future. The active bias evaluation board has an uncommitted portion of the PCB for this purpose. Thus, users can evaluate designs at other frequencies if desired.

The evaluation boards differ mainly in the bias techniques used. The active bias evaluation board uses PNP transistor Q2 with the diode connected PNP to function as a minimal temperature-compensated constant current source. DC feedback provided by the composite β of the 43RF0100 and transistor Q2 force the collector current of the RF device to be independent of device β.

Excellent design information is available in chapter 5 of Ralph Carson's *High Frequency Amplifiers, 2nd Edition* (J. Wiley, 1975). In addition, several manufacturers provide the active bias network in a self-contained IC.

Since the active bias network constrains the RF device collector and base currents, gain compression occurs at a nominal input level of -12dBm in the current design. No gain expansion is present.

The active bias evaluation board is excellent for characterizing small signal nonlinearity, IP3, noise figure, and device-to-device variations in RF parameters. Intermodulation distortion should be constant with frequency offset or channel spacing. Proper decoupling at audio frequencies is important to ensure this level of performance. For channel spacing less than 200 kHz, degradation of IP3 is possible due to insufficient audio bypass in the active bias network. If applications require a channel separation of less than 200 kHz, it is advisable to increase the values of capacitors C3 and C5 accordingly.

A nominal noise figure of 1.5dB with IIP3 of +10dBm minimum is achieved. These values, coupled with a gain of 12dB and unconditional stability at low RF device power consumption, are excellent tradeoffs. The evaluation board is not matched for minimum noise figure or maximum gain. Instead, a balanced tradeoff is maintained. Exact RF device current consumption is determined by measuring the voltage drop across 11-ohm stabilizing resistor R4. The active bias network is a stiff bias source. The network takes approximately the same bias current as the RF device.

The external bias evaluation board permits the use of class AB bias to evaluate RF device large signal operation. Different DC voltage levels, gain compressions, and gain expansions can be characterized. With no constant base bias current restraints, class AB bias allows the dc current level to increase under increasing RF drive levels.

With this arrangement, ACPR and large signal linearity is evaluated. Extra care must be exercised in setting bias conditions. Nominal base voltage is +0.823Vdc. V_{CC} at +3Vdc should use remote voltage sensing to accurately evaluate gain expansion at a -6dBm input power level.

For further technical assistance and data on the IBM43RF0100 transistor, consult the factory or refer to the *SiGe High Dynamic Range Low Noise Transistor* datasheet, available on-line at www.chips.ibm.com.

Conclusion

The IBM43RF0100EV Evaluation Boards provide a convenient means of testing and evaluating the performance of the IBM43RF0100 SiGe High Dynamic Range Low Noise Transistor at 1.9 GHz. A variety of parameters such as noise, power, distortion, and s-parameters can be determined under a variety of operating conditions.