Introduction

To assist in creating the best system designs using the fastest PowerPC 750s, the following guidelines are recommended.

L2 Interface

Pipeline Synchronous Burst SRAMs

Figure 1 shows the L2 interface interconnection for Pipeline Synchronous Burst SRAMs. Explanation of this type of interconnection is as follows.

- **Non-burst operation:** The 750 generates addresses for each beat of a burst read or write; therefore, the pipelined synchronous SRAM is connected in non-burst mode by setting $\overline{ADSP}$ = $\overline{ADV}$ = high, and $\overline{ADSC}$ = $\overline{LBO}$ = low.
- **Write enable:** The 750 $\overline{L2WE}$ is connected to the global write $\overline{GW}$. Byte writes are not used by the 750, so all byte write enables are tied inactive.
- **Chip selects:** The 750 $\overline{L2CE}$ is connected to $\overline{CS1}$. The other two chip selects, $\overline{CS2}$, and CS2, as well as $\overline{OE}$, are always tied enabled.
- **Single ended L2 clocks:** L2CLK_OUTA goes to one SRAM, and L2CLK_OUTB goes to the other SRAM. L2CLK_OUTA, B, and L2SYNC_OUT are all in phase with each other. Single ended clocking is programmed by setting L2CR(17) low.

Late Write Synchronous SRAMs

Figure 2 shows the L2 interface interconnection for IBM Late Write Synchronous SRAMs. Explanation of this type of interconnection is as follows.

- **Non-burst operation:** The IBM SRAMs shown in Figure 2 are non-burst SRAMs. The 750 will supply the address to the SRAM each cycle.
- **Write enable:** The 750 $\overline{L2WE}$ is connected to the global write $\overline{SW}$. Byte writes are not used by the 750, so all byte write enables are tied inactive.
- **Chip selects:** The 750 $\overline{L2CE}$ is connected to the global chip select $\overline{SS}$.
- **Differential L2 clocks:** L2CLK_OUTA and L2CLK_OUTB go to both SRAMs. L2CLK_OUTA goes to K, and L2CLK_OUTB goes to $\overline{K}$. Differential clocking is programmed by setting L2CR(17) high.
- **Clocking Mode:** This SRAM only supports the JEDEC single clock pipeline mode; therefore, M1 = tied low and M2 = tied high.

L2 Layout Considerations

L2 layout considerations to be followed are the same for Figure 1 or Figure 2.

- **Board Impedance (Zo):** Use at least 50 ohm controlled impedance boards.
- **L2 Clock Termination and Placement of Resistors:** All three L2 clock lines (L2_SYNC, L2CLK_OUTA, and L2CLK_OUTB) must be the same length and topology. We recommend using 33 ohm series termination resistors placed as near to the processor as possible. The ideal value of the resistor is 1/2 Zo.
- **L2 Clock, Address, and Data Line Lengths:** Make the three clock lines approximately 2 inches each, and the data and address lines as close to this length as possible, with the longest tracelengths not exceeding 2.5 inches. For extremely high speed designs, the longest address and data tracelengths must not exceed the worst clock line length.
- **L2 Clock, Address, and Control Routing:** Lines with two loads can be routed either daisy chain or from a T. For very high speed L2 interfaces, a T structure is preferred for balancing out transmission line effects.
- **SRAM placement:** SRAMs placed side by side on same side of the board are recommended because there is less concentrated noise and less power density.
- **SRAMs without parity:** x32 SRAMs may be used instead of x36 SRAMs See “Unused Pins” for how to tie off unused parity pins.

Figure 1. Pipelined Burst SRAM Interconnection

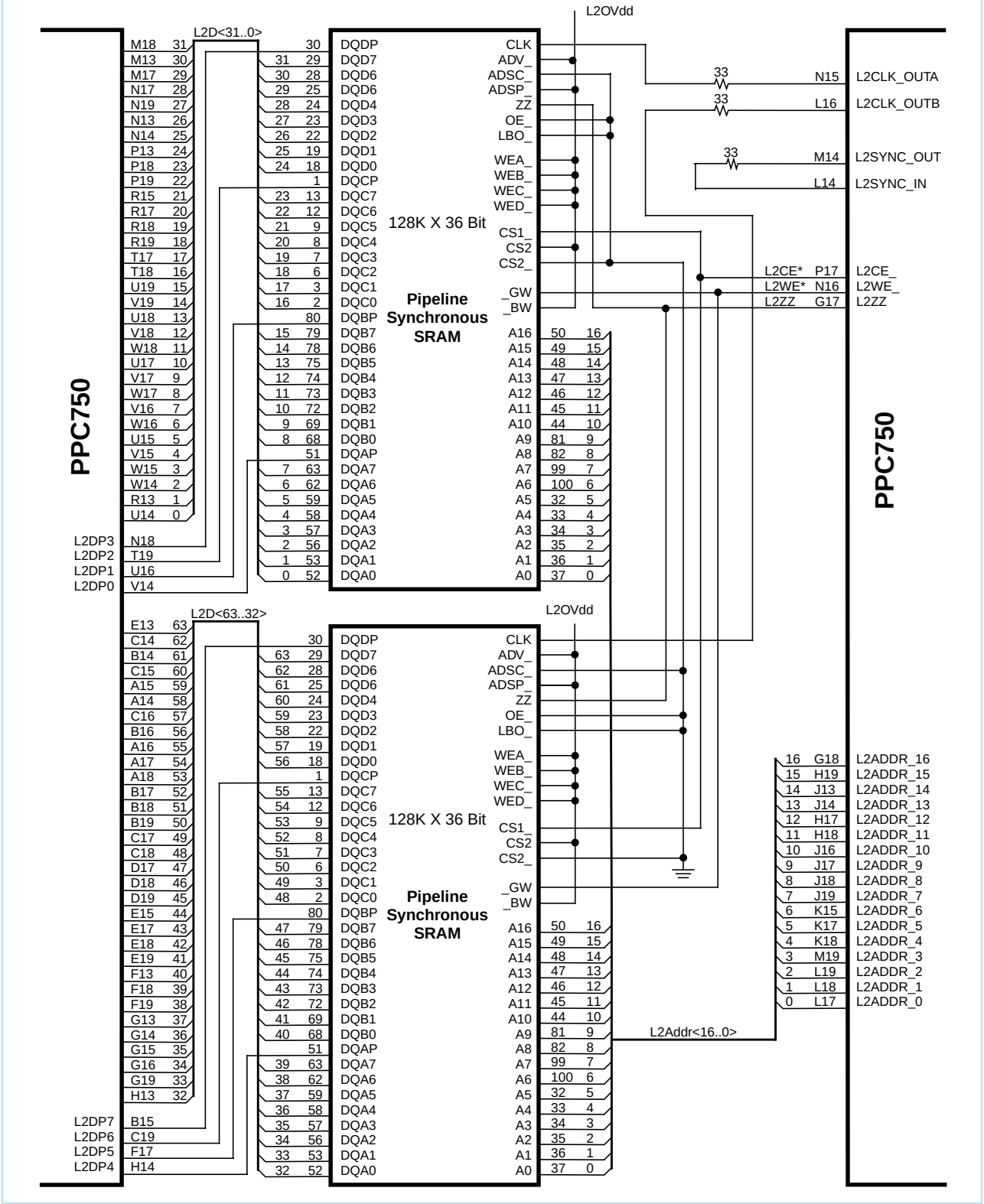
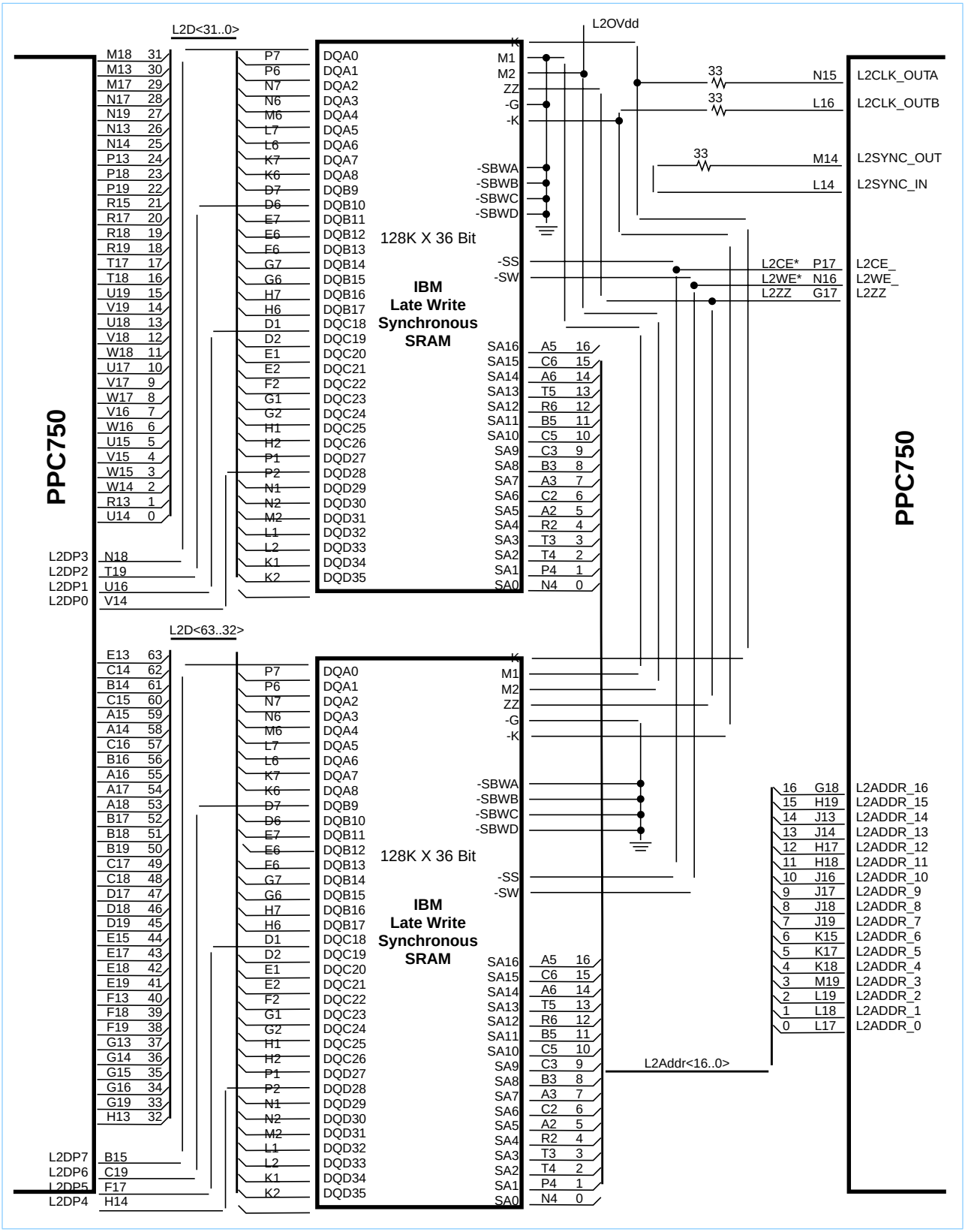


Figure 2. Late Write SRAM Interconnection



SRAMs Used

SRAMs that have been successfully used in applications at IBM are listed below.

- IBM Late Write BGA 128k x 36 (IBM043641RLAD - 5, 6, 7)
- Samsung TQFP 128k x 36 (KM736V789-6 and slower)
- Mitsubishi TQFP 64k x 32 (M5M5V2132GP-5H and slower)

From recent trade press articles, the following SRAMs have also been successfully used by other companies in their PPC system designs.

- IBM Late Write BGA 128k x 36 (IBM043641WLAB - 3P, 3, 4)

Note: Observed speed running 300MHz at 1:1.

Note that other SRAMs with similar output valid, output hold, input setup, and input hold timings may work equally as well.

L2 Cache Control Register (L2CR)

The L2 cache control register is used to configure and enable the L2 cache. The L2CR is a supervisor-level read/write, implementation-specific register that is accessed as SPR 1017. The contents of the L2CR are cleared during power-on reset. The following table describes the L2CR bits.

L2 Cache Initialization

Following a power-on or hard reset, the L2 cache and the L2 DLL are disabled initially. Before enabling the L2 cache, the L2 DLL must first be configured through the L2CR register, and the DLL must be allowed 640 L2 clock periods to achieve phase lock. Before enabling the L2 cache, other configuration parameters must be set in the L2CR, and the L2 tags must be globally invalidated. The L2 cache should be initialized during system start-up.

The sequence for initializing the L2 cache is as follows.

1. Power-on reset (automatically performed by the assertion of $\overline{\text{HRESET}}$ signal).
2. Disable interrupts and Dynamic Power Management (DPM).
3. Disable L2 cache by clearing L2 CR[L2E].
4. Set the L2CR[L2CLK] bits to the desired clock divider setting. Setting a nonzero value automatically enables the DLL. All other L2 cache configuration bits should be set to properly configure the L2 cache interface for the SRAM type, size, and interface timing required.
5. Wait for the L2 DLL to achieve phase lock. This can be timed by setting the decrementer for a time period equal to 640 L2 clocks, or by performing an L2 global invalidate.
6. Perform an L2 global invalidate. The global invalidate could be performed before enabling the DLL, or in parallel with waiting for the DLL to stabilize. Refer to the Section ”L2 Cache Global Invalidation,” for more information about L2 cache global invalidation. Note that a global invalidate always takes much longer than it takes for the DLL to stabilize.
7. After the DLL stabilizes, an L2 global invalidate has been performed, and the other L2 configuration bits have been set, enable the L2 cache for normal operation by setting the L2CR[L2E] bit to 1.

L2 Cache Global Invalidation

The L2 cache supports a global invalidation function in which all bits of the L2 tags (tag data bits, tag status bits, and LRU bit) are cleared. It is performed by an on-chip hardware state machine that sequentially cycles through the L2 tags. The global invalidation function is controlled through L2CR[L2I], and it must be performed only while the L2 cache is disabled. The PowerPC 750 can continue operation during a global invalidation provided the L2 cache has been properly disabled before the global invalidation operation starts.

The sequence for performing a global invalidation of the L2 cache is as follows.

1. Execute a **sync** instruction to finish any pending store operations in the load/store unit, disable the L2 cache by clearing L2CR[L2E], and execute an additional **sync** instruction after disabling the L2 cache to ensure that any pending operations in the L2 cache unit have completed.
2. Initiate the global invalidation operation by setting the L2CR[L2I] bit to 1.

3. Monitor the L2CR[L2IP] bit to determine when the global invalidation operation is completed (indicated by the clearing of L2CR[L2IP]). The global invalidation requires approximately 32K core clock cycles to complete.

After detecting the clearing of L2CR[L2IP], clear L2CR[L2I] and re-enable the L2 cache for normal operation by setting L2CR[L2E].

L2 Cache Control Register

Bit	Name	Function
0	L2E	L2 enable.
1	L2PE	L2 data parity generation and checking enable.
2–3	L2SIZ	L2 size—Should be set according to the size of the L2 data RAMs used. 00 Reserved 01 256 Kbyte 10 512 Kbyte 11 1 Mbyte
4–6	L2CLK	L2 clock ratio (core-to-L2 frequency divider). 000 L2 clock and DLL disabled 001 ÷1 010 ÷1.5 011 Reserved 100 ÷2 101 ÷2.5 110 ÷3 111 Reserved
7–8	L2RAM	L2 RAM type—Configures the L2 RAM interface for the type of synchronous SRAMs used. 00 Flow-through (register-buffer) synchronous burst SRAM 01 Reserved 10 Pipelined (register-register) synchronous burst SRAM 11 Pipelined (register-register) synchronous late-write SRAM
9	L2DO	L2 data-only. Setting this bit disables the caching of instructions in the L2 cache.
10	L2I	L2 global invalidate. Setting L2I invalidates the L2 cache globally by clearing the L2 status bits.
11	L2CTL	L2 RAM control (ZZ enable). Setting L2CTL enables the automatic operation of the L2ZZ (low-power mode) signal for cache RAMs that support the ZZ function. This bit should not be set when the 750 is in nap mode and snooping is being performed through deassertion of $\overline{\text{QACK}}$.
12	L2WT	L2 write-through. Setting L2WT selects write-through mode (rather than the default copy-back mode) so all writes to the L2 cache also write through to the 60x bus.
13	L2TS	L2 test support. Setting L2TS causes cache block pushes from the L1 data cache that result from **dcbf** and **dcbst** instructions to be written only into the L2 cache and marked valid, rather than being written only to the 60x bus and marked invalid in the L2 cache in case of hit. If L2TS is set, causes single-beat store operations that miss in the L2 cache to be discarded.
14–15	L2OH	L2 output hold. These bits configure the output hold time of the address, data, and control signals driven by the 750 to the L2 data RAMs. 00 0.5 nS 01 1.0 nS 10 Reserved 11 Reserved
16	L2SL	L2 DLL slow. Setting L2SL enables L2 data RAM clocking at frequencies less than 100 MHz.
17	L2DF	L2 differential clock. Setting L2DF configures the two clock-out signals (L2CLK_OUTA and L2CLK_OUTB) of the L2 interface to operate as one differential clock.
18	L2BYP	L2 DLL bypass. L2BYP is intended for use when the PLL is being bypassed, and for engineering evaluation.
19–21	—	Reserved. These bits are implemented but not used; keep at 0 for future compatibility.
22	L2CS	Used for processor test purposes. Keep at 0 for normal operation.
23	L2DRO	Used for processor test purposes. Keep at 0 for normal operation.
24-30	L2CTR	L2 DLL counter value (read only).
31	L2IP	L2 global invalidate in progress (read only)—This read-only bit indicates whether an L2 global invalidate is occurring.

Switching Between Modes and Settings

During debug, it may be useful to switch between various L2 modes and settings. For clean clock transitions and so that the processor does not hang, do the following.

- Disable the L2; L2CR(0) = 0.
- Turn off the L2 clocks; L2CR(4:6) = 000.
- Write the new L2 clock ratio, L2 size, and L2 type into the L2CR.
- Invalidate the L2 tags by going through the L2 Cache Global Invalidation procedure.
- Re-enable the L2 interface; L2CR(0) = 1.

Output Hold Settings

For pipelined SRAMs, use the minimum output hold setting L2CR(14,15) = 00 and for Late Write SRAMs, use L2CR(14,15) = 01, as specified in the PowerPC750 Datasheets. Note that increasing output hold will increase output valid by the same amount.

Decoupling on Power Supplies

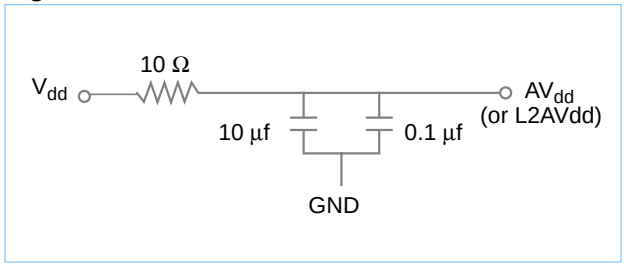
Vdd, OVdd

To reduce inductance, use thick traces that are close to vias connecting to the power planes and place decoupling caps close to the processor. Place multiple 0.1µf ceramic caps directly under the processor and with SMT pads directly tied to the Vdd and OVdd planes. Add 2-3 bulk 10µf ceramic (low ESR) caps for each voltage plane (Vdd and OVdd).

AVdd, L2AVdd

Both AVdd and L2AVdd must have their own filter tank circuit from Vdd as shown in Figure 3. The recommended circuit is a series 10 ohm resistor with a 10µf bulk capacitor and a 0.1µf capacitor. The 0.1µf must be placed very near the processor solder ball (ideally, immediately behind it). If backside capacitors cannot be supported, a thick trace must be used to escape the BGA cage, and the cap must be right on the processor edge.

Figure 3. AVdd or L2AVdd Filter Circuit



Unused Pins

Unused 60X bus or L2 bus parity pins must be tied high through a pullup resistor (1k to 10k).

Other unused I/Os, which are outputs only, do not need to be tied.

Any I/Os, which may be used as inputs for test purposes, must also be tied to avoid crowbar current in the receiver. The PPC 750 Datasheet documents how to tie test pins that are not used in normal operation in the pinout listings. For I/Os which are tied low, use a 100 ohm pull down resistor.

Debug Tips

Tip#1: If a system will not boot within the voltage range specified by the part number, but will boot below the minimum voltage range, check that I/Os which are supposed to be tied are actually tied and not floating.

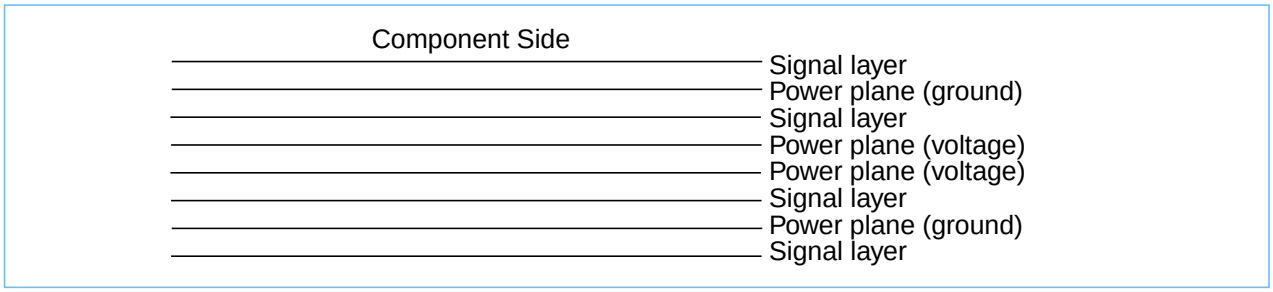
Tip#2: If a system boots without L2 enabled but not with L2 enabled, try lengthening the output hold using the L2CR(14,15) bits and reducing the processor core frequency. Also, check that L2CR(17) is configured correctly for the type of SRAM being used.

Tip#3: For Latewrite SRAM applications that have plenty of margin on the board design, lowering the output hold setting to L2CR(14,15) = 00 may work well and boost performance.

Clean Board Design Guidelines

An ideal board construction is shown in Figure 4. It is constructed with two voltage planes in the center, two signal layers, two ground planes, and two external layers.

Figure 4. Signal and Power Layers



References

Included below is a list of references for additional information regarding the PowerPC 750 product family and the IBM Static RAM memory products.

These documents can be found via the IBM Microelectronics web site.

IBM PowerPC web site: http://www.chips.ibm.com/products/ppc

IBM SRAM web site: http://www.chips.ibm.com/products/memory

1. “PowerPC 740/750 RISC Microprocessor User Manual,” Document No. GK21-0263-00, 6/98.
2. “PowerPC 750 SCM RISC Microprocessor Datasheet for the PID8p,” version 1.3, 8/12/98.
3. “PowerPC 750 SCM RISC Microprocessor Datasheet for the PID8t,” version 3.1, 6/10/98.
4. 128Kx36 & 256Kx18 SRAM Datasheet, Document No. 50H5020, 6/98.
5. IBM Memory Products Application Note, “Understanding Static RAM Operation,” 3/97.

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