Intel® IXF30005

Digital Wrapper for 10Gbit/s Optical Transport Networks (OTN)

Intel®
Internet Exchange
Architecture

The Intel® IXF30005 is a fully compliant G.709 digital wrapper device that covers most OTN applications on a single chip. Based on the digital signal wrapping technique defined by ITU-T G.709, the IXF30005 provides all functions required for an optical network transmission system, including transmission protection based on Forward Error Correction (FEC). With integrated FEC error statistics and overhead processing facilities, the Intel IXF30005 is a key component in wrapper-based transparent operation, administration, maintenance and provisioning of optical networks.

The IXF30005 is built on technology developed for the Intel® IXF30001 and Intel® IXF30003, which were the first 10Gbit/s FEC devices in the market. Supporting both asynchronous and synchronous mapping schemes, the IXF30005 provides special features for SONET/SDH data streams, such as a Performance Monitor (PM) and post processor.

Acting as a direct pin and software compatible drop-in replacement for the Intel IXF30001 and IXF30003 (FEC100), the Intel IXF30005 supports IXF30001 and IXF30003 G.975 framing, as well as ITU-T G.709. The IXF30005 may be operated as a gateway between existing IXF30001- or IXF30003-based systems and ITU-T G.709-compliant equipment.

Dual Data Paths

The Intel IXF30005 contains two completely separate signal paths (north and south) that are designed to operate as receiver and transmitter for single chip transponder applications. Using integrated bridges between both paths, the IXF30005 provides APS support and may also be configured as a regenerator. The IXF30005 supports both synchronous and asynchronous mapping of STM-64 streams for SDH payload data, and an integrated, non-intrusive PM in the south path (the FEC transmitter) can be used to check incoming payload signal quality.
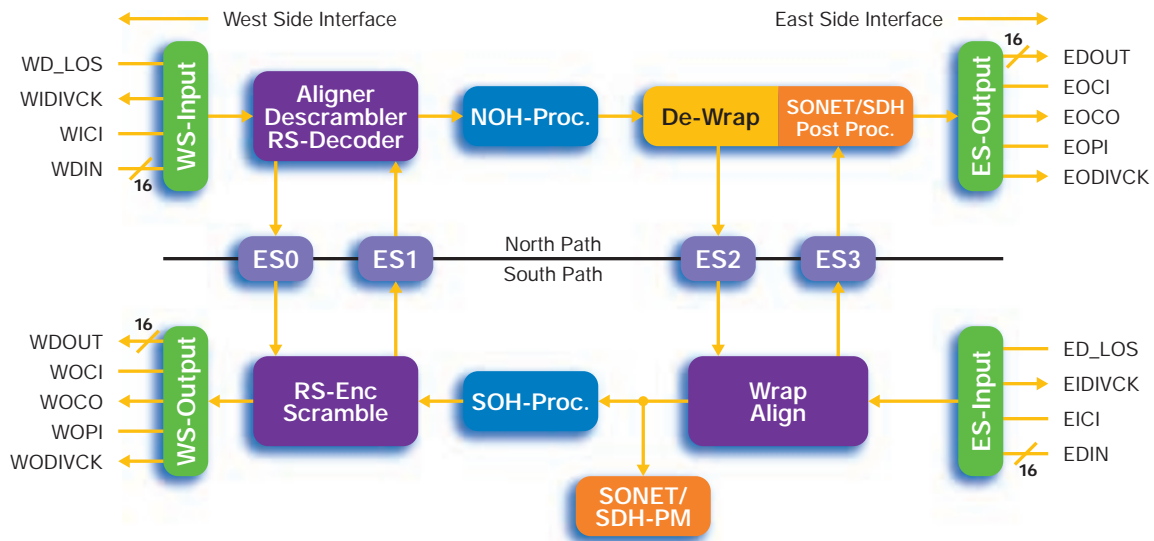
On the north path (the FEC receiver), an integrated SOH processor allows extraction of up to two configurable bytes. In the event of severe transmission error, such as the loss of signal or wrapper frame synchronization, received SONET/SDH data may be replaced by AIS frames.

Key Applications

- Long-haul optical transmission networks
- Increasing bandwidth in existing systems
- Submarine applications
- Optical Transport Networks according to G.709
- Bridge/gateway function between existing networks (SONET/SDH) and optical transport networks (OTN)

Support Collateral

- IXF30005 Data Sheet
- IXD80102 Evaluation System
- SONET/SDH Aggregation to OTN Application Brief
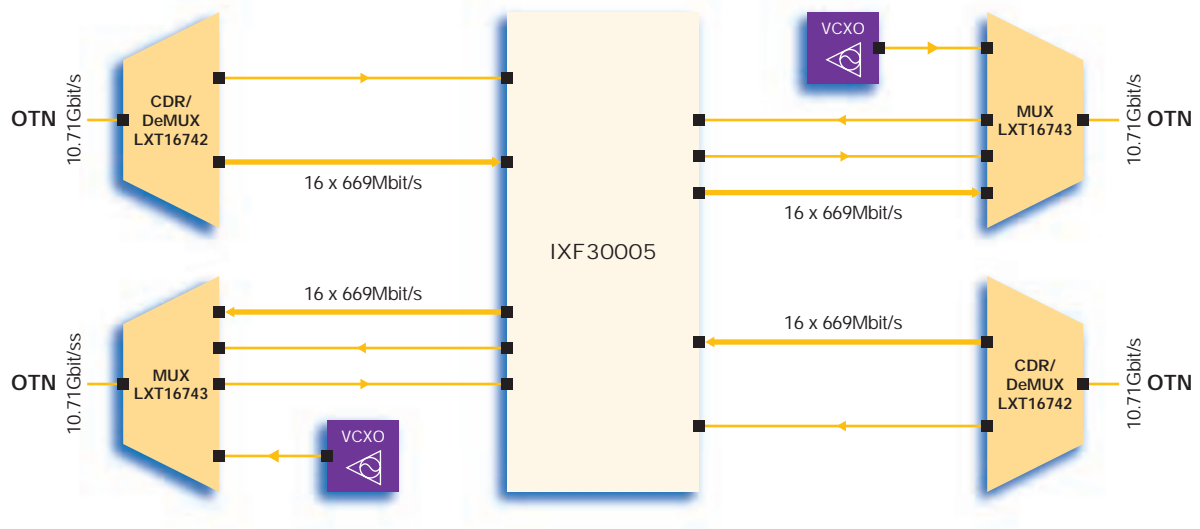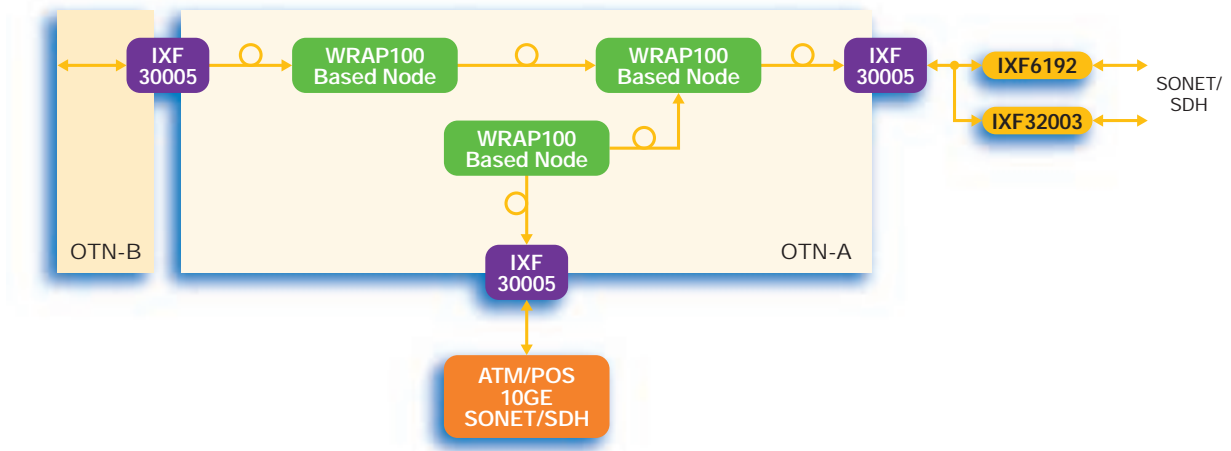- OTN/G.709 Optical Transport Network Node Interface Elements/Interconnects
- FAQs

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West Side Interface — East Side Interface (block diagram)

WD_LOS, WIDIVCK, WICI, WDIN (16) → WS-Input → Aligner Descrambler RS-Decoder → NOH-Proc. → De-Wrap / SONET/SDH Post Proc. → ES-Output → EDOUT (16), EOCI, EOCO, EOPI, EODIVCK

ES0 — ES1 — North Path / South Path — ES2 — ES3

WDOUT (16), WOCI, WOCO, WOPI, WODIVCK ← WS-Output ← RS-Enc Scramble ← SOH-Proc. ← Wrap Align ← ES-Input ← ED_LOS, EIDIVCK, EICI, EDIN (16)

SONET/SDH-PM

Features	Benefits
■ Flexible 10Gbit/s digital wrapper for OTN with ITU-T G.709 compliance, including Forward Error Correction (FEC).	■ Versatile enough to use in many locations and applications within an OTN, designed for current as well as future applications.
■ Wide coverage of OTN overhead functions implemented in hardware.	■ Reduces costs, space, power and software development time.
■ OC-192/STM-64 client processing related to OTN functions and applications.	■ Compliance with existing standards reduces development time.
■ Drop-in replacement for IXF30001 or IXF30003 (FEC100). Identical footprint and physical characteristics.	■ Eases migration pass and reuses all 622/66MHz PCB RF qualification data. Allows bridging between FEC100-based systems and OTN.
■ Low power consumption (4W maximum).	■ Eases mechanical systems design and power management.
■ OC-192/STM-64 SONET/SDH performance monitor (B1, B2, J0, general purpose) and post processor (AIS insertion).	■ No additional performance monitor device required, basic SDH functionality downstream.
■ Bidirectional device for single chip transponder operation (synchronous or asynchronous).	■ Compact system design, reduced cost, lower power consumption, different clocking schemes from which to choose.
■ OIF-compliant LVDS Inputs/Outputs.	■ Allows use of SERDES components provided by Intel and 3rd party vendors.

IXF30005 application diagram:

OTN 10.71Gbit/s → CDR/DeMUX LXT16742 → 16 x 669Mbit/s → IXF30005

OTN 10.71Gbit/ss → MUX LXT16743 → 16 x 669Mbit/s → IXF30005 (VCXO)

IXF30005 → 16 x 669Mbit/s → MUX LXT16743 (VCXO) → OTN 10.71Gbit/s

IXF30005 → 16 x 669Mbit/s → CDR/DeMUX LXT16742 → OTN 10.71Gbit/s

The Intel® IXF30005 may be operated as Intra Domain Interface (IaDI) and Inter Domain Interface (IrDI) within an OTN according to G.709, acting as a gateway between two OTNs or as a network node within an OTN. Because of the various types of framing it supports, the IXF30005 may also act as a gateway between existing IXF30001-based network and an G.709 compliant OTN.

Intel® Internet Exchange Architecture

Intel® Internet Exchange Architecture is an end-to-end family of high-performance, flexible and scalable hardware and software development building blocks designed to meet the growing performance requirements of today's networks. Based on programmable silicon and software building blocks, Intel® IXA solutions enable faster development, more cost-effective deployment and future upgradability of network and communications systems. Additional information can be found at www.intel.com/IXA
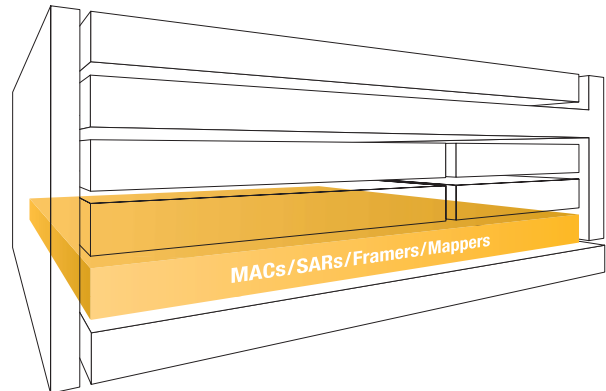
Intel Access

Developer's Site	http://developer.intel.com
Intel® Internet Exchange Architecture Home Page	http://www.intel.com/IXA
Networking Components Home Page	http://developer.intel.com/design/network
Other Intel Support: Intel Literature Center	http://developer.intel.com/design/litcentr (800) 548-4725 7 a.m. to 7 p.m. CST (U.S. and Canada) International locations please contact your local sales office.
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