Workstation cache applications up to 250MHz

1Mb High Performance SRAM

Highlights

Access Time
2.25 ns (Pipeline), 5.7ns (Flow Thru), 6.0 ns (Register Latch)

Cycle Time
4 ns (Pipeline),4 ns (Flow Thru), 6 ns (Register Latch)

Organizations
64K x 18, 32K x 36

Power Dissipation
HSTL x36
Active Power 2.3 W (250Mhz)
Standby Power 8.5 mW

HSTL/LVTTL I/O compatible

HSTL/PECL clock compatible

LVTTL JTAG I/O

Package
Industry standard Ball Grid Array 7 x 17, MO-163.

2.5VI/O capability

3.3Vpower supply

Registered addresses, write enables,synch select,data ins

Registered outputs
Pipeline operations
Register latch operations

Programmable HSTL output impedance

Asynchronous output enable

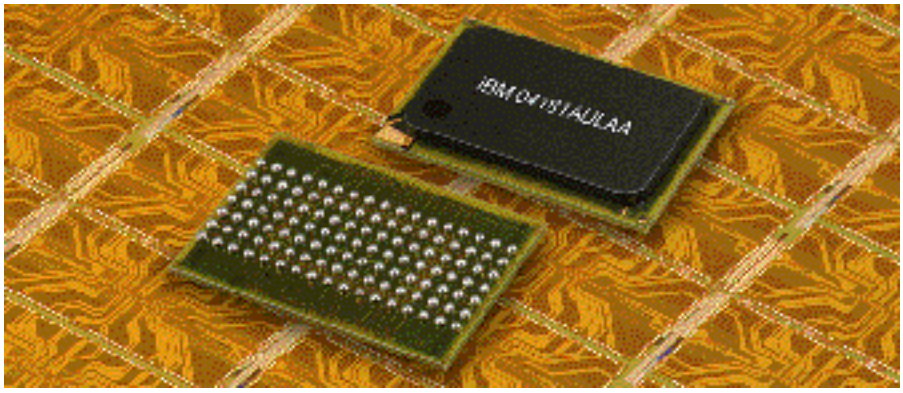
Flow thru output hold time control

Self-timed late write

Byte write capability and global write enable

Asynchronous sleep mode

Boundary scan using limited set of JTAG 1149.1 functions



Description

IBM introduces a High Performance 1 Mb Synchronous SRAM for workstations, workstation servers, and telecommunication applications operating at frequencies up to 250 MHz. These versatile CMOS SRAMs offer wide I/O configurations and various I/O voltage interface levels operating with a single 3.3 volt power supply. They support fully pipelined, flow thru, and register latch operations. The self-timed late write is featured in all SRAM devices.

Pipelined operation is accomplished by placing registers at the inputs and outputs of the devices. During a read or write operation, a latency of one cycle between the addresses and the data is expected. Pipelining is supported with a single clock operation.

Flow thru operation is accomplished by gating the output registers with the output clock. This dual clock operation provides control of the data out window. An output clock can be used to control data output hold time. This mode is available with dual clock operation.

Register latch operation uses the falling edge of the output clock to control the output register.

Self-timed late write simplifies the write operation significantly. The SRAM timings do not require an extra cycle when switching from a read to a write operation.

Product Options (All modules are 3.3V operation and 7x17 BGA.)

Part Number	Features and Compatibility	Access / Cycle Time (ns)	Org.
IBM041810TLAA	Flow Thru, Dual Clock, HSTL	5.7, 6.8, 7.0, 7.5 / 4.0, 5.0, 5.0, 6.0	x18
IBM043610TLAA	Flow Thru, Dual Clock, HSTL	5.7, 6.8, 7.0, 7.5 / 4.0, 5.0, 5.0, 6.0	x36
IBM041811ULAA	Pipeline, Single PECL Clock, LVTTL	2.5, 3.0 / 5.0, 6.0	x18
IBM043611ULAA	Pipeline, Single PECL Clock, LVTTL	2.5, 3.0 / 5.0, 6.0	x36
IBM041811TLAA	Pipeline, Single Clock, HSTL	2.25, 2.5, 3.0 / 4.0, 5.0, 6.0	x18
IBM043611TLAA	Pipeline, Single Clock, HSTL	2.25, 2.5, 3.0 / 4.0, 5.0, 6.0	x36
IBM04181AULAA	Register Latch, Single PECL Clock, LVTTL	6.0, 6.5, 7.0 / 6.0, 6.0, 6.0	x18
IBM04361AULAA	Register Latch, Single PECL Clock, LVTTL	6.0, 6.5, 7.0 / 6.0, 6.0, 6.0	x36

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