



## Features

- 128K x 36 or 256K x 18 Organizations
- CMOS Technology
- Synchronous Pipeline Mode Of Operation with Self-Timed Late Write
- Single Ended Pseudo-PECL Clock compatible with LVTTTL Levels
- Single +3.3V Power Supply,  $V_{DDQ}$  & Ground
- Common I/O & LVTTTL I/O Compatible
- Nominal 45 ohm driver
- Registered Addresses, Write Enables, Synchronous Select and Data Ins
- Registered Outputs
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary Scan Order.

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## Description

The IBM041841WLAD and IBM043641WLAD 4Mb SRAMs are Synchronous Pipeline Mode, high performance CMOS Static Random Access Memories that are versatile, wide I/O, and achieve 3.3ns cycle times. A single ended K clock with  $\bar{K}$  tied to 1.25V are used to initiate the read/write operation, and all internal operations are self-timed. At the rising edge of the K Clock, all Addresses, Write-Enables, Sync

Select and Data Ins are registered internally. Data Outs are updated from output registers off the next rising edge of the K Clock. An internal write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a +3.3V power supply, output power supply compatible with 2.5V or 3.3V, and is compatible with LVTTTL I/O interfaces.

## x36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	SA5	SA7	NC	SA16	SA14	V <sub>DDQ</sub>
B	NC	NC	SA8	NC	SA11	NC	NC
C	NC	SA6	SA9	V <sub>DD</sub>	SA10	SA15	NC
D	DQc18	DQc19	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQb10	DQb9
E	DQc20	DQc21	V <sub>SS</sub>	$\overline{SS}$	V <sub>SS</sub>	DQb12	DQb11
F	V <sub>DDQ</sub>	DQc22	V <sub>SS</sub>	$\overline{G}$	V <sub>SS</sub>	DQb13	V <sub>DDQ</sub>
G	DQc23	DQc24	$\overline{SBWc}$	NC	$\overline{SBWb}$	DQb15	DQb14
H	DQc25	DQc26	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQb17	DQb16
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	DQd34	DQd35	V <sub>SS</sub>	K	V <sub>SS</sub>	DQa8	DQa7
L	DQd32	DQd33	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQa6	DQa5
M	V <sub>DDQ</sub>	DQd31	V <sub>SS</sub>	$\overline{SW}$	V <sub>SS</sub>	DQa4	V <sub>DDQ</sub>
N	DQd29	DQd30	V <sub>SS</sub>	SA0	V <sub>SS</sub>	DQa3	DQa2
P	DQd27	DQd28	V <sub>SS</sub>	SA1	V <sub>SS</sub>	DQa1	DQa0
R	NC	SA4	M1*	V <sub>DD</sub>	M2*	SA12	NC
T	NC	NC	SA3	SA2	SA13	NC	ZZ
U	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**Note:** \* M1 and M2 are clock mode pins. For this application, M1 and M2 are fuse blown to connect to V<sub>SS</sub> and V<sub>DD</sub>, respectively. Thus in this application these pins are No Connects.

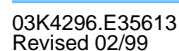
## x18 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V <sub>DDQ</sub>	SA5	SA7	NC	SA16	SA14	V <sub>DDQ</sub>
B	NC	NC	SA8	NC	SA11	NC	NC
C	NC	SA6	SA9	V <sub>DD</sub>	SA10	SA15	NC
D	DQb9	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQa1	NC
E	NC	DQb12	V <sub>SS</sub>	$\overline{SS}$	V <sub>SS</sub>	NC	DQa2
F	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{G}$	V <sub>SS</sub>	DQa4	V <sub>DDQ</sub>
G	NC	DQb15	$\overline{SBWb}$	NC	V <sub>SS</sub>	NC	DQa5
H	DQb16	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQa8	NC
J	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
K	NC	DQb17	V <sub>SS</sub>	K	V <sub>SS</sub>	NC	DQa7
L	DQb14	NC	V <sub>SS</sub>	$\overline{K}$	$\overline{SBWa}$	DQa6	NC
M	V <sub>DDQ</sub>	DQb13	V <sub>SS</sub>	$\overline{SW}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
N	DQb11	NC	V <sub>SS</sub>	SA0	V <sub>SS</sub>	DQa3	NC
P	NC	DQb10	V <sub>SS</sub>	SA1	V <sub>SS</sub>	NC	DQa0
R	NC	SA4	M1	V <sub>DD</sub>	M2	SA13	NC
T	NC	SA2	SA3	NC	SA17	SA12	ZZ
U	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**Note:** \* M1 and M2 are clock mode pins. For this application, M1 and M2 are fuse blown to connect to V<sub>SS</sub> and V<sub>DD</sub>, respectively. Thus in this application these pins are No Connects.



## Block Diagram



## SRAM Features

### Late Write

The Late Write function allows for write data to be registered one cycle after addresses and controls. This feature will alleviate SRAM data bus contention going from a Read to Write cycle by eliminating one dead cycle. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. In case a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with the address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array data occurs on a byte by byte basis. When one byte is written during a write cycle, read data from the last written address will have new byte data from the write buffer and remaining bytes from the SRAM array.

### Mode Control

There is no Mode Control available on this part. Fuses are blown to pre-set the part to Pipeline Mode. \* General Definition: Mode control pins: M1 and M2 are used to select four different JEDEC standard read protocols. This SRAM only supports the single clock pipeline (M1 =  $V_{SS}$ , M2 =  $V_{DD}$ ) protocol. Mode control inputs must be set with power up and must not change during SRAM operation.

### Power Down Mode

Power Down Mode, or "Sleep Mode," is accomplished by switching asynchronous signal ZZ high. When powering the SRAM down, inputs must be dropped first and  $V_{DDQ}$  must be dropped before or simultaneously with  $V_{DD}$ .

### Power-Up Requirements

In order to guarantee the optimum internally regulated supply voltage, the SRAM requires 4 $\mu$ s of power-up time after  $V_{DD}$  reaches its operating range. Power up requirements for the SRAM are that  $V_{DD}$  must be powered before or simultaneously with  $V_{DDQ}$ , then inputs after  $V_{DDQ}$ .  $V_{DDQ}$  limitation is that  $V_{DDQ}$  should not exceed  $V_{DD}$  supply by more than 0.4V during power up.

### Sleep Mode Operation

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin HIGH. During sleep mode, all other inputs are ignored and outputs are brought to a High-Z state. Sleep mode current and output High Z are guaranteed after the specified sleep mode enable time. During sleep mode, the array data contents are preserved. Sleep mode must not be initiated until after all pending operations have completed, as any pending operation is not guaranteed to properly complete after sleep mode is initiated. Sense amp data is lost. Normal operation can be resumed by bringing ZZ low, but only after specified sleep mode recovery time.



Preliminary

IBM041841WLAD  
IBM043641WLAD  
**128K x 36 & 256K x 18 SRAM**

## Ordering Information

Part Number	Organization	Speed	Leads
IBM041841WLAD-3 (Rev D)	256K x 18	2.5ns Access / 3.7 ns Cycle	7 X 17 PBGA
IBM041841WLAD-4 (Rev D)	256K x 18	2.8ns Access / 4.0 ns Cycle	7 X 17 PBGA
IBM041841WLAD-7 (Rev D)	256K x 18	3.5ns Access / 7.0 ns Cycle	7 X 17 PBGA
IBM043641WLAD-3P (Rev D)	128K x 36	2.4ns Access / 3.3 ns Cycle	7 X 17 PBGA
IBM043641WLAD-3 (Rev D)	128K x 36	2.5ns Access / 3.7 ns Cycle	7 X 17 PBGA
IBM043641WLAD-4 (Rev D)	128K x 36	2.8ns Access / 4.0 ns Cycle	7 X 17 PBGA
IBM043641WLAD-5 (Rev D)	128K x 36	2.8ns Access / 5.0 ns Cycle	7 X 17 PBGA
IBM043641WLAD-7 (Rev D)	128K x 36	3.5ns Access / 7.0 ns Cycle	7 X 17 PBGA

## Clock Truth Table

K	ZZ	SS	SW	$\overline{\text{SBW}}_{\text{a}}$	$\overline{\text{SBW}}_{\text{b}}$	$\overline{\text{SBW}}_{\text{c}}$	$\overline{\text{SBW}}_{\text{d}}$	DQ (n)	DQ (n+1)	MODE
L→H	L	L	H	X	X	X	X	X	D <sub>OUT</sub> 0-35	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	X	D <sub>IN</sub> 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	X	D <sub>IN</sub> 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	X	D <sub>IN</sub> 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	X	D <sub>IN</sub> 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	X	D <sub>IN</sub> 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	X	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	X	High-Z	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

## Output Enable Truth Table

Operation	$\overline{\text{G}}$	DQ
Read	L	D <sub>OUT</sub> 0-35
Read	H	High-Z
Sleep (ZZ=H)	X	High-Z
Write ( $\overline{\text{SW}}$ =L)	X	High-Z
Deselect ( $\overline{\text{SS}}$ =H)	X	High-Z

## Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V <sub>DD</sub>	-0.5 to 3.9	V	1
Output Power Supply Voltage	V <sub>DDQ</sub>	V <sub>DD</sub>	V	1
Input Voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5	V	1
Output Voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5	V	1
Operating Temperature	T <sub>J</sub>	0 to +110	°C	1
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C	1
Short Circuit Output Current	I <sub>OUT</sub>	25	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PBGA Thermal Characteristics

Item	Symbol	Rating	Units
Thermal Resistance Junction to Case	R <sub>ΘJC</sub>	1	°C/W

**Recommended DC Operating Conditions** ( $T_A=0$  to  $85^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	$V_{DD}$	3.135	3.3	3.63	V	1
OCD Supply Voltage	$V_{DDQ}$	2.25	3.3	$V_{DD}$	V	1
Input High Voltage	$V_{IH}$	2.0	—	$V_{DD}+0.3$	V	1, 2
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V	1, 3
Output Current	$I_{OUT}$	—	5	8	mA	

1. All voltages referenced to  $V_{SS}$ . All  $V_{DD}$ ,  $V_{DDQ}$  and  $V_{SS}$  pins must be connected.  
2.  $V_{IH}(\text{Max})\text{DC} = V_{DD} + 0.3\text{ V}$ ,  $V_{IH}(\text{Max})\text{AC} = V_{DD} + 1.5\text{ V}$  (pulse width  $\leq 4.0\text{ns}$ ).  
3.  $V_{IL}(\text{Min})\text{DC} = -0.3\text{ V}$ ,  $V_{IL}(\text{Min})\text{AC} = -1.5\text{ V}$  (pulse width  $\leq 4.0\text{ns}$ ).

**PBGA Capacitance** ( $T_A=0$  to  $+85^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} +10/-5\%$ ,  $f=1\text{MHz}$ )

Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	4	pF
Data I/O Capacitance (DQ0-DQ35)	$C_{OUT}$	$V_{OUT} = 0\text{V}$	7	pF

**DC Electrical Characteristics** ( $T_A = 0$  to  $+85^\circ\text{C}$ ,  $V_{DD} = V_{DDQ} = 3.3\text{V} +10/-5\%$  unless otherwise noted)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current - x36 ( $I_{OUT} = 0$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $ZZ$ & $SS = V_{IL}$ )	$I_{DD3.3}$ $I_{DD3.7}$ $I_{DD4}$ $I_{DD5}$ $I_{DD7}$	—	810 750 700 580 450	mA	1
Average Power Supply Operating Current - x18 ( $I_{OUT} = 0$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $ZZ$ & $SS = V_{IL}$ )	$I_{DD3.7}$ $I_{DD4}$ $I_{DD7}$	—	675 625 400	mA	1
Power Supply Standby Current ( $ZZ = V_{IH}$ , All other inputs = $V_{IH}$ or $V_{IL}$ , $I_{OUT} = 0$ )	$I_{SBZZ}$	—	120	mA	1
Power Supply Standby Current ( $SS = V_{IH}$ , $ZZ = V_{IL}$ , All other inputs = $V_{IH}$ or $V_{IL}$ , $I_{OUT} = 0$ )	$I_{SBSS}$	—	150	mA	
Input Leakage Current, any input ( $V_{IN} = V_{SS}$ or $V_{DD}$ )	$I_{LI}$	—	+1	$\mu\text{A}$	
Output Leakage Current ( $V_{OUT} = V_{SS}$ to $3.0\text{V}$ , DQ in High-Z) ( $V_{OUT} = 3.0\text{V}$ to $V_{DD}$ max, DQ in High-Z)	$I_{LO1}$ $I_{LO2}$	—	+6 +100	$\mu\text{A}$ $\mu\text{A}$	
Output High "H" Level Voltage ( $I_{OH} = -8\text{mA}$ @ $2.4\text{V}$ for $V_{DDQ} = 3.3\text{V}$ )	$V_{OH}$	2.4	—	V	
Output Low "L" Level Voltage ( $I_{OL} = +8\text{mA}$ @ $0.4\text{V}$ for $V_{DDQ} = 3.3\text{V}$ )	$V_{OL}$	—	0.4	V	
Output High "H" Level Voltage ( $I_{OH} = -8\text{mA}$ @ $1.6\text{V}$ for $V_{DDQ} = 2.5\text{V}$ )	$V_{OH}$	1.6	—	V	
Output Low "L" Level Voltage ( $I_{OL} = +8\text{mA}$ @ $0.4\text{V}$ for $V_{DDQ} = 2.5\text{V}$ )	$V_{OL}$	—	0.4	V	

1.  $I_{OUT}$  = Chip Output Current.  $I_{DD4}$  means current at 4ns cycle time for example



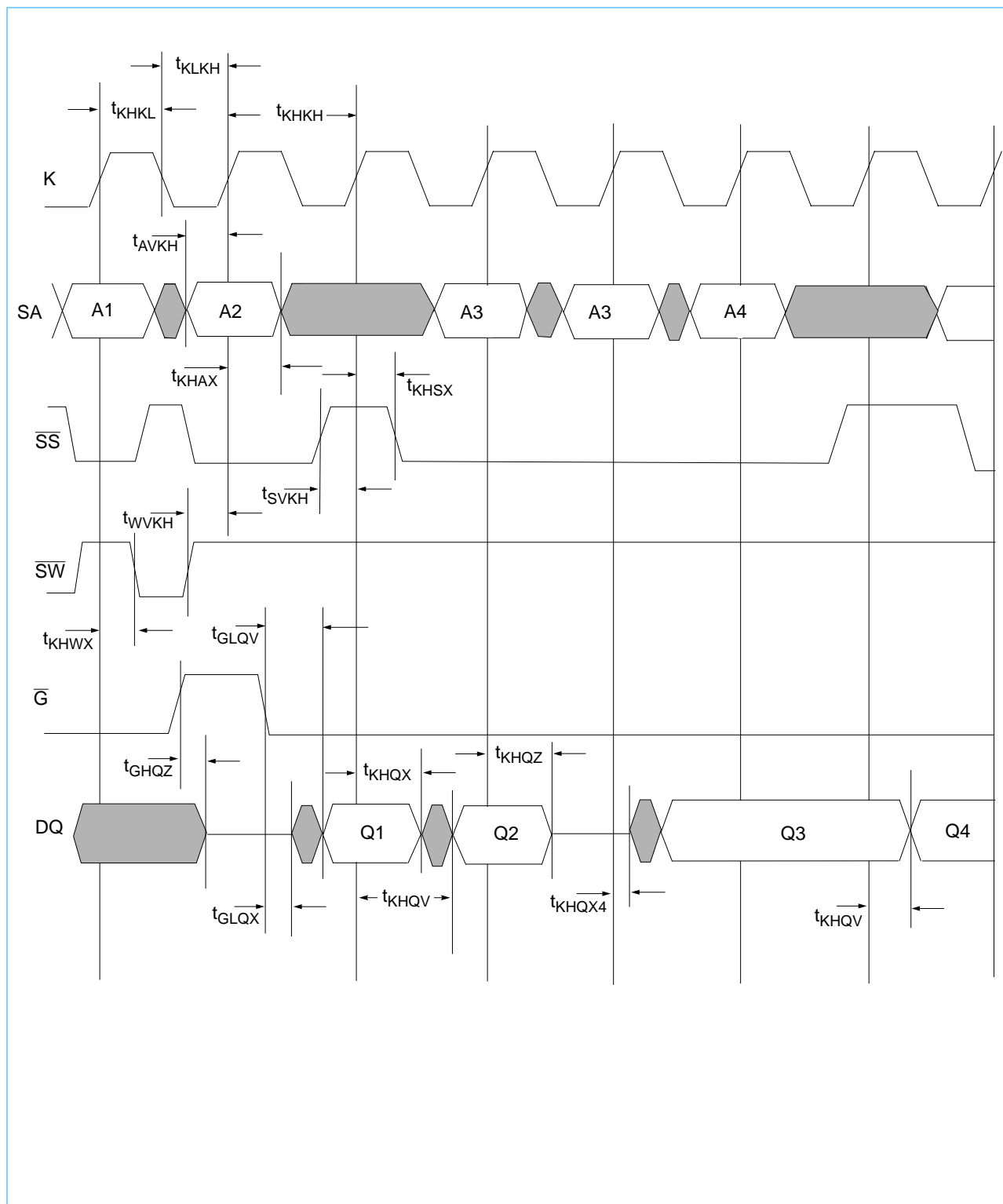


**AC Characteristics** ( $T_A=0$  to  $+85^{\circ}\text{C}$ ,  $V_{DD}=3.3 \pm 10\%$  V,  $V_{DDQ}=2.5 \pm 5\%$  V)

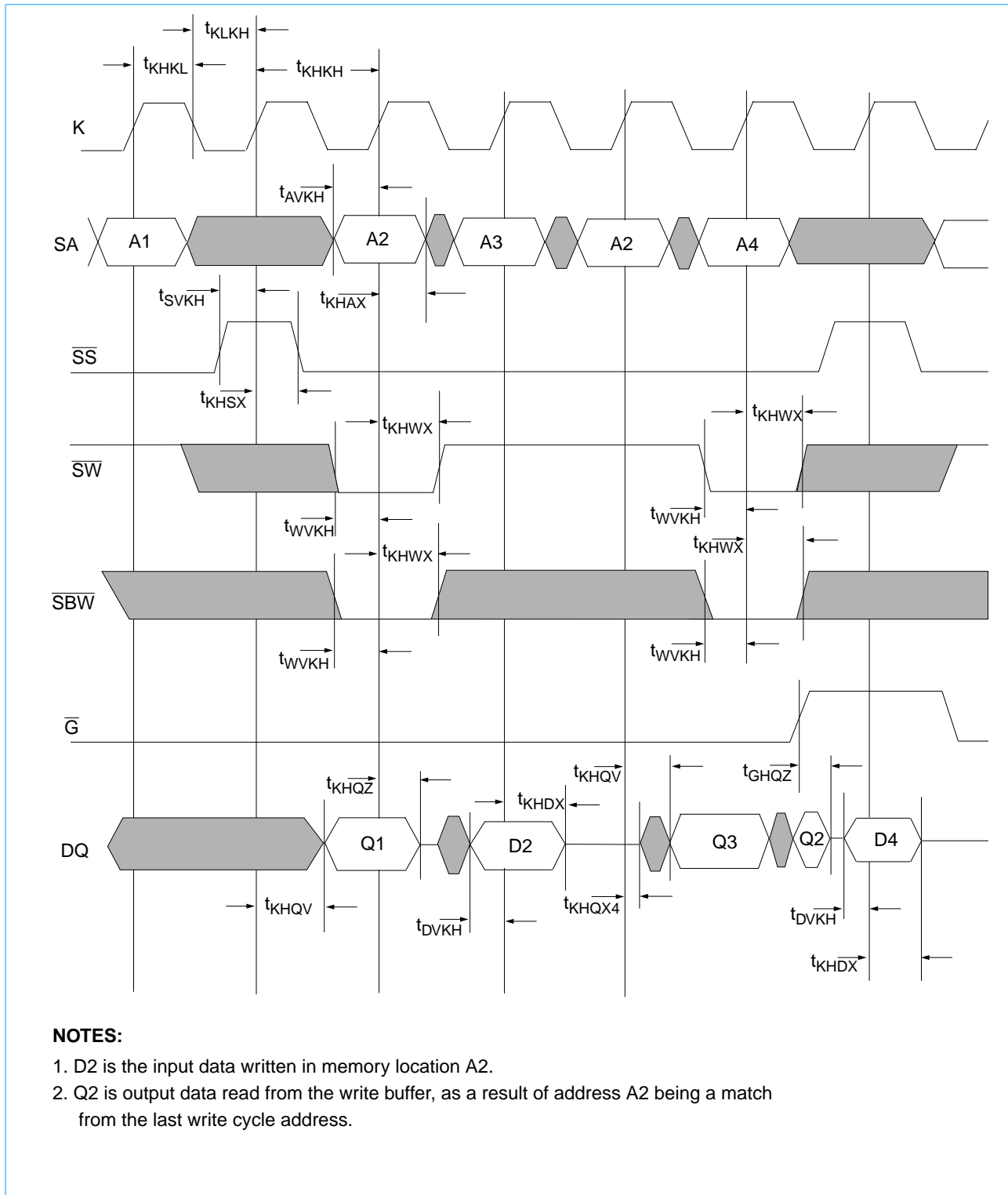
Parameter	Symbol	-3P(x36 only)		-3		-4		-5(x36 only)		-7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	$t_{KHKH}$	3.3	—	3.7	—	4.0	—	5.0	—	7.0	—	ns	
Clock High Pulse Width	$t_{KHKL}$	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
Clock Low Pulse Width	$t_{KLKH}$	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
Clock to Output Valid	$t_{KHQV}$	—	2.4	—	2.5	—	2.8	—	2.8	—	3.5	ns	1
Address Setup Time	$t_{AVKH}$	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Address Hold Time	$t_{KHAX}$	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Sync Select Setup Time	$t_{SVKH}$	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Sync Select Hold Time	$t_{KHSX}$	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Write Enables Setup Time	$t_{WVKH}$	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Write Enables Hold Time	$t_{KHWX}$	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Data In Setup Time	$t_{DVKH}$	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Data In Hold Time	$t_{KHDX}$	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Data Out Hold Time	$t_{KHQX}$	0.5	—	0.7	—	0.7	—	0.7	—	0.7	—	ns	1
Clock High to Output High-Z	$t_{KHQZ}$	—	2.5	—	2.5	—	2.5	—	2.5	—	3.5	ns	1, 2
Clock High to Output Active	$t_{KHQX4}$	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	1, 2
Output Enable to High-Z	$t_{GHQZ}$	—	2.5	—	2.5	—	2.5	—	2.5	—	3.5	ns	1, 2
Output Enable to Low-Z	$t_{GLQX}$	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	1, 2
Output Enable to Output Valid	$t_{GLQV}$	—	2.5	—	2.5	—	2.5	—	2.5	—	3.5	ns	1
Sleep Mode Recovery Time	$t_{ZZR}$	3.3	—	3.7	—	4	—	5	—	7	—	ns	3
Sleep Mode Enable Time	$t_{ZZE}$	—	3.3	—	3.7	—	4	—	5	—	7	ns	3

1. See AC Test Loading on page 8.  
 2. Verified by design and tested without guardband.  
 3. This specification is for No Data Retention. For data integrity at least 200ns of Recovery Time is recommended coupled with a 0.5ns Set-up time around K clock.

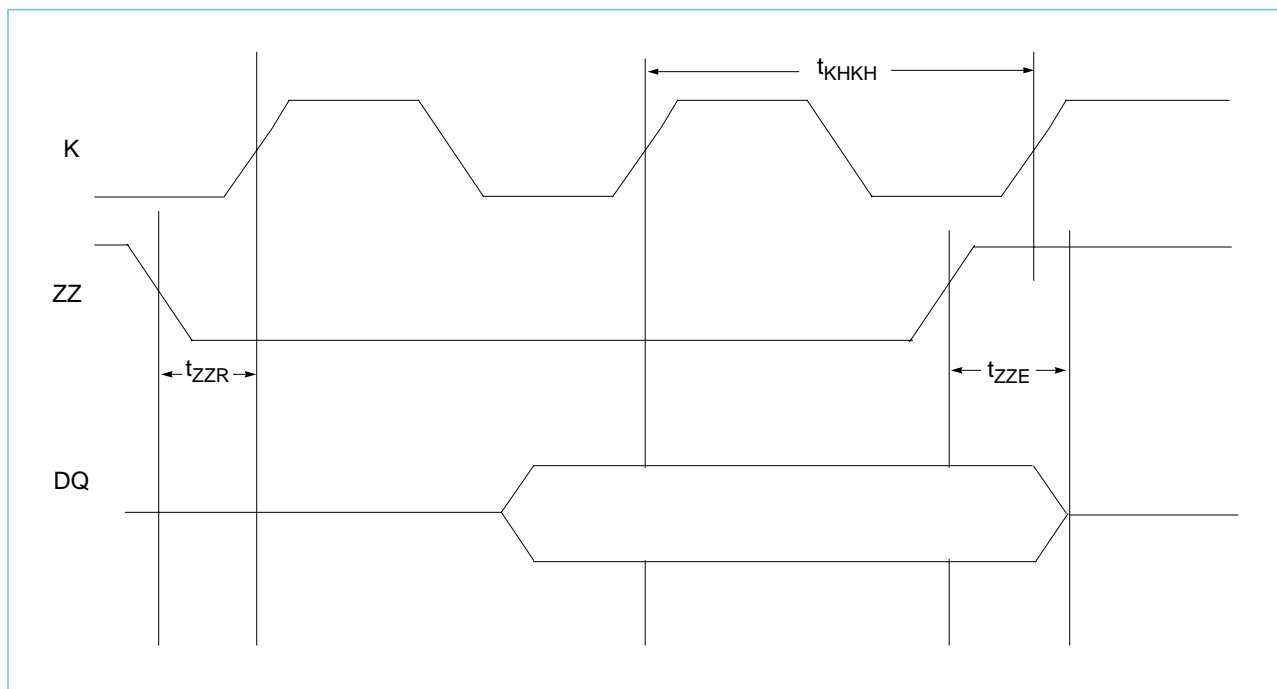
## Timing Diagram (Read and Deselect Cycles)



## Timing Diagram (Read Write Cycles)



## Timing Diagram (Sleep Mode)





## IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAM contains a TAP controller, Instruction register, Boundary Scan register, Bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required.

### Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

**Caution:** TCK, TMS, and TDI must be tied down, even when JTAG is not used. TCK tied off will not allow any data to be clocked in, however.

### JTAG Recommended DC Operating Conditions ( $T_A=0$ to $85^{\circ}\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	$V_{IH1}$	2.2	—	$V_{DD}+0.3$	V	1
JTAG Input Low Voltage	$V_{IL1}$	-0.3	—	0.8	V	1
JTAG Output High Level	$V_{OH1}$	2.4	—	—	V	1, 2
JTAG Output Low Level	$V_{OL1}$	—	—	0.4	V	1, 3

1. All JTAG Inputs and Outputs are LVTTTL Compatible only.
2.  $I_{OH1} = -8\text{mA}$  at 2.4V.
3.  $I_{OL1} = +8\text{mA}$  at 0.4V.

### JTAG AC Test Conditions ( $T_A=0$ to $+85^{\circ}\text{C}$ , $V_{DD}=3.3\text{V} \pm 10\%$ / $-5\%$ )

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	$V_{IH1}$	3.0	V	
Input Pulse Low Level	$V_{IL1}$	0.0	V	
Input Rise Time	$T_{R1}$	2.0	ns	
Input Fall Time	$T_{F1}$	2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

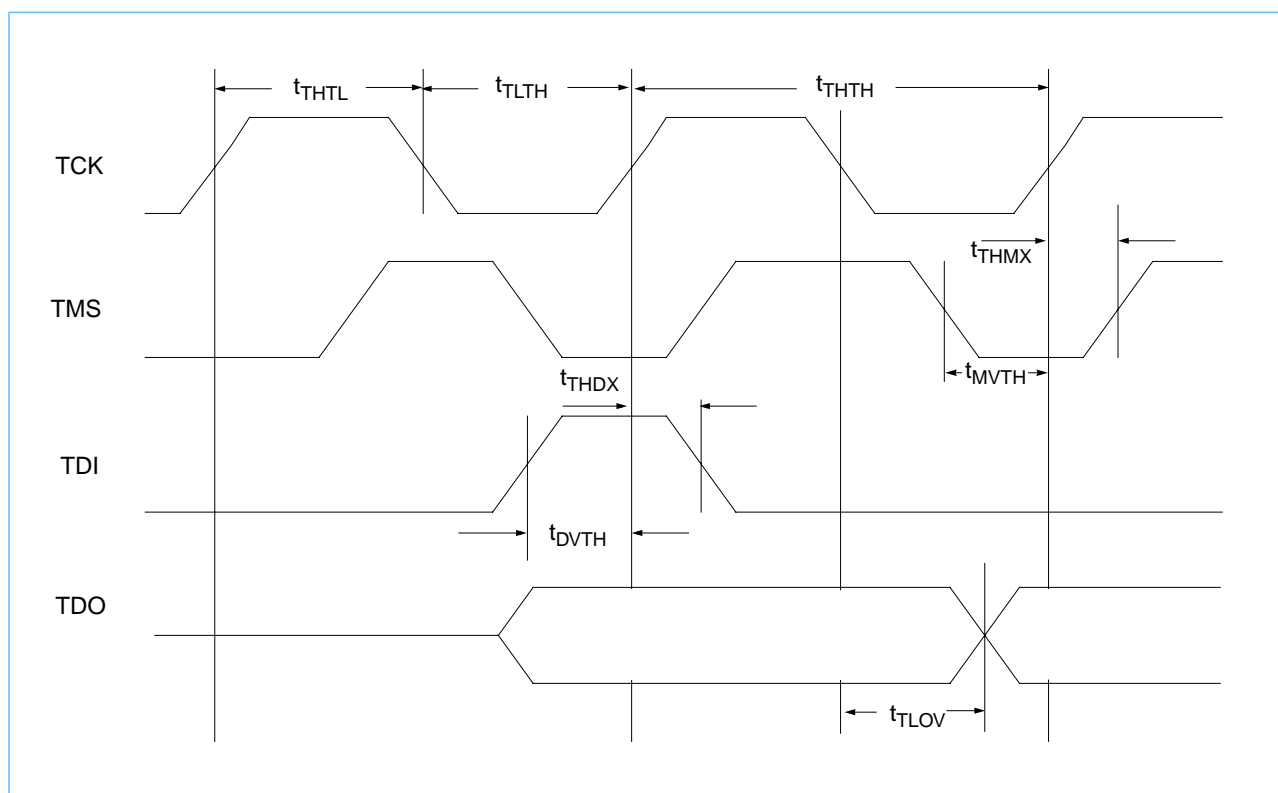
1. See AC Test Loading on page 8.

## JTAG AC Characteristics ( $T_A=0$ to $+85^{\circ}\text{C}$ , $V_{DD}=3.3\text{V} \pm 10\%$ )

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	$t_{\text{THTH}}$	20	—	ns	
TCK High Pulse Width	$t_{\text{HTHL}}$	7	—	ns	
TCK Low Pulse Width	$t_{\text{LTH}}$	7	—	ns	
TMS Setup	$t_{\text{MVTH}}$	4	—	ns	
TMS Hold	$t_{\text{THMX}}$	4	—	ns	
TDI Setup	$t_{\text{DVTH}}$	4	—	ns	
TDI Hold	$t_{\text{THDX}}$	4	—	ns	
TCK Low to Valid Data	$t_{\text{TLOV}}$	—	7	ns	1

1. See AC Test Loading on page 8.

## JTAG Timing Diagram





## Scan Register Definition

Register Name	Bit Size X18	Bit Size X36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

\* The Boundary Scan chain consists of the following bits:

- 36 or 18 bits for Data Inputs Depending on X18 or X36 Configuration
- 17 bits for SA0 - SA16 for X36, 18 bits for SA0 - SA17 for X18
- 4 bits for SBW<sub>a</sub> - SBW<sub>d</sub> in X36, 2 bits for SBW<sub>a</sub> and SBW<sub>b</sub> in X18
- 8 bits for K,  $\bar{K}$ , SS,  $\bar{G}$ ,  $\bar{S}$ W, ZZ, M1 and M2
- 5 bits for Place Holders

\* K and  $\bar{K}$  clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

## ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit(0)
256K X18	0001	011 100 1011	001111	000 101 001 00	1
128K X36	0001	011 010 1100	001111	000 101 001 00	1

## Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	2
010	SAMPLE-Z	1
011	PRIVATE	5
100	SAMPLE	4
101	PRIVATE	5
110	PRIVATE	5
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V<sub>SS</sub> when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. This instruction is reserved for the exclusive use of IBM. Invoking this instruction may cause improper SRAM functionality.

### List of IEEE 1149.1 standard violations:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 6.1.1.d

## Boundary Scan Order (x36) (PH =Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2=V <sub>DD</sub>	5R	25	DQ13	6F	49	DQ26	2H
2	SA1	4P	26	DQ11	7E	50	DQ25	1H
3	SA2	4T	27	DQ12	6E	51	$\overline{\text{SBWc}}$	3G
4	SA12	6R	28	DQ9	7D	52	ZQ= 0 (PH)	4D
5	SA13	5T	29	DQ10	6D	53	SS	4E
6	ZZ	7T	30	SA14	6A	54	C=0 <sup>2</sup>	4G
7	DQ1	6P	31	SA15	6C	55	C=1 <sup>2</sup>	4H
8	DQ0	7P	32	SA10	5C	56	SW	4M
9	DQ3	6N	33	SA16	5A	57	$\overline{\text{SBWd}}$	3L
10	DQ2	7N	34	PH <sup>1</sup>	6B	58	DQ34	1K
11	DQ4	6M	35	SA11	5B	59	DQ35	2K
12	DQ6	6L	36	SA8	3B	60	DQ32	1L
13	DQ5	7L	37	PH <sup>1</sup>	2B	61	DQ33	2L
14	DQ8	6K	38	SA7	3A	62	DQ31	2M
15	DQ7	7K	39	SA9	3C	63	DQ29	1N
16	$\overline{\text{SBWa}}$	5L	40	SA6	2C	64	DQ30	2N
17	$\overline{\text{K}}$	4L	41	SA5	2A	65	DQ27	1P
18	K	4K	42	DQ19	2D	66	DQ28	2P
19	G	4F	43	DQ18	1D	67	SA3	3T
20	SBWb	5G	44	DQ21	2E	68	SA4	2R
21	DQ16	7H	45	DQ20	1E	69	SA0	4N
22	DQ17	6H	46	DQ22	2F	70	M1=V <sub>ss</sub>	3R
23	DQ14	7G	47	DQ24	2G			
24	DQ15	6G	48	DQ23	1G			

1. Input of PH register connected to V<sub>SS</sub>.
2. Balls 4G and 4H are unused C Clock pins in this application.

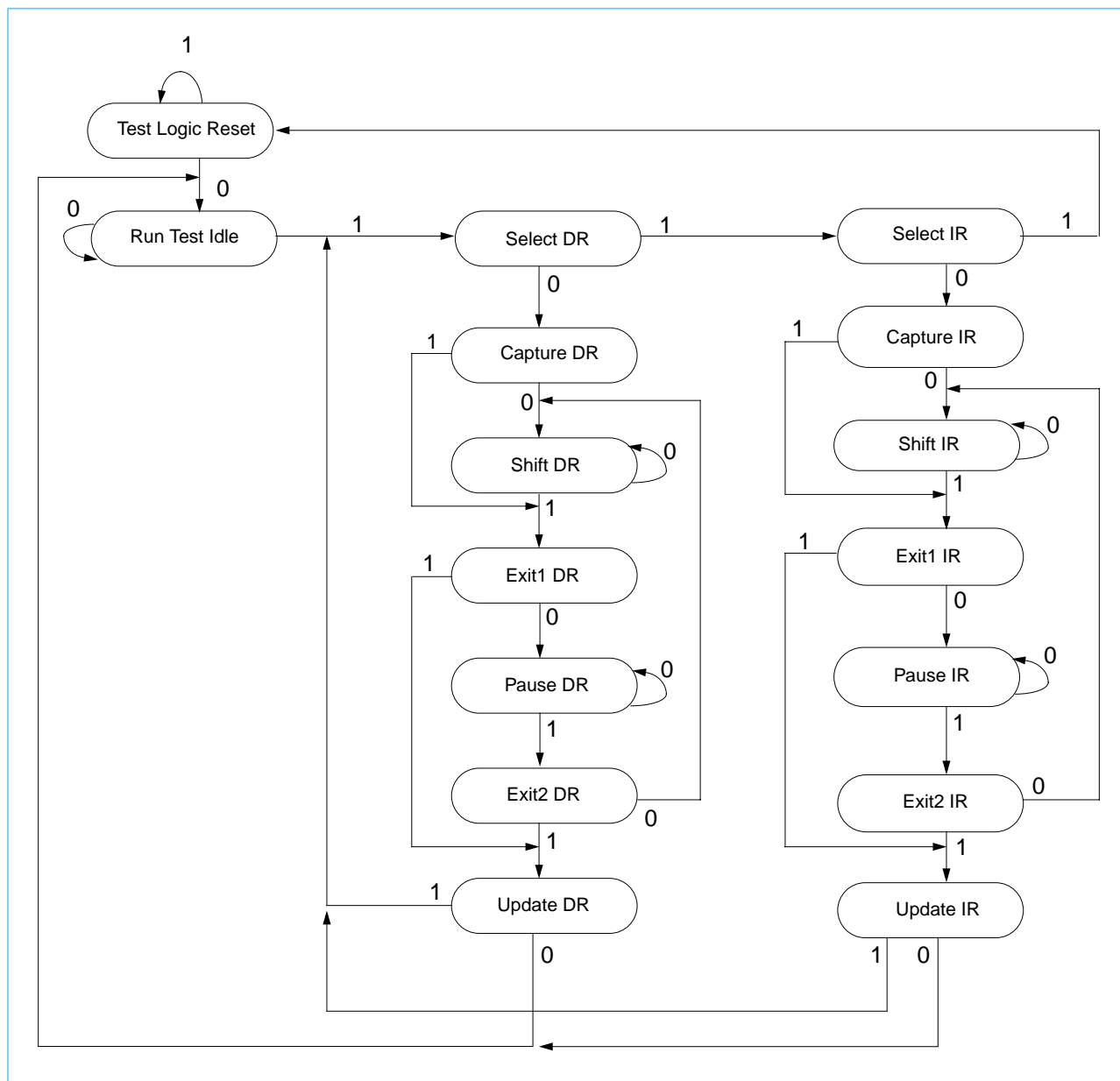


**Boundary Scan Order (x18)** (PH =Place Holder)

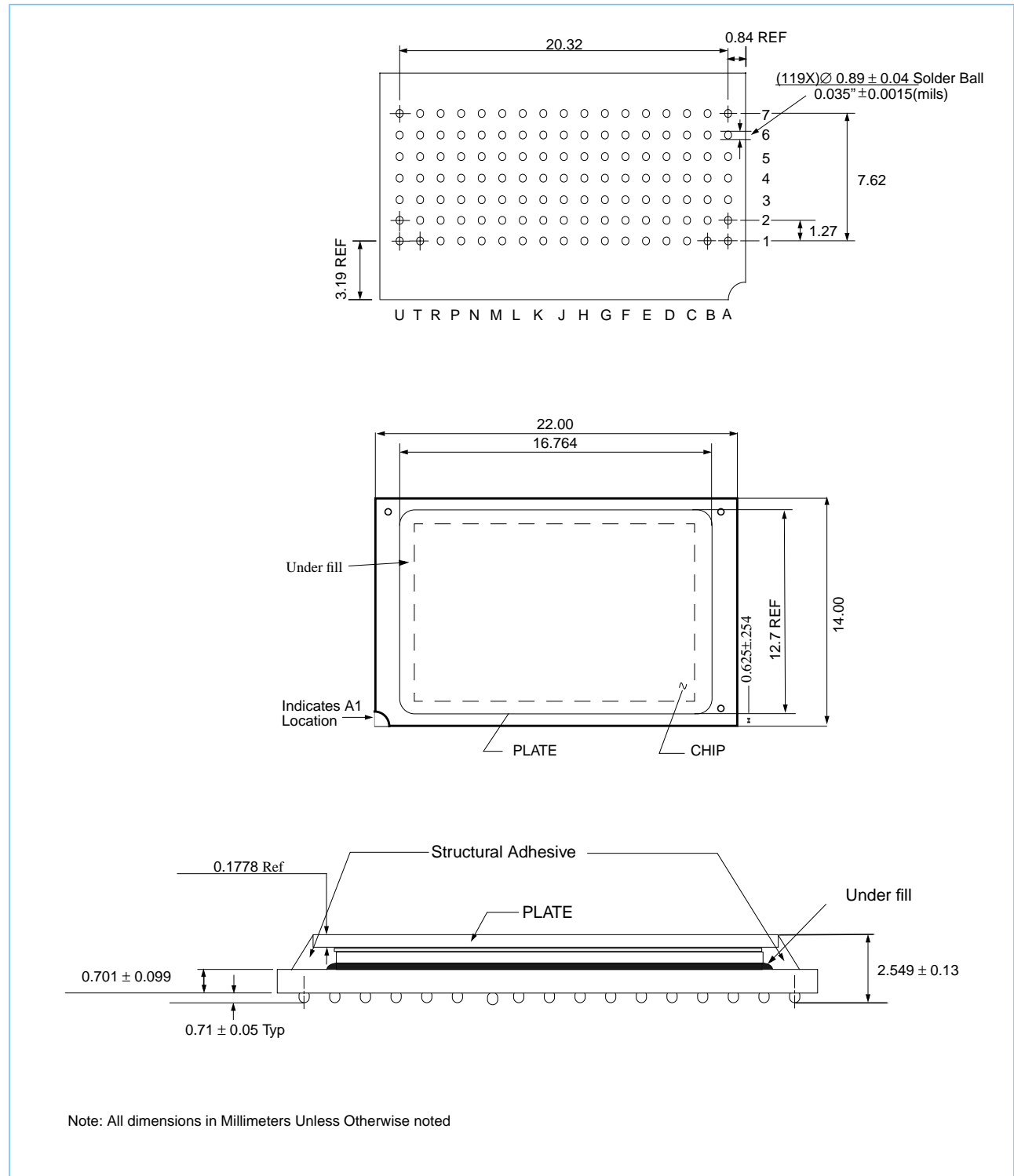
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2=V <sub>DD</sub>	5R	27	PH <sup>1</sup>	2B
2	SA12	6T	28	SA7	3A
3	SA1	4P	29	SA9	3C
4	SA13	6R	30	SA6	2C
5	SA17	5T	31	SA5	2A
6	ZZ	7T	32	DQ9	1D
7	DQ0	7P	33	DQ12	2E
8	DQ3	6N	34	DQ15	2G
9	DQ6	6L	35	DQ16	1H
10	DQ7	7K	36	$\overline{\text{SBWb}}$	3G
11	$\overline{\text{SBWa}}$	5L	37	ZQ= 0 (PH)	4D
12	$\overline{\text{K}}$	4L	38	SS	4E
13	K	4K	39	C=0 <sup>2</sup>	4G
14	G	4F	40	C=1 <sup>2</sup>	4H
15	DQ8	6H	41	SW	4M
16	DQ5	7G	42	DQ17	2K
17	DQ4	6F	43	DQ14	1L
18	DQ2	7E	44	DQ13	2M
19	DQ1	6D	45	DQ11	1N
20	SA14	6A	46	DQ10	2P
21	SA15	6C	47	SA3	3T
22	SA10	5C	48	SA4	2R
23	SA16	5A	49	SA0	4N
24	PH <sup>1</sup>	6B	50	SA2	2T
25	SA11	5B	51	M1=V <sub>ss</sub>	3R
26	SA8	3B			

1. Input of PH register connected to V<sub>SS</sub>.
2. Balls 4G and 4H are unused C Clock pins in this application.

## TAP Controller State Machine



## 7 x 17 PBGA Dimensions



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## References Rev "D" - Last Character in Part Number (D)

The following documents give recommendations, restrictions and limitations for 2nd level attach process:

C4 SRAM Assembly Guide for Single Sided Assembly

Double Sided 4Meg Coupled Cap PBGA Card Assembly Guide

There is qualification information, including scope of application conditions qualified, available from your marketing representative.



Preliminary

IBM041841WLAD  
IBM043641WLAD  
128K x 36 & 256K x 18 SRAM

## Revision Log

Rev	Contents of Modification
9/97	Initial Release.
5/98	Added CBGA parts. Updated -3P sort and capacitance numbers. Updated output leakage #. Also nomenclature about tri-state test in AC characteristics - test did not change.
6/98	Updated PBGA mechanical drawing and references. Changed part numbers from Rev "B" to Rev "D". Removed Ceramic information. Minor definition to boundary scan.
11/98	Changed Tkhqx for -3P part from 0.7 to 0.5ns.
02/99	Tightened the BGA ball diameter tolerance.



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