TARGET SPECIFICATION

TRAILBLAZER

IS82C600 — Virtual Dual-Port SRAM

GENERAL DESCRIPTION

The TrailBlazer Virtual Dual Port (VDP) SRAM simplifies DSP-based system design and layout, providing no-wait-state performance up to 120 MHz, along with the convenience of a dual-ported interface. And in many cases, TrailBlazer allows existing system designs to be easily upgraded, enabling the reuse of available ASICs and logic designs.

A key benefit of the TrailBlazer device is its ability to interface easily to high-performance DSPs taking advantage of minimum impedance, point-to-point interconnect between the DSP and SRAM. Together with access times as fast as 7 ns, this allows the DSP to operate at maximum frequency with no-wait-states up to 120 MHz. Also, it eases PCB timing and layout related considerations and simplifies layout, often allowing a reduction in the number of PC board layers.

FEATURES

- **Virtual dual-port (VDP) SRAM**
- **Seamless interface to Texas Instruments' '5x and '54x high-speed DSPs**
- **Zero wait-state performance up to 120 MHz on the primary DSP port**
  - — Point-to-point interface between the SRAM and the high-speed DSP
- **Integrates the single ported SRAM with a dual ported interface**
  - — 7 ns access time to the SRAM
  - — TrailBlazer can be used as a stand alone high-speed SRAM
- **Integrates the DSP port to DSP port bridge function**
  - — Broadcasts all DSP cycles from primary DSP port to the secondary DSP port
    - Programmability to only broadcast non-SRAM cycles to the secondary DSP port
  - — Programmability to "divide" the memory into six segments, corresponding to the six regions of TI DSPs
    - The upper/lower halves of Data Space ($\overline{DS}$), the upper/lower halves of Program Space ($\overline{PS}$) and the upper/lower halves of I/O Space ($\overline{IS}$).
    - Programmability to insert wait states to the memory space (TI DSPs can only program wait states for all of I/O Space)
  - — Supports existing, slower DSP peripheral control devices on the secondary DSP port
  - — "No glue logic" interface for local peripherals on the secondary DSP poprt
  - — 12 chip selects, six on the primary DSP port and six on the secondary DSP port
  - — Allows the DSP to access the devices on the secondary port
  - — Supports bootable ROM on the secondary or primary port
  - — Allows the Shadowing of the ROM on the secondary port into the on-board SRAM
- **Supports dual DSP designs**
  - — Provides high-speed SRAM access on both DSP ports
  - — Programmable to be local or global memory of the DSPs
  - — Programmable "software locked" operations
  - — Programmable Master/Slave configuration for the dual-ported SRAM access
  - — Allows local port concurrency for each DSP
  - — $\overline{XCVR}$ pin allows device to be a transceiver for the DMA transfers between two DSPs
- **Allows dynamic reallocation of memory space for transparent block moves**
  - — Large blocks of data can be "transparently" moved from data space to program space and back by reprogramming mode bits

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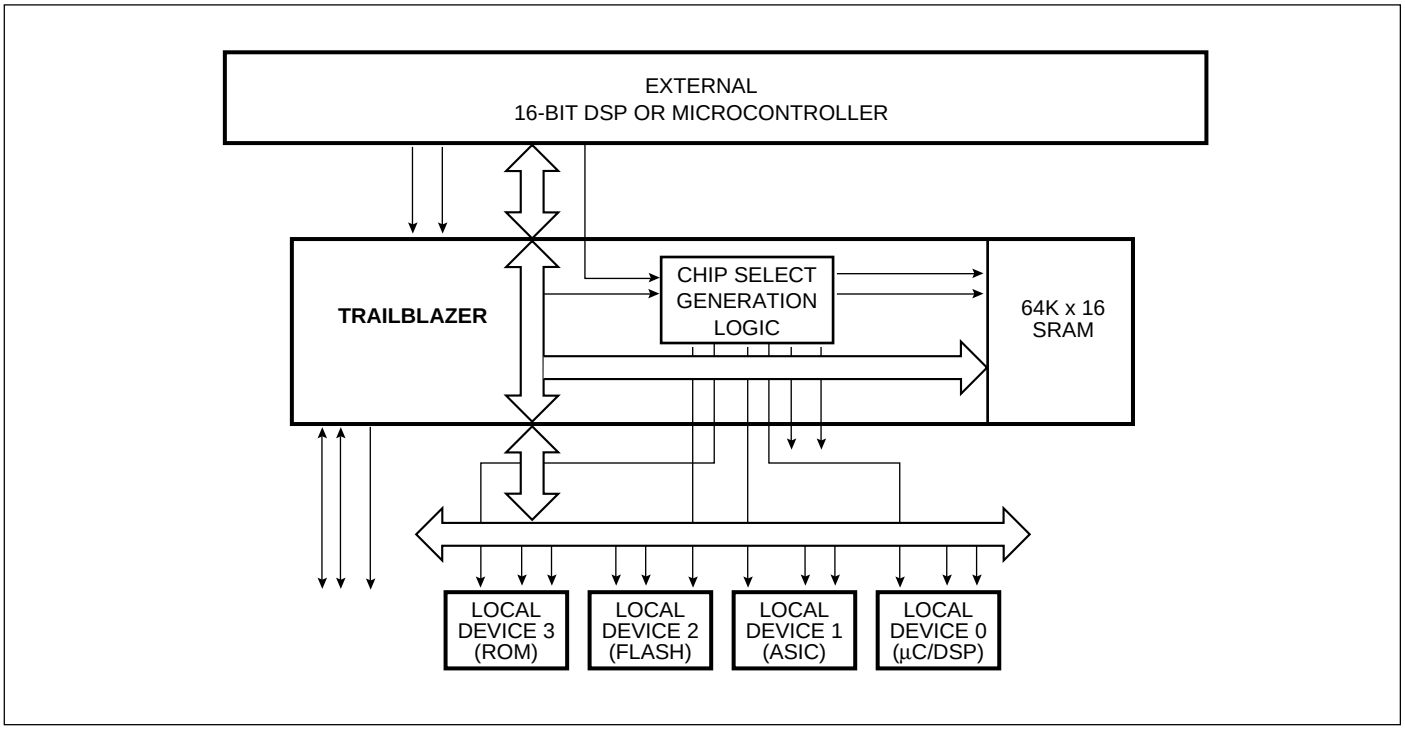
Product Overview

TrailBlazer, Virtual Dual-Ported SRAM, integrates the high-speed dual ported SRAM with a DSP port to DSP port bridge function to the high-speed DSP designs. This provides 7 ns access times to the DSP on the primary port that enables low cost implementation of the 120 MHz DSP system.

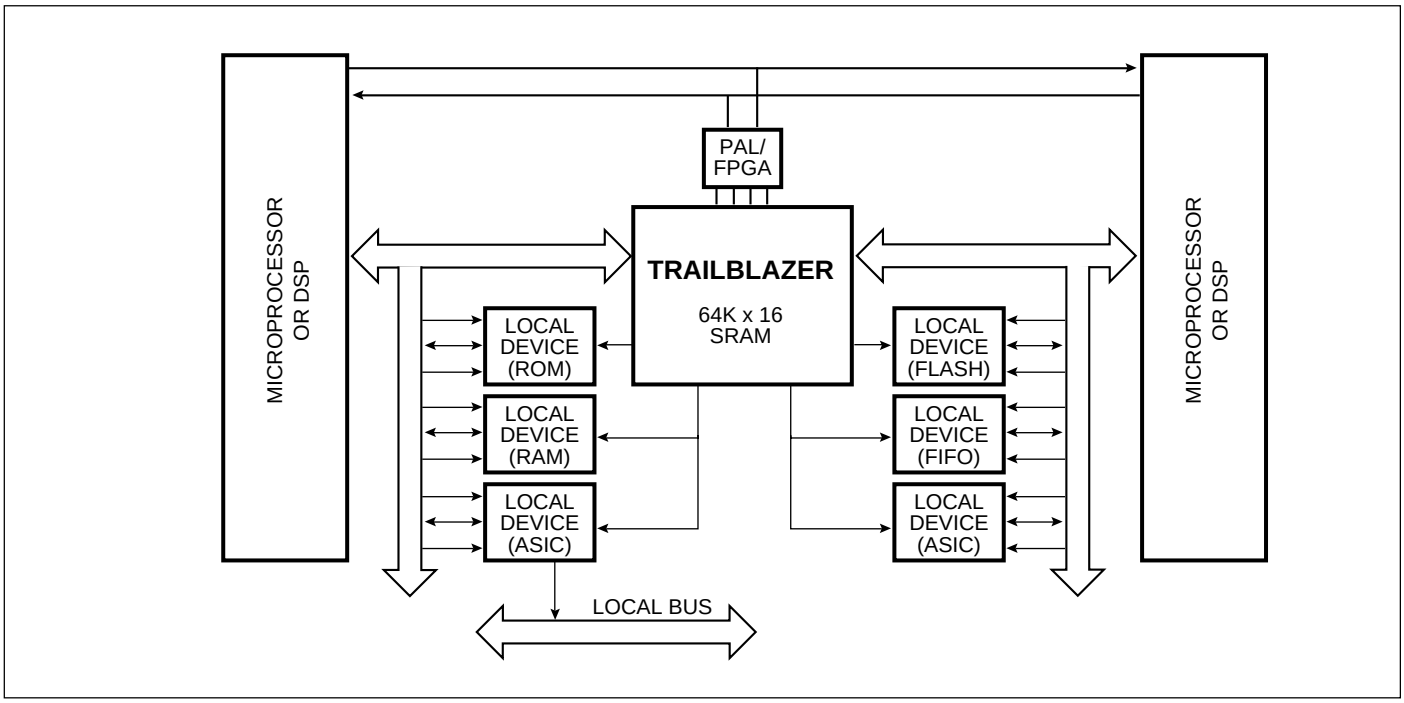
TrailBlazer combines a high-performance, single ported memory array with two-ported interface logic to enable maximum performance and flexibility while keeping costs at a minimum. In order to simplify system development, TrailBlazer duplicates the DSP bus signals on its second port to permit the use of existing system solutions and ASICs with a new generation of higher frequency DSPs. On its primary port, TrailBlazer provides a high-speed SRAM interface to the DSP and then broadcasts DSP cycles to its secondary port allowing the DSP to access peripherals. Since the peripherals are accessed using the same signals, in may cases existing ASICs can be re-used.

TrailBlazer provides an optimized, seamless interface to TI ‘5x and ’54x high speed DSPs along with a “no glue logic” interface for local peripherals on the second port; up to 12 chip select outputs are provided. If desired, TrailBlazer can turn off broadcast of DSP cycles to its second port which can save considerable system power at high frequency.

TrailBlazer can also be used as local or global memory for a two DSP or microcontroller system; chip select logic on each port allows the same data to be accessed at different locations in memory if desired.



TrailBlazer System Block Diagram with High-Speed DSP on the Primary Port and the Slower Existing DSP System Components on the Secondary Port



TrailBlazer System Block Diagram showing a Dual DSP System

PIN CONFIGURATION: 119-pin PBGA

	1	2	3	4	5	6	7
A	$\overline{\text{CSMEMp3}}$	$\overline{\text{CSMEMp5}}$	Ap4	Ap5	Ap11	$\overline{\text{XCVR}}$	$\overline{\text{ISp}}$
B	$\overline{\text{CSMEMp2}}$	$\overline{\text{CSMEMp4}}$	Ap3	Ap6	Ap12	$\overline{\text{PSp}}$	$\overline{\text{DSp}}$
C	$\overline{\text{CSMEMp0}}$	$\overline{\text{CSMEMp1}}$	Ap2	Ap7	Ap13	Dp0	Dp1
D	Ds1	Ds0	Ap1	Ap8	Ap14	Dp2	Dp3
E	Ds3	Ds2	Ap0	Ap9	Ap15	Dp4	Dp5
F	Ds4	GND	GND_Q	Ap10	GND_Q	V_{CC}	Dp6
G	Ds7	Ds6	Ds5	Dp7	$\overline{\text{HOLDAp}}$	$\overline{\text{CSINTp}}$	$\overline{\text{RWp}}$
H	$\overline{\text{OEMEMp}}$	GND_Q	$\overline{\text{WEMEMp}}$	V_{CCQ}	$\overline{\text{RDp}}$	GND_Q	$\overline{\text{IOSTRBp}}$
J	Ds8	$\overline{\text{OEMEMs}}$	V_{CCQ}	V_{CCQ}	$\overline{\text{WEs}}$	$\overline{\text{WEp}}$	$\overline{\text{MSTRBp}}$
K	Ds9	GND_Q	$\overline{\text{WEMEMs}}$	V_{CCQ}	$\overline{\text{IOSTRBs}}$	GND_Q	$\overline{\text{MSTRBs}}$
L	Ds10	Ds11	As1	As7	$\overline{\text{CSINTs}}$	$\overline{\text{RWs}}$	$\overline{\text{RDs}}$
M	Ds12	GND	GND_Q	As8	GND_Q	GND	$\overline{\text{HOLDAs}}$
N	Ds13	Ds14	As2	As9	Dp10	Dp9	Dp8
P	Ds15	$\overline{\text{CSMEMs0}}$	As3	As10	Dp13	Dp12	Dp11
R	$\overline{\text{CSMEMs1}}$	$\overline{\text{CSMEMs2}}$	As4	As11	$\overline{\text{PRGM}}$	$\overline{\text{DSs}}$	Dp14
T	$\overline{\text{CSMEMs3}}$	$\overline{\text{CSMEMs5}}$	As5	As12	As15	$\overline{\text{ISs}}$	Dp15
U	$\overline{\text{CSMEMs4}}$	As0	As6	As13	As14	$\overline{\text{PSs}}$	NC

DETAILED PIN DESCRIPTION

Table 1. Primary Side Pins

Pin Name	Pin Count	Pin Type	Pin Description
Ap[15:0]	16	I/O	**ADDRESS:** Address pins that connect to the primary side DSP or microcontroller.
Dp[15:0]	16	I/O	**DATA:** Data pins that connect to the primary side DSP or microcontroller.
$\overline{\text{RDp}}$	1	I/O	**READ STROBE:** Enables a read on the primary side.
$\overline{\text{WEp}}$	1	I/O	**WRITE STROBE:** Enables a write on the primary side.
$\overline{\text{IOSTRBp}}$	1	I/O	**I/O STROBE:** Enables I/O access on the primary side.
$\overline{\text{MSTRBp}}$	1	I/O	**MEMORY (DATA) STROBE:** Memory access on the primary side.
$\overline{\text{PSp}}$	1	I/O	**PROGRAM SPACE SELECT:** Selects Program Space on the primary side.
$\overline{\text{DSp}}$	1	I/O	**DATA SPACE SELECT:** Selects Data Space on the primary side.
$\overline{\text{ISp}}$	1	I/O	**I/O SPACE SELECT:** Selects I/O Space on the primary side.
$\overline{\text{RWp}}$	1	I/O	**READ/WRITE:** Indicates a Read or Write Cycle on the primary side.
$\overline{\text{HOLDAp}}$	1	I	**HOLD ACKNOWLEDGE:** Indicates primary side is relinguishing control of TrailBlazer.
$\overline{\text{CSINTp}}$	1	I	**INTERNAL SRAM CHIP SELECT:** When asserted, it overrides any MODE configuration.
$\overline{\text{CSMEMp}}$[5:0]	6	O	**EXTERNAL MEMORY CHIP SELECTS:** Based on the 6-32K memory regions.
$\overline{\text{WEMEMp}}$	1	O	**EXTERNAL MEMORY WRITE ENABLE:** Based on the 6-32K memory regions.
$\overline{\text{OEMEMp}}$	1	O	**EXTERNAL MEMORY OUTPUT ENABLE:** Based on the 6-32K memory regions.

Table 2. Secondary Side Pins

Pin Name	Pin Count	Pin Type	Pin Description
As[15:0]	16	I/O	**ADDRESS:** Address pins that connect to the secondary side DSP or microcontroller.
Ds[15:0]	16	I/O	**DATA:** Data pins that connect to the secondary side DSP or microcontroller.
$\overline{\text{RDs}}$	1	I/O	**READ STROBE:** Enables a read on the secondary side.
$\overline{\text{WEs}}$	1	I/O	**WRITE STROBE:** Enables a write on the secondary side.
$\overline{\text{IOSTRBs}}$	1	I/O	**I/O STROBE:** Enables I/O access on the secondary side.
$\overline{\text{MSTRBs}}$	1	I/O	**MEMORY (DATA) STROBE:** Memory access on the secondary side.
$\overline{\text{PSs}}$	1	I/O	**PROGRAM SPACE SELECT:** Selects Program Space on the secondary side.
$\overline{\text{DSs}}$	1	I/O	**DATA SPACE SELECT:** Selects Data Space on the secondary side.
$\overline{\text{ISs}}$	1	I/O	**I/O SPACE SELECT:** Selects I/O Space on the secondary side.
$\overline{\text{RWs}}$	1	I/O	**READ/WRITE:** Indicates a Read or Write Cycle on the secondary side.
$\overline{\text{HOLDAs}}$	1	I	**HOLD ACKNOWLEDGE:** Indicates secondary side is relinguishing control of TrailBlazer.
$\overline{\text{CSINTs}}$	1	I	**INTERNAL SRAM CHIP SELECT:** When asserted, it overrides any MODE configuration.
$\overline{\text{CSMEMs}}$[5:0]	6	O	**EXTERNAL MEMORY CHIP SELECTS:** Based on the 6-32K memory regions.
$\overline{\text{WEMEMs}}$	1	O	**EXTERNAL MEMORY WRITE ENABLE:** Based on the 6-32K memory regions.
$\overline{\text{OEMEMs}}$	1	O	**EXTERNAL MEMORY OUTPUT ENABLE:** Based on the 6-32K memory regions.

Table 3. Miscellaneous Pins

Pin Name	Pin Count	Pin Type	Pin Description
$\overline{\text{PRGM}}$	1	I	**PROGRAM ENABLE**: This pin latches the As[15:0] bus to determine the MODEp[7:0] and MODEs[7:0] registers.
$\overline{\text{XCVR}}$	1	I	**TRANSCEIVER MODE:** This pin puts TrailBlazer device into a transceiver-like mode, supports internal DSP DMA through the TrailBlazer.