Data Sheet

JUNE 2000
Revision 0.2

IXF6401

Broadband Access Processor

General Description

Flexibility, scalability, effficiency & integration of different traffic types for a single network is the beauty of the IXF6401 Broadband Access Processor. Enabling ease of OEM development, the IXF6401 provides industry standard interfaces for 64-bit/66 Mhz PCI Bus, 64-bit SSRAM/SDRAM Local Memory (LM) Bus and UTOPIA levels 1, 2 ATM & POS interfaces for direct coupling of a broad range of Layer 1 physical interfaces.

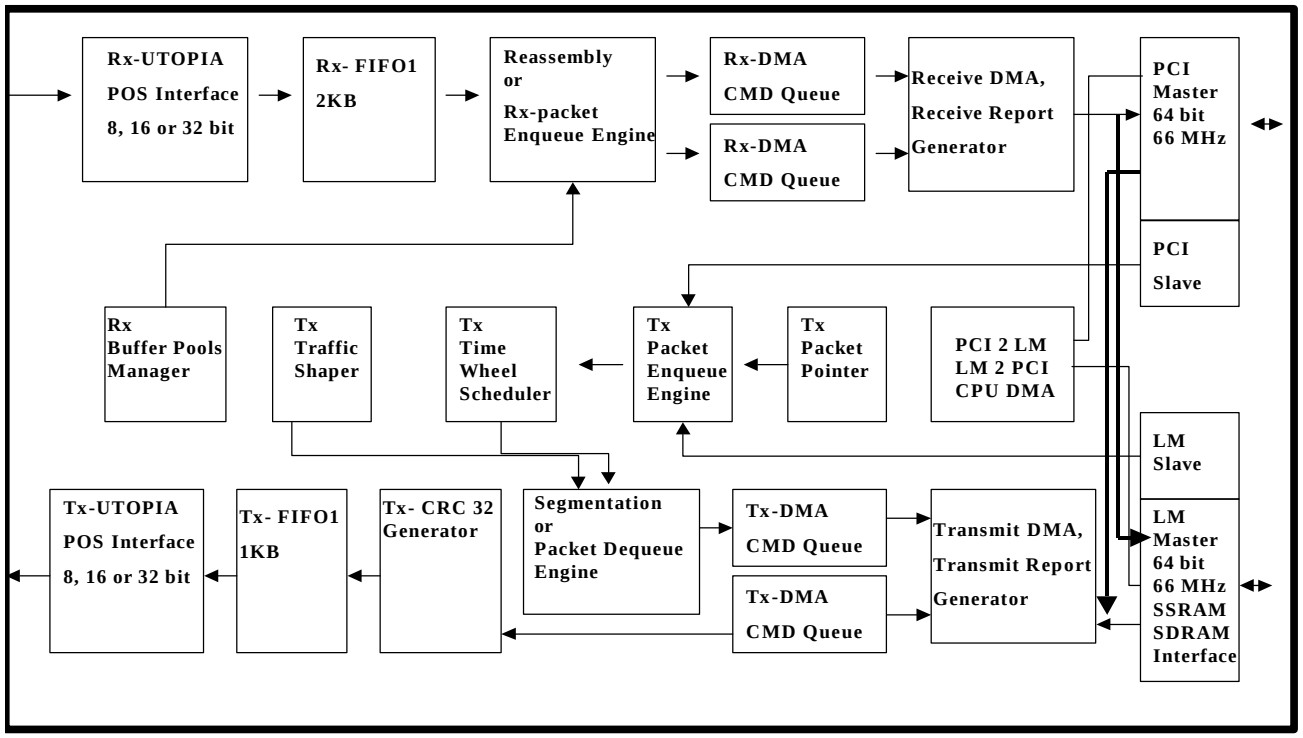
The IXF6401's 64-bit, 66Mhz LM Bus acts in concert with the 64-bit, 66 Mhz PCI Bus to provide up to 8 Gbps of bus bandwidth. An on-board DMA "engine" controls access to and from both the PCI Bus and the LM Bus and runs in master or slave modes.

The feature rich IXF6401 obtains its full speed by using extensive & dedicated hardware-based state machines. OEMs can use APIs that run on top of the 6401's device driver to achieve any value added differentiated service.

Features

- State of the Art Process Technology
- Sophisticated Buffer Management
- Comprehensive Support
- LANE Hardware Assist
- Wide Range of Applications
- PCI 2.1 Compliance
- Highest Performance
- Extensive VC Traffic Shaping & Policing
- Upper Layer Assist
- ATM & POS UTOPIA Support

IXF6401 Block Diagram



SECTION 1 - FEATURE LIST

High Performance

- Integrated ATM OC-12c Segmentation & Reassembly (SAR)
- Full duplex line rate operation for 64 byte packets
- 64-bit architecture
- Hardware encapsulation & tagging
- Hardware packet formatting

Extensive Traffic Shaping & Policing

- Up to 64K VC supported
- Traffic shaping resources for CBR, VBR
- Granularity for rates down to 1 Kbps
- Time wheel shaper for ABR/UBR with gauranteed frame rate
- Dual GCRA policing per VC
- Weighted fair queuing and dynamic priority arbitration
- Maximum bandwidth utilization with UBR fill-in for idle cells

Upper Layer Assist

- LEC ID, ELAN ID, LLC/SNAP, MPOA, IP encapsulations
- 64 byte header
- Programmable header encapsulation or tagging
- LAN, MPOA, MPLS and IP protocol assist
- Support for both packet and VC tagging
- 9 different transmit and receive report ring size configuration
- Transmit report disable feature for reduced PCI bus utilization
- Support 16 offset configuration per VC per packet or buffer in Receive process
- Support for 32-bit cell-or-packet counters for Receive
- Concurrent cell-or-packet counter reporting for ease of statistic tracking
- Support for transmit per packet offset up to 256 bytes on byte bundary
- Per packet CLP-bit setting in transmitting for frame relay congestion flag support

Feature Rich Silicon

- AAL Types 0, 1, 3/4 & 5
- TM 4.0 compliant
- Flow control: UBR, CBR, VBR, ABR
- Full 64-byte VC descriptors
- Scalable to OC-48
- ATM & POS UTOPIA 1, 2 Support

Sophisticated Buffer Management

- Full scatter/gather DMA
- Extensive transmit and receive buffering
- Two-dimensional link-list packet queuing
- 164K internal packet descriptor and packet buffer pools
- Multiple buffer sizes and buffer pools
- Support for 2 & 4-bank-structured SDRAM

State of the Art Process Technology

- 3.3V+/- 5% tolerant I/Os
- 0.35um CMOS design
- 352 pin EBGA/SBGA package
- Power consumption 6.0W @ 66Mhz

LANE Hardware Assist

- LANE V1 and V2 packet header generation
- LEC ID, ELAN ID, and/or LLC/SNAP encapsulation
- Separate LANE control buffer pool with 4K bitmap
- LANE flush protocol assist
- Programmable packet holding mode
- “Wait for Flush” reply message

Interfaces:

- Quad OC-12c or Quad OC-3c
- Glueless 64-bit SSRAM and SDRAM I/F
- PCI 2.1 compliant 33 / 66 MHz, 32 / 64 bit operation
- UTOPIA 1, 2
- ATM or Packet Over Sonet

PCI 2.1 Compliance:

- Single-cycle, master-based, fast back-to-back transaction
- PCI read-write overlap operations when either operation encounters a re-try response
- Support for PCI Master to access the 256 Mbyte Local Memory

Comprehensive Support

- Full source for device drivers provided
- Internetworking, Development, Evaluation & Application -(IDEA Platform) development environment available
- Complete GigaBlade™ reference design available
- Technical support

SECTION 2 - ARCHITECTURAL OVERVIEW

2.1 Hardware Packet Processing

The IXF6401 performs all relevant Layer 2 functions and provides extensive hardware assistance to your CPU, FPGA or ASIC-based higher-layer processing engine. Because all SAR, traffic shaping, tagging, encapsulation, buffer management & DMA is handled by the IXF6401, it enables your higher-layer engine to focus on application functions layers such as bridging, routing, encryption, network O/S, management and security.

The IXF6401 is also capable of handling any high-level application that relies on stateful inspection of packet headers as they traverse an interface boundary, such as security, firewalling, or encryption.

The IXF6401 supports a multitude of encapsulation methods that accelerate packet processing at layers 2 and 3, and can automate packet header generation using the LEC ID, ELAN ID, MAC address or any required bit field. It also performs LLC/SNAP encapsulation, LANE, MPLS, IP protocols and any custom packet tagging schemes.

2.2 ATM Processing

In addition to features for higher layer processing, the IXF6401 still comprises a full suite of ATM processing functions.

It supports ATM AAL-0, 1, 3/4 and 5 and can deliver true UBR, CBR, VBR and ABR for up to 64K VC's. The design features full 64-byte VC descriptors and multiple SONET ports.

In ATM mode, the IXF6401 provides all of the necessary termination functions currently established by the ATM Forum and IETF including:

- ATM Forum UNI 3.1 ATM Adaptation Layer and ATM Layer Specifications
- ATM Forum Traffic Management Specifications, Rev. 4.0
- RFC 1483 (Multi Protocol Encapsulation Over ATM Adaptation Layer 5)
- RFC 1626 (Default IP MTU for Use Over ATM AAL 5)
- RFC 1577 (Classical IP and ARP over ATM)
- ATM Forum LANE Specification, Version 1.0
- ATM Forum LANE Version 2.0 - LUNI Baseline Document, Draft 5, February 1997
- ATM Forum MPOA Specification, Version 1.0 - Baseline Document, February 1997

The design incorporates numerous features to maximize both chip level and system level throughput. The IXF6401 has 128 VC descriptors in its on-chip cache providing additional bandwidth for the whole system. Adding external high-speed SSRAM to the 6401's local bus increases total capacity to 64K VCs.

The IXF6401 has a sophisticated buffer management scheme. All pointer structures (128K for transmit and 36K for receive) are internal to the 6401 and greatly reduces the number of read/write operations performed during lookup, segmentation and re-assembly. Multiple buffer sizes and non-contiguous cell splitting are fully supported in hardware.The IXF6401 offers support for a PCI Master to access 256 Mbyte Local Memory. It also supports a 4-bank-structured SDRAM for Packet Buffer.

Unlike traditional SARs, which only link buffers to VCs and perform no packet processing, the IXF6401 uses a two-dimensional link list to first, link packets on a per-VC basis, and second, link buffers on a per-packet basis with enqueue/dequeue pointers to control the link list.

Enabling tremendous flexibility to perform extensive packet processing assist in hardware, as the IXF6401 can differentiate between packets within a given VC. The IXF6401 supports multiple packets per VC, with multiple buffers per p acket. The GigaBlade subsystem uses this feature to provide complete LANE 1.0 data path processing in hardware.

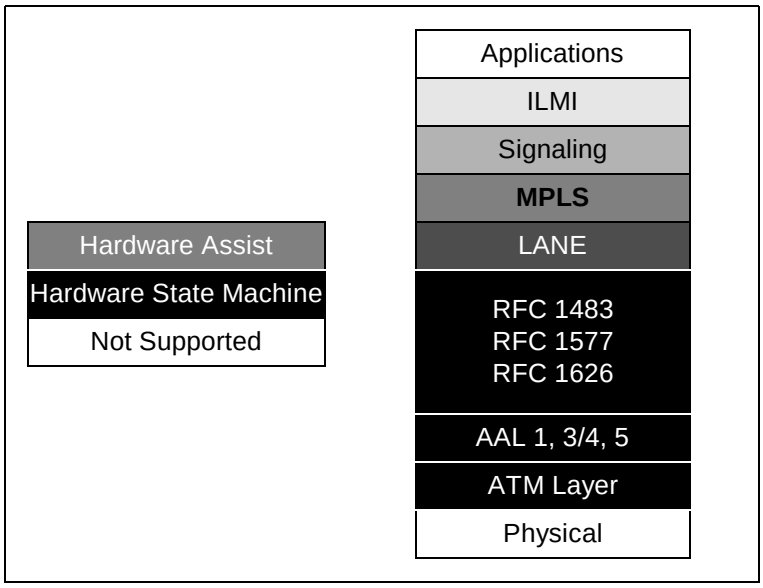


Figure 1: ATM Functionality

2.3 Traffic Shaping and Policing

The IXF6401 provides the most granular and efficient traffic shaping in the industry, making it an ideal fit for DSLAM, VoIP and class-of-service sensitive applications. It includes 16 on-chip traffic shapers for CBR/VBR, along with a complete TM 4.0 compliant ABR scheduler with guaranteed "MCR not Zero" hardware support and on board RM cell processing. The CBR/VBR shape has the support for automatic link/dink feature upon packet availability to improve bandwidth utilization.

During segmentation, if the CBR/VBR VC has no packet to send the hardware will dink the VC from shape. During an ADD PACKET command the hardware will link the VC into the shape.

During segmentation, if the ABR VC has no packet to send, the hardware will remove the VC from the scheduler table. During an "ADD PACKET command, the hardware will add the VC back into the scheduler table.

Each VC can be independently shaped within a VP to rates as low as 1Kbps giving you unprecedented control over traffic on a per-VC basis. The IXF6401's leaky take out bucket and virtual scheduling algorithms have been implemented for per VC policing.

There is no embedded RISC processor in the path of any per-cell or per-packet transaction that would slow device operation or system throughput. This massive hardware assist off loads the local CPU saving valuable cycles for other critical tasks such as bridging, routing, encryption, policy execution and security.

2.4 Basic Operation

Using the IXF6401 is simple. To send a packet to the SONET infrastructure you issue an "Add-Packet" command. The command is 64-bit and specifies how you want the packet encapsulated, tagged, what the target VPI/VCI is, what the traffic shaping parameters are. As well as the packet location and length. This can/may immediately followed by a series of "add-buffer" commands (8-byte each) telling the engine where the additional payload resides (in local SDRAM or across the PCI bus) in case the packet is spread across several buffers. From this point on the IXF6401 takes control. If required, the payload is encapsulated and tagged then passed to the traffic shapers and then to the Segmentation Engine. As it passes through the packet-cell boundary, cell headers are automatically generated as specified in the descriptor.

On the receive side, the IXF6401 performs VPI/VCI to 16-bit VC descriptor mapping and allocates buffer from its internal pools (36K). It polices the traffic using the GCRA virtual scheduling algorithm and has the ability to count or drop the non-conforming cells or packets. The IXF6401 offers the ability to differentiate between control and data

packets by directing all control packets to a different port than the data packets according to the on-chip 4K small buffer pool setting and dedicating the other on-chip 32k large buffer pool strictly to data packets.

The process of associating a packet with a descriptor is an application-level function. For example, if your application is routing, IP route matches will direct packets destined to a remote subnet to a VPI/VCI defined in a local or centralized table. In LAN Emulation or Bridging, a similar process occurs based on the MAC/LECID address.

The IXF6401 can perform any desired combination of operations on individual packets and reliably deliver wire-speed OC-12c performance for 64-byte packets. Designs must issue the requisite "add-packet" commands at whatever rates are required to achieve target performance levels.

Full support for newly developed ABR service category and multi protocols, such as TCP/IP over ATM, are also supported. On-chip memory enables cached VC descriptors to be registered and allows extensive cell buffering, which further enhances performance for OC-12c rate operation.

To handle changes to networking standards, the IXF6401 obtains configuration information from the PCI address space or from a tightly-coupled local RISC processor. The local RISC processor is not in the critical path of any per-cell or per-packet transaction and, when coupled with the extensive hardware assist of the IXF6401 is able to support multi protocol data rates of 622 Mbps, full duplex. The processor further increases overall end-system performance and manageability by off-loading ATM service-specific software functions, IP over ATM, and network statistical and management functions from the end-system's main processor. This allows the load to be distributed to each local processor which greatly reduces system bus bandwidth.

An intelligent DMA interface provides a high-speed transfer mechanism between the chip's internal or local memory and external host memory or PCI address space. The architecture also provides SSRAM and SDRAM support. In very high-performance applications, part of the memory can be allocated to SSRAM. Architectural innovations make the SRAMs unnecessary in OC-3c applications and optional in some OC-12c applications. The IXF6401 generates packet and/or buffer reports providing all information the user needs to know about the transmitted or reassambled packets. It communicates with external intelligence using a single location or a circular ring. There is also an automatic receive buffer recover feature upon completition of a CPU DMA tranfer from local bus to PCI bus.

Up to 32 Mbytes of SDRAM can be used for local buffering to support host latency, a large number of connections or virtual channels (VCs). For applications that support a smaller number of virtual channels, such as a low-end network interface card, local memory is not required. The chip's internal 32 Kbytes of memory provides fast local storage for cells and descriptor buffering.

SECTION 3 - PIN CONFIGURATION

Figure 2: IXF6401 Pin Configuration

	A	B	C	D	E	F	G	H	J	K	L	M	N
1	GND	GND	TXCLAV (3)	TXCLAV (0)	TXEN#	TXDATA (14)	TXDATA (10)	TXDATA (6)	TXDATA (3)	RCDATA (15)	RCDATA (12)	RCCLK	GND
2	GND	VCC	GND	TXL-CAV(1)	TXA-DDR(0)	TXDATA (15)	TXDATA (11)	TXDATA (7)	TXDATA (4)	TXDATA (1)	RCDATA (13)	RCDATA (9)	RCDATA (7)
3	LM_IRL(0)	GND	VCC	TXCLAV (2)	TXA-DDR(1)	TXPRTY	TXDATA (12)	TXDATA (8)	TXDATA (5)	TXDATA (2)	RCDATA (14)	RCDATA (9)	RCDATA (7)
4	LM_SA(2)	LM_IRL(1)	EXT_CLK	VCC	TXA-DDR(2)	TXSOC	TXDATA (13)	TXDATA (9)	VCC	TXCLK	TXDATA (0)	RCDATA (11)	VCC
5	LM_SA(3)	NC(GND)	LM_RCM CS#	OTEOP									
6	LM_A(2)	LM_SA(4)	IRMOD(1)	LM_IRL(2)									
7	OTMOD(1)	LM_SA(6)	IRMOD(0)	LM_SA(5)									
8	LM_A(4)	OTMOD(0)	LM_A(3)	IREOP									
9	LM_A(7)	LM_A(6)	LM_A(5)	VCC									
10	LM_A(10)	LM_A(9)	LM_CS#	LM_A(8)									
11	CPUDMA_ BUSY	DMAQF	LM_A(12)	LM_A(11)									
12	LM_A(16)	LM_A(15)	LM_A(14)	LM_A(13)									
13	GND	LM_A(17)	LM_CLK	IERR									
14	GND	LM_A(19)	LM_A(18)	VCC									
15	LM_A(23)	LM_A(22)	LM_A(21)	LM_A(20)									
16	LM_RD#	LM_WR#	LM_A(25)	LM_A(24)									
17	LM_D(1)	LM_D(0)	SSRAMC S#(0)	LM_WE# (0)									
18	LM_D(4)	LM_D(3)	LM_D(2)	VCC									
19	LM_WE# (1)	LM_D(7)	LM_D(6)	LM_D									
20	LM_D(10)	LM_D(9)	LM_D(8)	SSRAMC S#(1)									
21	LM_D(13)	SSRAMCS #(2)	LM_D(13)	LM_D(11)									
22	LM_WE# (2)	NC(VCC)	LM_D(15)	LM_D(14)									
23	IRVAL	LM_D(17)	LM_D(16)	VCC	LM_D(22)	LM_WE# (3)	LM_D(26)	LM_D(30)	VCC	LM_D(33)	LM_D(37)	LM_RAS# (1)	LM_D(41)
24	LM_D(18)	GND	VCC	NC(GND)	LM_D(23)	NC(GND)	LM_D(27)	LM_D(31)	LM_CAS# (0)	LM_D(34)	LM_D(38)	LM_CAS# (1)	LM_D(42)
25	GND	VCC	GND	LM_D(20)	NC(Vcc)	SSRAMC S#(3)	LM_D(28)	LM_WE# (4)	SDRAMC S#(0)	LM_D(35)	LM_D(39)	SDRAMC S#(1)	LM_D(43)
26	GND	GND	LM_D(19)	LM_D(21)	LM_D(24)	LM_D(25)	LM_D(29)	LM_RAS# (0)	LM_D(32)	LM_D(36)	LM_WE# (5)	LM_D (40)	GND
	A	B	C	D	E	F	G	H	J	K	L	M	N

IXF6401

352SGBA

Bottom View

(Left Side)

VCC	Power Pin (+3V)	NC(VCC)	Reserved Power pin (+3V)
GND	Ground Pin	NC(GND)	Reserved Ground Pin
CLOCK	Clock Input Pin		

Figure 2: IXF6401 Pin Configuration (cont)

P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
GND	RCDATA (0)	RCCLAV (2)	RCADDR (1)	RCEN#	DIS_ALL#	TCK	TDO	PLI_AD (27)	NC(VCC)	PCI_AD (24)	GND	GND	1
RCDATA (4)	RCDATA (1)	RCCLAV (3)	RCADDR (2)	TCADDR (0)	TMS	TDI	TRST#	NC(GND)	PCI_AD (15)	GND	VCC	GND	2
RCDATA (5)	RCDATA(2)	RCSOC	RCCLAV (0)	PCI_INT#	PCI_RST #	PCI_REQ #	PCI_AD (30)	PCI_AD (28)	PCI_AD (26)	VCC	GND	PCI_AD (23)	3
RCDATA (6)	RCDATA (3)	RCPRTY	RCCLAV (1)	VCC	PCI_CLK	PCI_GNT #	PCI_AD (3)	PCI_AD (29)	VCC	PCI_CBE #(3)	PCI_IDSE L#	PCI_AD(2 2)	4
									PCI_AD (21)	PCI_AD (20)	PCI_AD (19)	PCI_AD (18)	5
									PCI_AD (17)	PCI_AD (16)	PCI_CBE #(2)	PCI_FRA ME#	6
									PCI_IRDY #	PCI_TRD Y#	PCI_DEV SEL#	PCI_STO P	7
									PCI_PER R#	PCI_SER R#	PCI_PARI TY	PCI_CBE #(1)	8
									VCC	PCI_AD (15)	PCI_AD (14)	PCI_AD (13)	9
									PCI_AD (12)	PCI_AD (11)	PCI_AD (10)	PCI_AD (9)	10
									PCI_AD (8)	PCI_CBE #(0)	PCI_AD (7)	PCI_AD (8)	11
									PCI_AD (5)	PCI_AD (4)	PCI_AD (3)	PCI_AD (2)	12
									VCC	PCI_AD (1)	PCI_AD (0)	GND	13
									PCI_ACK #	PCI_REQ 64#	PCI_CBE #(7)	GND	14
									PCI_CBE #(6)	PCI_CBE #(5)	PCI_CBE #(4)	PCI_AD (63)	15
									PCI_AD (62)	PCI_AD (61)	PCI_AD (60)	PCI_AD (59)	16
									PCI_AD (58)	PCI_AD (57)	PCI_AD (56)	PCI_AD (55)	17
									VCC	PCI_AD (54)	PCI_AD (53)	PCI_AD (52)	18
									PCI_AD (51)	PCI_AD (50)	PCI_AD (49)	PCI_AD (48)	19
									PCI_AD (47)	PCI_AD (46)	PCI_AD (45)	PCI_AD (44)	20
									PCI_AD (43)	PCI_AD (42)	PCI_AD (41)	NC (Vcc)	21
									PCI_AD (40)	PCI_AD (39)	PCI_AD (38)	PCI_AD (37)	22
VCC	LM_D(46)	LM_CAS# (2)	LM_D(50)	VCC	LM_RAS# (3)	LM_D(57)	LM_D(61)	LM_BWAI T#	VCC	NC(GND)	PCI_AD (38)	PCI_AD (35)	23
LM_D(44)	LM_D(47)	SDRAMC S#(2)	LM_D(51)	LM_D(54)	LM_CAS# (3)	LM_D(58)	LM_D(62)	LM_BACK #	NC(VCC)	VCC	GND	PCI_AD(3 4)	24
LM_D(45)	LM_WE #(6)	LM_D(48)	LM_D(52)	LM_D(55)	SDRAMC S#(3)	LM_D(59)	LM_D(63)	LM_BREQ#	PCI_PARI TY64	GND	VCC	GND	25
GND	LM_RAS# (2)	LM_D(49)	LM_D(53)	LM_WE# (7)	LM_D(58)	LM_D(60)	LM_BREL #	OLM_CLK	PCI_AD (32)	PCI_AD (33)	GND	GND	26
P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	

IXF6401

352SGBA

Bottom View

(Left Side)

VCC	Power Pin (+3V)	NC(VCC)	Reserved Power pin (+3V)
GND	Ground Pin	NC(GND)	Reserved Ground Pin
CLOCK	Clock Input Pin		

SECTION 4 - SIGNAL DEFINITIONS

Table 1: PCI Bus Signals

Pin Numbers	Signal Name	I/O	Description
AF15, AC16, AD16, AE16, AF16, AC17, AD17, AE17, AF17, AD18, AE18, AF18, AC19, AD19, AE19, AF19, AC20, AD20, AE20, AF20, AC21, AD21, AE21, AC22, AD22, AE22, AF22, AE23, AF23, AF24, AD26, AC26, AA4, AA3, AB4, AB3, AB1, AC3, AC2, AD1, AF3, AF4, AC5, AD5, AE5, AF5, AC6, AD6, AD9, AE9, AF9, AC10, AD10, AE10, AF10, AC11, AE11, AF11, AC12, AD12, AE12, AF12, AD13, AE13	PCI_AD[63:0]	I/O	PCI Bus Multi-plexed 64-bit Address/Data. During a data phase, the upper 32 bits are meaningful when both PCI_REQ64# and PCI_ACK# are asserted. During the address phase, only the lower 32 bits are used.
AE14, AC15, AD15, AE15, AD4, AE6, AF8, AD11	PCI_CBE#[7:0]	I/O	PCI Bus Command and Byte Enable. During an address phase, PCI_CBE# represents a PCI bus command. During a data phase it represents a byte enable.
AF6	PCI_FRAME#	I/O	PCI Bus Cycle Frame. This signal is driven by the Bus master to indicate the start and end of a transaction.
AE4	PCI_IDSEL	I	PCI Bus Initialization Device Select. This signal is used as a chip select during configuration read and write transactions.
AC7	PCI_IRDY#	I/O	PCI Bus Initiator Ready. When asserted, the bus master is ready to complete the current data phase.
AD7	PCI_TRDY#	I/O	PCI Bus Target Ready. This signal is driven by the target to indicate its ability to complete current data phase.
AE7	PCI_DEVSEL#	I/O	PCI Bus Device Select. When driven, this signal indicates that the driving device has decoded its address as the target of the current access.
AF7	PCI_STOP#	I/O	PCI Bus Stop. The PCI target asserts this signal to request the bus master to stop the current transaction.
V3	PCI_INT#	O	PCI Bus Interrupt Signal. This signal should be connected to INTA# of the PCI connector.
AD8	PCI_SERR#	O	PCI Bus System Error. This signal is used to report address parity errors, data parity on the Special Cycle command, or any other system error where the result will be catastrophic. PCI_SERR# is an open drain signal.

AC8	PCI_PERR#	I/O	PCI Bus Parity Error. This bit is only used for reporting data parity errors during all PCI transactions, except for a Special Cycle.

Table 1: PCI Bus Signals (cont)

Pin Numbers	Signal Name	I/O	Description
AE8	PCI_PARITY	I/O	PCI Bus Parity Bit. Sets even parity across PCI_AD[31:0] and PCI_C/BE#[3:0].
W4	PCI_CLK	I	PCI Bus Clock. Up to 66 MHz.
Y3	PCI_REQ#	O	PCI Bus Request. The IXF6401 asserts this signal when it is trying to access the PCI bus.
Y4	PCI_GNT#	I	PCI Bus Grant for the IXF6401.
W3	PCI_RST#	I	PCI Bus Reset. This is the master reset signal for IXF6401.
AD14	PCI_REQ64#	I/O	PCI Bus Request 64-bit Transfer. When asserted, this signal indicates a 64-bit transaction.
AC14	PCI_ACK64#	I/O	PCI Bus Acknowledge 64-bit. When asserted, this signal indicates the target is willing to transfer data using 64 bits.
AC25	PCI_PARITY64	I/O	PCI Bus Parity Doubleword. Sets even parity across PCI_AD[63:32] and PCI_C/BE#[7:4].

Table 2: Local Memory Bus Signals

Pin Numbers	Signal Name	I/O	Description
AB23	LM_BWAIT#	O	Local Bus External Master Wait. During slave access, after the external master asserts LM_CS#, the IXF6401 asserts this signal when it is not ready for a data transaction. The IXF6401 removes LM_BWAIT# when it is ready for transaction. During slave read access, the data on the local bus is valid the cycle AFTER LM_BWAIT# is deasserted. The external master must hold the data until 1 cycle after this signal is deasserted during a slave write transaction.
AB24	LM_BACK#	I	Local Bus Acknowledge. This is the grant signal to the IXF6401 bus request. It should remain asserted throughout the transaction. To optimize the performance of the chip, external logic can assert this signal all the time. However, if external master is present, external logic needs to deassert this signal only when external master requires the bus by asserting LM_BREL# and LM_BREQ# is deasserted by the IXF6401. After LM_BACK# is deasserted, it must remain deasserted until the external master has completed the transaction.

AB25	LM_BREQ#	O	Local Bus Request. When asserted, this signal indicates that the IXF6401 wants to access the local bus. Once it is asserted, it remains asserted until the external master asserts LM_BREL#. If the IXF6401 is idle when LM_BREL# is asserted, the IXF6401 deasserts LM_BREQ# in the next clock cycle; otherwise, it will be 2 cycles after the IXF6401 finishes the current transaction. The IXF6401 deasserts this signal for 1 cycle only.

Table 2: Local Memory Bus Signals (cont)

Pin Numbers	Signal Name	I/O	Description
AA25, AA24, AA23, Y26:Y23, W26, V25, V24, U26:U23, T26, T25, R24, R23, P25, P24, N25:N23, M26, L25, L24, L23, K26:K23, J26, H24, H23, G26:G23, F26, E26, E24, E23, D26, D25, C26, A24, B23, C23, D22, A21, C22, C21, D21, A20, B20, C20, B19, C19, D19, A18, B18, C18, A17, B17	LM_D[63:0]	I/O	Local Bus Data. Output during master write or slave read. Input when master read or slave write. When writing to SSRAM or SDRAM, data is valid on every clock provided any of the memory chip enables are asserted. During SSRAM read access, data is valid 1 cycle after SSRAMCS# is asserted; therefore, the first cycle after SSRAMCS# is deasserted, data is still valid. When reading from SDRAM, depending on the CAS latency value, data could be valid 3 clock AFTER SDRAMCS# is asserted. As a result, data could still be valid for 3 cycles after SDRAMCS# has been removed. Data is invalid in all other cycles when IXF6401 is in master mode. During slave write, the external device must put the valid data on the data bus in the same cycle that it asserts LM_CS#, and the value of the data must be held until for 1 cycle after LM_BWAIT# is deasserted. During slave read, data is valid 1 cycle after LM_BWAIT# is deasserted and it is held until LM_CS# is deasserted by the external device.
V26, R25, L26, H25, F23, A22, A19, D17	LM_WE#[7:0]	I/O	Local Bus Write Enable. Output during master read/write and input during slave read/write. LM_WE#[7] controls LM_D[63:56]. LM_WE#[6] controls LM_D[55:48]. LM_WE#[5] controls LM_D[47:40]. LM_WE#[4] controls LM_D[39:32]. LM_WE#[3] controls LM_D[31:24]. LM_WE#[2] controls LM_D[23:16]. LM_WE#[1] controls LM_D[15:8]. LM_WE#[0] controls LM_D[7:0]. LM_WE#[2 *i*] and LM_WE#[2 *i*+1] should be connected to DQML and DQMU of the SDRAM, respectively, where *i* is 0 to 3. When connected to SSRAM, LM_WE#[*i*] should be connected to BW*i*#. LM_WE# has the same timing as local memory chip select when the IXF6401 is performing a master write.
W25, T24, M25, J25	SDRAMCS#[3:0]	O	Local Bus SDRAM Chip Select. When asserted, the IXF6401 wants to access SDRAM. These signals are asserted 2 cycles after LM_BACK# is asserted if there is a transaction pending. They remain asserted until the burst transaction has completed. Note that when these signals are deasserted at the end of the read cycle, it does not mean the data is invalid from then on; also, these signals are for flow- through only. Please see LM_D for more information.

F25, B21, D20, C17	SSRAMCS#[3:0]	I/O	Local Bus SSRAM Chip Select. When asserted, the IXF6401 wants to access SSRAM. These signals should be connected to CS# and ADSC#. ADSP# and ADV# should be tied high. These signals are asserted 2 cycles after LM_BACKLM_BREQ# is asserted if there is a transaction pending. They remain asserted until the burst transaction has completed. Note that when these signals are deasserted at the end of the read cycle, it does not mean the data is invalid from then on. Please see LM_D for more information.

Table 2: Local Memory Bus Signals (cont)

Pin Numbers	Signal Name	I/O	Description
AB26	OLM_CLK#	O	Local memory clock output
W24, T23, M24, J24	LM_CAS#[3:0]	I/O	Local Bus SDRAM Column Address Strobe Command. When this signal and SDRAMCS# are both asserted while LM_RAS# is deasserted, then the column address is selected. They remain asserted until the transaction has completed. These signals are also asserted for 1 cycle during either refresh or mode set. They should be connected directly to CAS# of a SDRAM. They are input and shaped during slave external master access local SDRAM.
W23, R26, M23, H26	LM_RAS#[3:0]	I/O	Local Bus SSRAM Colum Address Strobe Command. When this signal and SDRAMCS# are both asserted while LM_RAS# is deasserted, then the colum address is selected. They remain asserted until the transaction has completed. These signals are also asserted for 1 cycle during either refresh or mode set. They are imput and shaped during slave external master access local SDRAM.
AA26	LM_BREL#	I	Local Bus Release. The external master asserts this signal to indicate that it intents to use the local bus. It deasserts this signal once it detects that LM_BREQ# is deasserted. To improve performance, the external master should not assert this signal until there is a transaction waiting to be performed.
10 C16, D16, A15, B15, C15, D15, B14, C14, B13, A12, B12, D22, A21, C11, D11, A10, B10, D10, A9, B9, C9, A8, C8, A6	LM_A[25:2]	I/O	Local Bus Address. The SDRAM row address is selected by LM_A[14:3]. The SDRAM column address is represented by LM_A[10:3] if a "x16" device is chosen. During SSRAM operation, a new address is presented on every clock if SSRAMCS# is asserted. When the external master is performing a slave transaction, it must hold the address until LM_BWAIT# is deasserted.
B16	LM_WR#	I/O	Local Bus Write. Asserted when the IXF6401 accesses SDRAM and has the same timing as SDRAMCS#. Note that this signal is NOT asserted during a master write to SSRAM. During Slave access, the external master asserts LM_WR# to indicate a write access. The external logic should hold the signal until the IXF6401 deasserts lm_wait#.
A16	LM_RD#	I/O	Local Bus Read. Asserted when the current transaction performed by the IXF6401 is a read instruction to SSRAM. It has the same timing as SSRAMCS#. Please notice that this signal is NOT used when a master read from SDRAM is performed. This signal is asserted by the external master during a slave read transaction and external logic should hold the signal until the IXF6401 deasserts lm_wait#.

C13	LM_CLK	I	Local Bus Clock. This is the master clock for the local memory bus and the IXF6401.
C10	LM_CS#	I	Local memory chip when asserted the IXF6401 wants to access local memory.
B7, D7, B6, A5, A4	LM_SA[6:2]	O	Local Bus Spare Memory Address. When LM_A[6:2] is used for SDRAM. The LM_SA[6:2] should be used for SSRAM or vice-versa. This signal has the same timing as LM_A. However, instead of becoming input during a slave access, these pins will be tristated.
D6, B4, A3	LM_IRL[2:0]	O	Local Bus Interrupt. LM_IRL[0] is asserted when any bit in the Error Interrupt register is set. LM_IRL[1] is set when any bit in the Status Interrupt register is asserted. LM_IRL[2] is set when any bit in the Status[2:0] register is set.

Table 2: Local Memory Bus Signals (cont)

Pin Numbers	Signal Name	I/O	Description
C5	LM_ROMCS#	O	Local Bus Expansion ROM Chip Select. If ROM is present, this signal will be asserted during the booting process. PCI Master Access Expansion ROM. Only 16-bit EPROM is supported by the IXF6401 and it should be connected to LM_A[18:3] and LM_A[63:48].

Table 3: UTOPIA Bus Signals

Pin Numbers	Signal Name	I/O	Description
C1, D3, D2, D1	TXCLAV[3:0]	I	UTOPIA Bus Transmit Cell Available. When asserted, this signal indicates that MPHY is ready to accept the transfer of a complete cell.
E4, E3, E2	TXADDR[2:0]	O	UTOPIA Bus Transmit MPHY Address. When address polling is enabled, these signal are the MPHY address. When address polling is disabled, these signals are used as TXEN#[3:1].
F2, F1, G4:G1, H4:H1, J3:J1, K3, K2, L4	TXDATA[15:0]	O	UTOPIA Bus Transmit Data. This bus carries the ATM cell and is only valid when TXEN# is asserted.
F4	TXSOC	O	UTOPIA Bus Transmit Start of Cell. When asserted, this signal indicates that the current data on TXDATA is the beginning of a new ATM cell. F3 TXPRTY O UTOPIA Bus Transmit Data Parity. TXPRTY serves as the odd parity bit over TXDATA[15:0]. When FPE (Force Parity Error) is set in the UTOPIA control register, the IXF6401 asserts even parity on this pin.
F3	TXPRTY	O	UTOPIA Bus Transmit Data Parity. TXPRTY serves as the odd parity bit over TXDATA[15:0]. When FPE (Force Parity Error) is set in the UTOPIA Control register, the IXF6401 assert even parity on this pin.
E1	TXEN#	O	UTOPIA Bus Transmit Enable. When asserted, this signal indicates that the current cycle contains a valid ATM cell. K4 TXCLK I UTOPIA Bus Transmit Clock. This signal is the UTOPIA Bus transmit clock.

K4	TXCLK	I	UTOPIA Bus Transmit Clock. This signal is the UTOPIA Bus transmit clock.
T2, T1, U4, U3	RCCLAV[3:0]	I	UTOPIA Bus Receive Cell Available. When asserted, MPHY is ready to transfer a complete cell.
U2, U1, V2	RCADDR[2:0]	O	UTOPIA Bus Receive MPHY Address. When address polling is enabled, these signals are the Receive MPHY address. When polling is disabled, these signals are used as RxEn#[3:1].
K1, L3:L1, M4:M2, N3, N2, P4:P2, R4:R1	RCDATA[15:0]	I	UTOPIA Bus Receive Data. These signals carry the ATM cell and are valid only in cycles following those with RCEN# asserted.
T3	RCSOC	I	UTOPIA Bus Receive Start of Cell. This signal indicates the current data on RCDATA is the beginning of a new ATM cell.
T4	RCPRTY	I	UTOPIA Bus Receive Data Parity. This signal is only valid in cycles following those with RCEN# asserted. This bit serves as the odd parity bit over RCDATA[15:0]. When FPE (Force Parity Error) is set in the UTOPIA Control register, the IXF6401 assert even parity on this pin.
V1	RCEN#	O	UTOPIA Bus Receive Enable. When asserted, indicates that the IXF6401 is ready to accept a ATM cell in the following cycles.
M1	RCCLK	I	UTOPIA Bus Receive Clock This is the UTOPIA Bus receive clock.
D5	TEOP	O	Tx end of packet
D8	REOP	I	Rx end of packet
D13	RERR	I	Rx packet error, assert only when reop is asserted.
C6 C7	RMOD [1:0]	I	Rx module indicates the number of valid bytes in rx data. 8 bit mode - not applicable 16 bit mode - only rmod [0] is used 0: only rmod [15:0] are valid 1: only rcDATA [15:8] are valid 32 bit mode - 00 : Rc Data[31:0] are valid 01 : Rc Data [31: 8] are valid 10 : Rc Data [31: 16] are valid 11 : Rc Data [31: 24] are valid
A7 B8	TMOD[1:0]	O	Tx modulo indicates the number of valid bytes in tcdata. 8 bit mode - not applicable 16 bit mode - only TMOD [0] is used 0 : Tx Data [15:0] are valid 1 : only Tx Data [15] are valid 32 bit mode - 00 : Tx Data [31: 0] are valid 01 : Tx Data [31: 8] are valid 10 : Tx Data [31: 16] are valid 11 : Tx Data [31: 24] are valid

Table 4: Support For POS Feature

PIN #	SIGNAL NAME	I/O	SIGNAL DEFINITIONS	When in ATM Mode
D5	OTEOP	O-4mA	Transmit EOP	No Connect
D8	IREOP	I	Receive EOP	Pulldown
D13	IERR	I	Receive Error	Pulldown
C6	IRMOD(1)	I	Receive Modulo(1)	Pulldown
C7	IRMOD(0)	I	Receive Modulo(0)	Pulldown
A7	OTMOD(1)	O-4mA	Transmit Modulo(1)	No Connect
B8	OTMOD(0)	O-4mA	Transmit Modulo(0)	No Connect
A23	IRVAL	I	POS RC-Data Valid	Pullup

Table 5: JTAG Signals

Pin Numbers	Signal Name	I/O	Description
W2	TMS	I	JTAG Test Mode Select. It is used to control the state of the TAP controller in the device.
Y1	TCK	I	JTAG Input Clock.
Y2	TDI	I	JTAG Data Input.
AA1	TDO	O	JTAG Data Output.
AA2	TRST#	I	JTAG Test Reset. This will reset the TAP controller.

Table 6: Miscellaneous Signals

Pin Numbers	Signal Name	I/O	Description
W1	DIS_ALL#	I	Disable All. This signal disables all output and tristate signals. For normal operation, this signal should be high. A11 PKT_BUSY O Packet Processor Busy.
B11	CPUDMA_BUSY	O	DMA Queue Full. C4 EXT_CLK I External Clock. This clock can be used as an external clock source for the shaper.
C4	EXT_CLK	I	External clock . This clock can be used as an external source for the traffic shaper.

A11	PKT_BUSY	O	The purpose of this pin is to help the hardware to keep track of whether the IXF6401's four entry Transmit_ADD_PKT_QUEUE and 2-entry ADD_BUFFER_QUEUE are available to accept another command.
B5, D24, F24, AB2, AD23	NC(GND)	I	No connect (reserved for ground).
B22, E25, AC1, AC24, AF21	NC(VCC)	I	No connect (reserved for power).
A1, A2, A13, A14, A25, A26, B1, B3, B24, B26, C2, C25, N1, N26, P1, P26, AD2, AD25, AE1, AE3, AE24, AE26, AF1, AF2, AF13, AF14, AF25, AF26	GND	I	Ground.
B2, B25, C3, C24, D4, D9, D14, D18, D23, J4, J23, N4, P23, V4, V23, AC4, AC9, AC13, AC18, AC23, AD3, AD24, AE2,	VCC	I	Power, 3.3V.

SECTION 5 - ELECTRICAL CHARACTERISTICS

Above which the useful life of the chip may be impaired.
For user guidelines, not tested.

Table 7: Absolute Maximum Ratings

Rating	Value
Case Temperature under bias	0 C to 85 C
Storage Temperature	-65 C to 150 C
Ambient Temperature (Power ON)	-55 C to 125 C
Voltage on any pin	-0.3V to Vcc+0.3V (with respect to GND)
DC Input Voltage	–0.5V to 7.0V
Output current into TTL Outputs (LOW)	30mA
Output current into PECL Outputs (HIGH)	-50mA

Table 8: Operating Range

Range	Ambient Temperature	VCC
Commercial	0 C to +70 C	3.3V ± 5%

Table 9: DC Characteristics

Item	Symbol	Min	Type	Max	Units	Condition	Notes
Input Voltage (LV-TTL level)	VIHT VILT	2.0 -0.3	- -	Vcc+0.3 0.8	V V	-	
Input Voltage	VTT-	0.8	-		V	Vcc = 3.3V	
TTL Level	VTT	0.3	-		V	Vcc = 3.3V	
Schmitt	VTT+	-	-	2.0	V	Vcc = 3.3V	
Input Voltage (CMOS level)	VTT- AVTT	0.3Vcc 0.3	- -	- -	V V	FCC = 3.3V Vcc = 3.3V	

Table 9: DC Characteristics

Item	Symbol	Min	Type	Max	Units	Condition	Notes
Output Voltage (TTL level)	VOHT VOLT	2.4 -	- -	- 0.4	V V	IOH = -2/-4/-8/-12/-24 mA IOL = 2/4/8/12/24 mA	
Output Voltage (CMOS level)	VOHC VOLC	Vcc-0.1 -	- -	- 0.1	V V	VCC = 3.3V VCC = 3.3V	
Input leak current	ILI	-	-	1.0	µA	-	
Output leak current	ILO	-	-	1.0	µA	High impedance output mode	
Pull up current (TTL)	IPUT	120	330	800	µA	VIN = GND	
Pull up current (CMOS)	IPUC	60	165	400	µA	VIN = GND	
Pull down current (TTL)	IPDT	120	330	800	µA	VIN = VCC	
Pull down current (CMOS)	IPDC	60	165	400	µA	VIN = VCC	
Output high mini-mum current	IOH (min)	-12VCC	-	-	mA	VOUT = 0.3VCC	1
output high maximum current	IOH (max)	-	-	-32VCC	mA	VOUT = 0.7VCC	
Output low Minimum current	IOL(min)	-16VCC	-	-	mA	VOUT = 0.6VCC	1
output low maximum current	IOL (max)	-	-	38VCC	mA	VOUT = 1.8VCC	
Output High Voltage	VOH	0.9VCC	-	-	V	IOUT = -1.5mA	
Output Low Voltage	VOL	-	-	0.1VCC	V	IOUT = 1.5mA	
High clamp current	ICH	25 + (VIN-VCC-1) / 0.015	-	-	ma	VCC+4>VIN>=VCC+1	
Low clamp current	ICL	-25 + (VIN+1) / 0.015	-	-	ma	-3 < VIN >= -1	
Output Rise slew rate	Tx	1	-	4	V/ns	0.3VCC to 0.6VCC	2
Output Fall slew rate	Tx	1	-	4	V/ns	0.6VCC to 0.3VCC	2

Note: VCC = 3.3V ± 0.3V, Ta = 0° C to +70° C

Notes:

Switching current characteristics for the PCI_REQ64# and PCI_GNT# pins are permitted to be one half of what is specified here, i.e. half sized drivers may be used on these signals. This specification does not apply to PCI_CLK and PCI_RST# which are system outputs. “Switching Current High” specifications are not relevant to PCI_SERR# and PCI_INT# which are open drain outputs.

This parameter is to be interpreted as the cumulative edge rate across the specified range rather than the instantaneous rate at any point within the transition range. The specified load is optional. The designer may elect to meet this parameter with an unloaded output per rev 2.0 of the PCI spec. However, adherence to both maximum and minimum parameters is now required (the max is no longer simply a guideline).

The V/I curves define the min and max output buffer drive strength. These curves should be interpreted as traditional DC curves with one exception: from a quiescent or steady state condition, the current associated with the AC drive point must be reached within the output delay time, Tval. Note however, that this delay time also includes necessary logic time. The partitioning of Tval between clock distribution, logic and output buffer is not specified, but the faster the buffer (as long as it does not exceed the maximum rise/fall time specification) the more time allowed for logic delay inside the part.

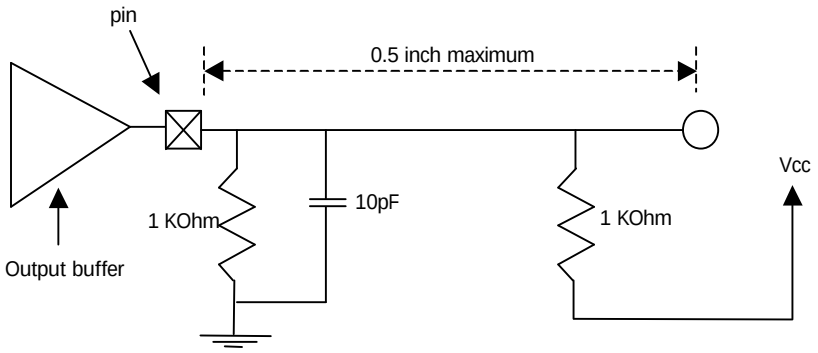


Figure 3: Tval (min) and Slew Rate

SECTION 6 - TIMING SPECIFICATIONS

6.1 Clock Timing

The clock waveform must be delivered to each 66Mhz PCI component in the system. In the case of add-in boards, compliance with clock specification is measured at the add-in board component, not at the connector slot.

Fig 4 shows the clock waveform and required measurement points for 3.3V signaling environments.

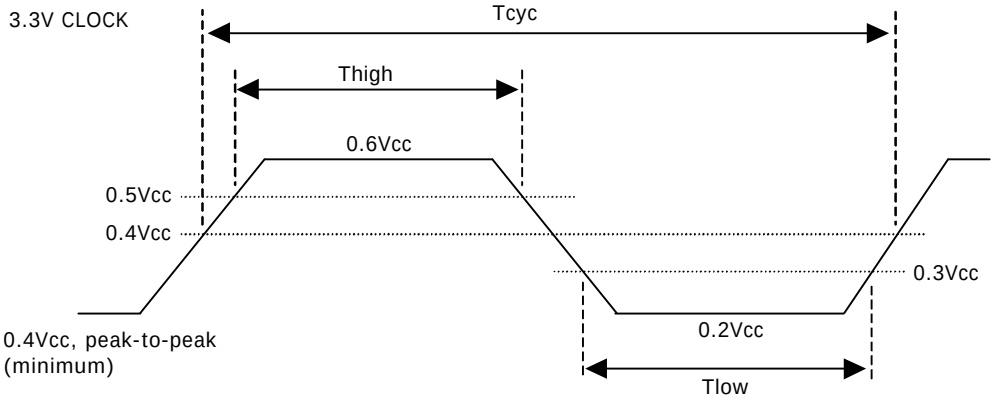


Figure 4: 3.3V CLOCK Waveform

6.2 Clock Specifications

Table 10: 33Mhz / 66Mhz Timing Parameters

Symbol	Parameter	66Mhz		33Mhz		Units	Notes
		min	max	min	max		
Tcyc	Clock cycle time	15		30		ns	1, 3
Thigh	Clock high time	6	9	12	18	ns	
Tlow	Clock low time	6	9	12	18	ns	
Tslew	Clock slew rate	1.5	4	1	4	V/ns	2

Notes:

In general, all 66.6Mhz PC components must work with a clock frequency of up to 66.6Mhz. Device operational parameters at frequencies under 33Mhz must conform to the specifications in Chapter 4 of the PCI specification, rev 2.1. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle and high and low times are not violated. The clock maybe stopped only in a low state. A variance on this specification is allowed for components designed for use on the system planar only. For clock frequency between 33Mhz and 66.6Mhz, the clock frequency may not change except in conjunction with a PCI reset.

Rise and Fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Fig 4. Clock slew rate is measured by the slew rate circuit shown in Table 10. The minimum clock rate must not be violated for any single clock cycle, i.e. accounting for all system jitter.

6.3 UTOPIA Timing Parameters

The IXF6401 UTOPIA interface is fully compliant with the ATM Forum Specifications. The following timing description is an extract from the ATM Form UTOPIA Level 2 Specification, Version 1.0 of June 1995 (af-phy-0039.0000).

Table 11: Transmit timing (16-bit data bus, Û50 MHz at cell interface)

Signal Name	DIR	Item	Description	Min	Max
TxClk		f1 tT2 tT3 tT4	TxClk frequency (nominal) TxClk duty cycle TxClk peak-to-peak jitter TxClk rise/fall time	0 40% - -	50MHz 60% 5% 2ns
TxData[15:0], TxPrty, TxSOC, TxEnb*, Txaddr	A=>P	tT5 tT6	Clock to Output Valid @ 35 pf	2 -	14 -
TxFull*/ TxClav	A<=P	tT7 tT8	Input setup to TxClk Input hold from TxClk	4ns 1ns	- -

Table 12: Receive timing (16-bit data bus, Û50 MHz at cell interface, single-PHY)

Signal Name	DIR	Item	Description	Min	Max
RxClk		f1 tT2 tT3 tT4	RxClk frequency (nominal) RxClk duty cycle RxClk peak-to-peak jitter TxClk rise/fall time	0 40% - -	50MHz 60% 5% 2ns
RxEnb*, Rxaddr	A=>P	tT5 tT6	Clock to Output Valid @ 35 pf	2 -	14 -
RxData[15:0], RxPrty, RxSOC, RxEmpty*/RxClav	A<=P	tT7 tT8	Input setup to RxClk Input hold from RxClk	4ns 1ns	- -

6.4 PCI Timing Parameters

Table 13: 33Mhz and 66Mhz Timing Parameters

Symbol	Parameter	66Mhz		33Mhz		Units	Notes
		min	max	min	max		
Tval	PCI_CLK to signal valid delay – bused signals	2	6	2	11	ns	1, 2, 3, 7
Tval(ptp)	PCI_CLK to signal valid delay – point-to-point signals	2	6	2	12	ns	1, 2, 3, 7
Ton	Float to active delay	2		2		ns	1, 7, 8
Toff	Active to Float delay		14		28	ns	1, 8
Tsu	Input setup time to PCI_CLK – bused signals	3				ns	3, 4
Tsu(ptp)	Input setup time to PCI_CLK – point-to-point signals	5		10, 12		ns	3, 4
Th	Input Hold time from PCI_CLK	0		0		ns	4
Trst	RESET active time after Power stable	1		1		ms	5
Trst-clk	RESET active time after PCI_CLK stable	100		100		us	5
Trst-off	RESET active to output float delay		40		40	ns	5
Trrsu	PCI_REQ64# to PCI_RST# setup time	10Tcyc		10Tcyc		ns	
Trrh	PCI_RST# to PCI_REQ64# HOLD time	0	50	0	50	ns	

Notes:

It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.

Minimum times are measured at the package pin with the load circuit. Maximum times are measured with the load circuit.

PCI_REQ64# and PCI_GNT# are point-to-point signals and have different input setup times than do bused signals. The PCI_REQ64# and PCI_GNT# signals have a setup time of 5 ns at 66.6Mhz. All other signals are bused.

PCI_RST# is asserted and deasserted asynchronously with respect to PCI_CLK. All output drivers must be floated when PCI_RST# is active.

When M66EN is asserted, the minimum specification for Tval(min), Tval(ptp)(min) and Ton may be reduced to 1ns if a mechanism is provided to guarantee a minimum value of 2ns when M66EN is deasserted.

For purpose of active/float timing measurements, the HI-Z or “off” state is defined as when the total current delivered through the component pin is less than or equal to the current leakage specification.

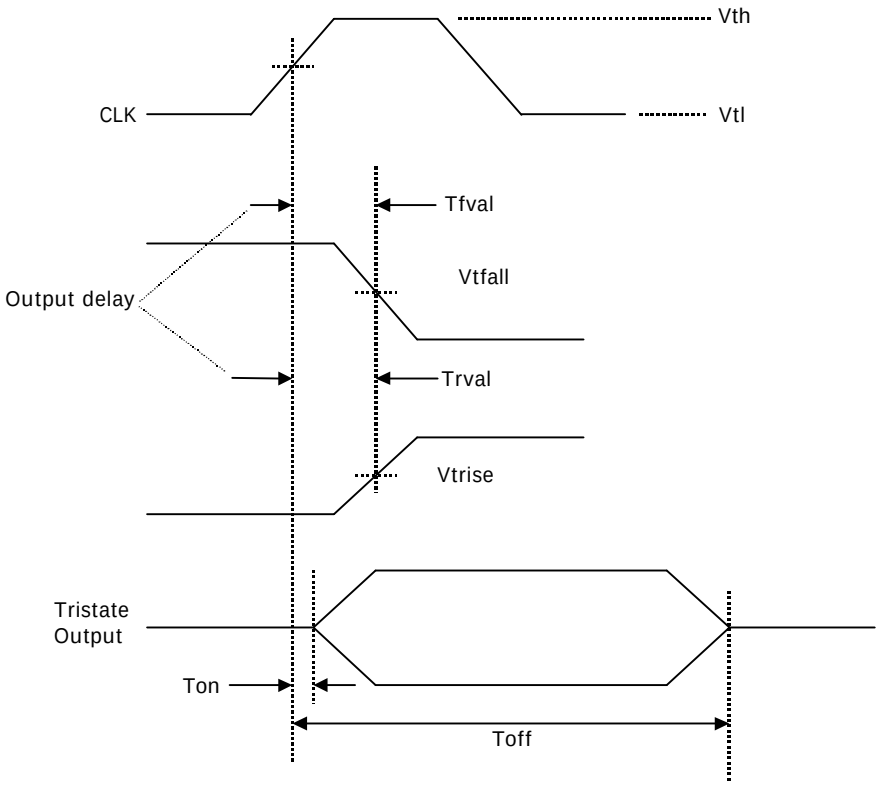


Figure 5: Output timing measurement conditions

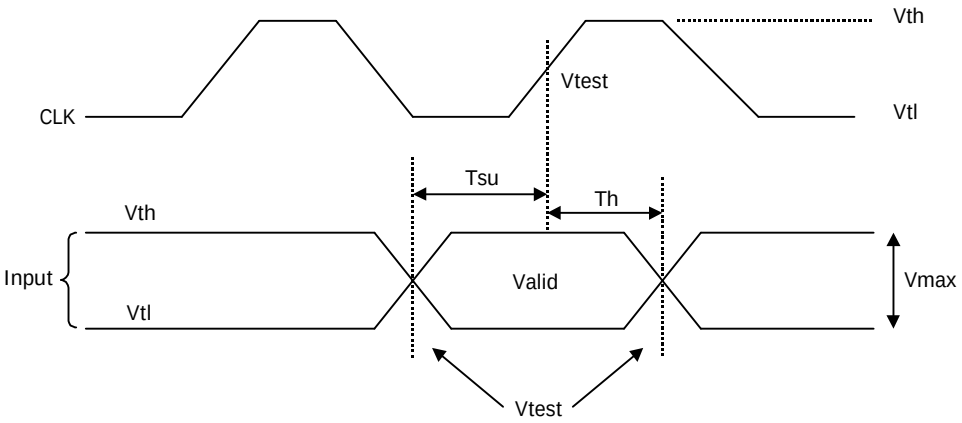


Figure 6: Input timing measurement conditions

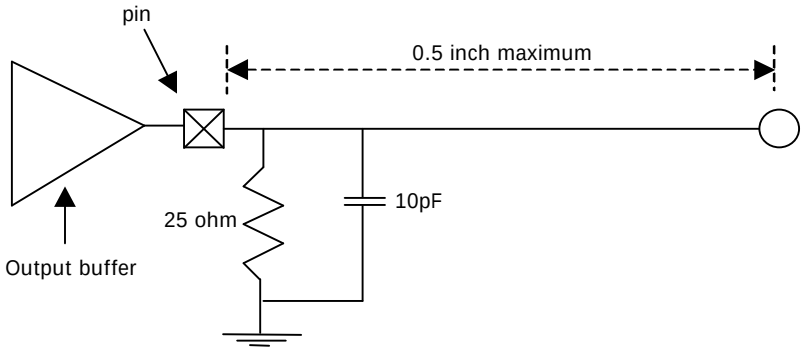


Figure 7: Tval (max) Rising edge

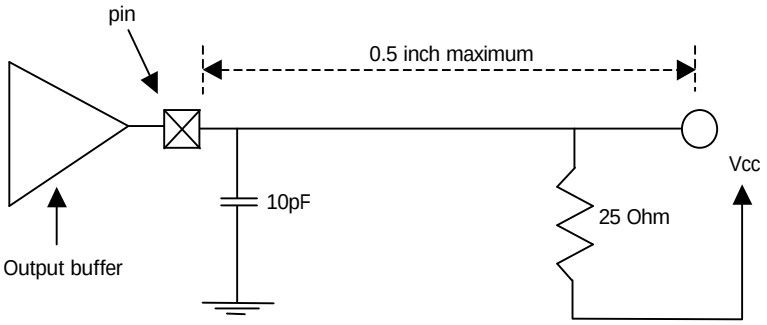


Figure 8: Tval (max) Falling edge

6.5 Local Memory Bus Timing

Table 14: Local Memory Bus Timing Parameters

Symbol	Parameter	66Mhz		33Mhz		Units	Notes
		min	max	min	max		
Tcyc	Clock cycle time	15				ns	1, 3 (clk timing)
Thigh	Clock high time	6	9			ns	
Tlow	Clock low time	6	9			ns	
Tsetup	Input setup	3				ns	
Thold	Input hold	3				ns	
Tdelay	Output delay	4	10			ns	
Thigh-z	High impedance delay	5	14			ns	

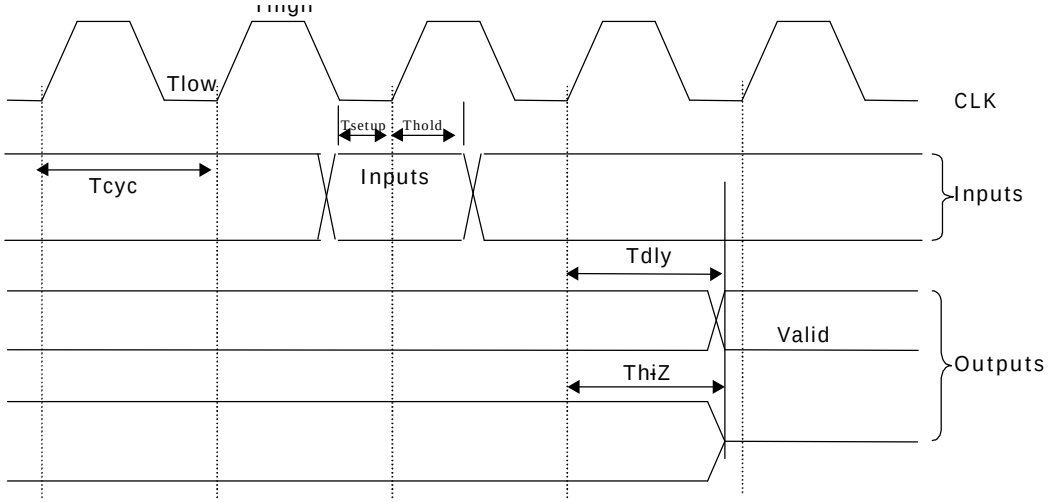


Figure 9: Local Memory Bus Timing Specifications

SECTION 7 - PACKAGE INFORMATION

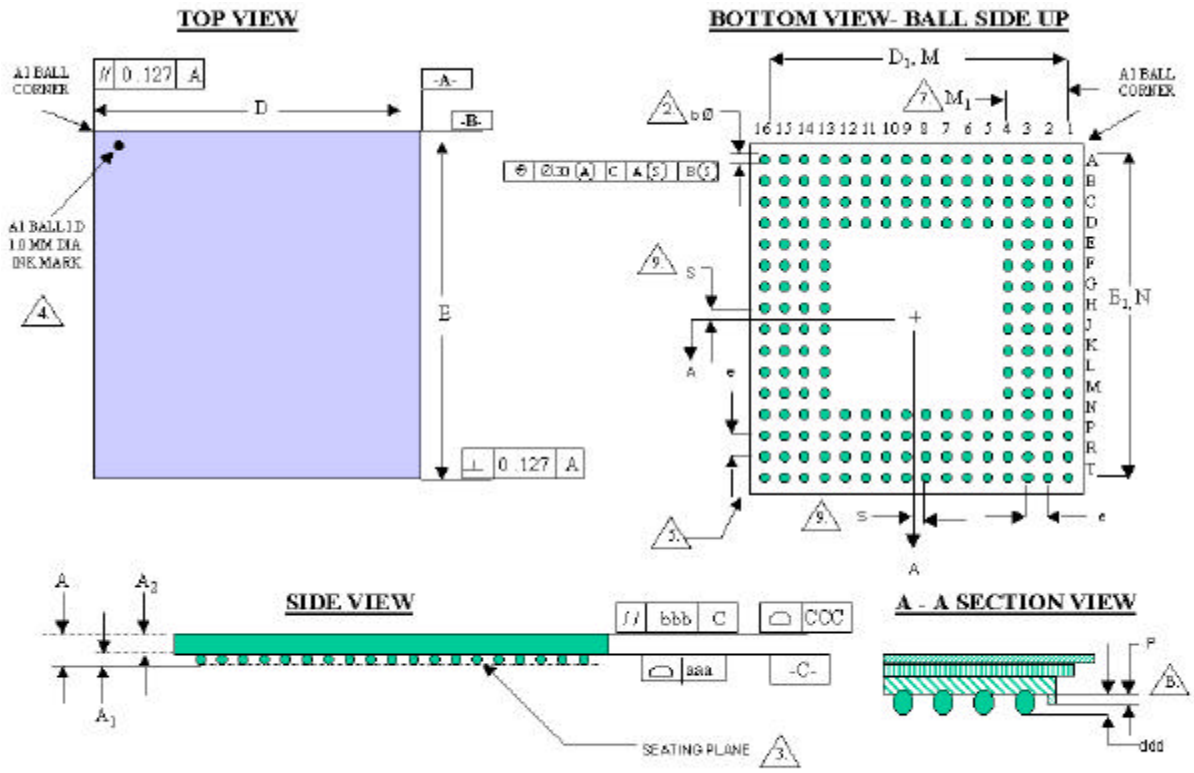


Figure 10: 352-pin Ball Array

Parameter		Millimiters		
		Min	Nom	Max
Package Height	A	1.41	1.54	1.67
Ball Height	A_1	0.56	0.63	0.70
Package Body Thickness	A_2	0.85	0.91	0.97
Package Body Width	D	34.90	35.00	35.10
Ball Foot Print	D_1	31.65	31.75	31.85
Package Body Length	E	34.90	35.00	35.10
Ball (Lead) Count	E_1,	31.65	31.75	31.85
Ball Matrix	M, N	26 x 26		
No. Of Rows Deep	M_1	2 - 4		
Ball (Lead) Width	b	0.60	0.75	0.90
Ball Pitch	e	1.27		
Complanarity	aaa			0.15
Parallel	bbb			0.15
Top Flatness	ccc			0.20
Seating Plane Clearance	ddd	0.15	0.33	0.50
Encapsulation Height	p	0.20	0.30	0.35
Solder Ball Placement	s			0.635

Table 15: 352-pin Ball Array

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