System Clock Chip for Pentium Asynchronous PCI System Board using Mobile Triton Core Logic

Approved Product

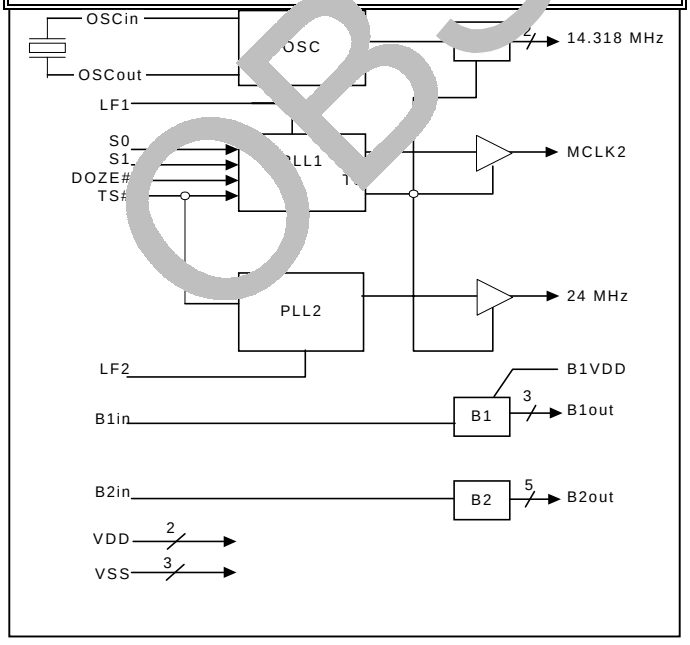
PRODUCT FEATURES

- Supports Pentium™ asynchronous PCI system board designs using mobile Triton core logic
- Integrates system clocks and distribution buffers
- Operates from 5V or 3.3V supply
- Separate B1 buffer VDD supports mixed 5V/3.3V outputs
- Doze and power down low power operating modes
- 60 mA buffer switching current
- 28 Pin SSOP package for minimum board space

FREQUENCY SELECTION

S1	S0	MCLK	
		DOZE# = 1	DOZE# = 0
0	0	66.66	33.3
0	1	50	33.3
1	0	60	33.3
1	1	40	33.3

BLOCK DIAGRAM

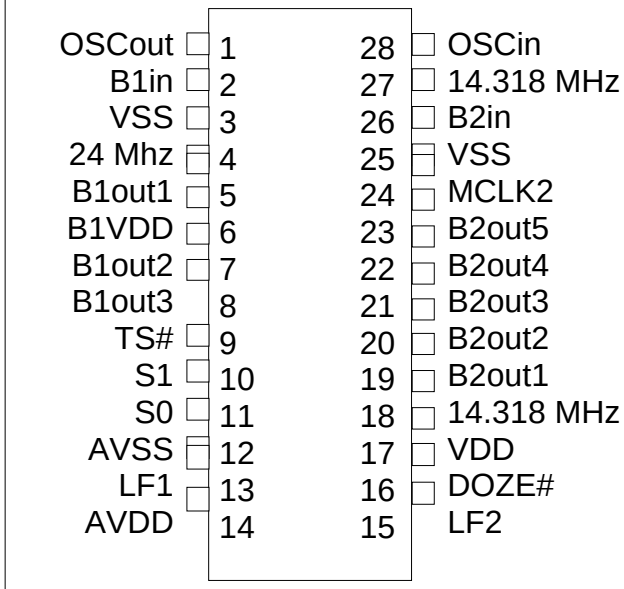


APPLICATIONS

Two 3.3V operating modes support new low voltage components on the CPU bus. Operating the B1OUT* buffers at 3.3V (B1VDD) and routing the CPU clock through B1IN distributes a 3.3V signal to the CPU bus. 60mA switching current is provided at the B1out* buffers operated at 3 volts.

Both buffers can distribute the CPU signal at 3.3V if both the core logic VDD and B1VDD=3.3V. With this configuration, the CPU signal can be distributed to 8 traces with up to 2 planar loads per trace.

CONNECTION DIAGRAM



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PIN DESCRIPTION

OSCin OSCout- These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCin may also serve as input for an externally generated reference signal.

S0 and S1- Standard frequency select inputs. These inputs control the high speed MCLK2, frequency selection. All these inputs have internal pull-ups. MCLK2 switches smoothly to changes in these inputs.

The output frequency selection is shown on page 1.

MCLK2 - Master clock output. Programmable output frequencies can be selected using S0-S1 inputs.

DOZE# - DOZE control pin. When DOZE# is high, the clock chip operates in the standard mode. When this pin goes low, output frequencies are switched to the preprogrammed DOZE frequencies. Switching to DOZE frequencies occurs smoothly to allow tracking by the internal PLL. This pin has an internal pull-up.

B1in and B2in - On-chip buffer inputs. These pins have internal pull-up.

B1out - Buffered outputs of B1in. Switching current and output high level voltage controlled by B1VDD.

B2out - Buffered outputs of B2 buffer. Switching current and output high level controlled by VDD.

24 MHz - SIO clock output.

TS# - Logic low on this input tristates all PLL outputs if S1=S0 = logic high. PLL's are stopped to reduce power and all circuitry is reset. Other states of S1 and S0 put circuit in a test mode. This pin has an internal pull-up.

14.318 MHz- 14.318 MHz output. Buffered output from on-chip reference oscillator or externally provided reference.

LF1 and LF2 - These are the phase detector outputs for the clock generators. They are single-ended, tristate output for use as loop error signal. A 0.1uF capacitor to ground should be connected from this pin to form the loop filter. Grounding LF puts PLL in low power mode.

VSS- Circuit ground

VDD- Positive power supply

AVDD- Analog positive power supply

AVSS- Analog circuit ground

B1VDD - 3.3V/5V logic level control for B1out buffers. B1VDD $\leq$ VDD.

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MAXIMUM RATINGS

Voltage Relative to VSS	-0.3V
Voltage Relative to VDD	0.3V
Ambient Temperature:	-0°C to + 70°C
Storage Temperature:	-65°C to +150°C
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)< VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	
Input High Voltage	VIH	2.0		-	Vdc	All Inputs
Input Low Current with Pull up or Pull-down	IIL	-	-	5 ±50	uA	TS#, S0-S1 Inputs
Input High Current with Pull-up or Pull-down	IIH	-	-	5 ±50	uA	TS#, S0-S1 Inputs
Output Low Voltage IOL = 12 mA		-	-	0.8		All Outputs
Output High Voltage IOH=12mA	OH	2.4	-	-	Vdc	All Outputs
Tri-State Leakage Current	IOZ	-	-	10	uA	LF1 and LF2
Dynamic Supply Current	ICC	-	-	30	mA	MCLK2 = 50 MHz
Static Supply current	ICC(PD)	-	-	300	µA	TS# = low, S1=S0= High
Short Circuit Current	ISC	25	-	-	mA	

AVDD = VDD = 5V ± 10%, B1VDD = 3.3v ± 10% TA = 0°C to +70°C

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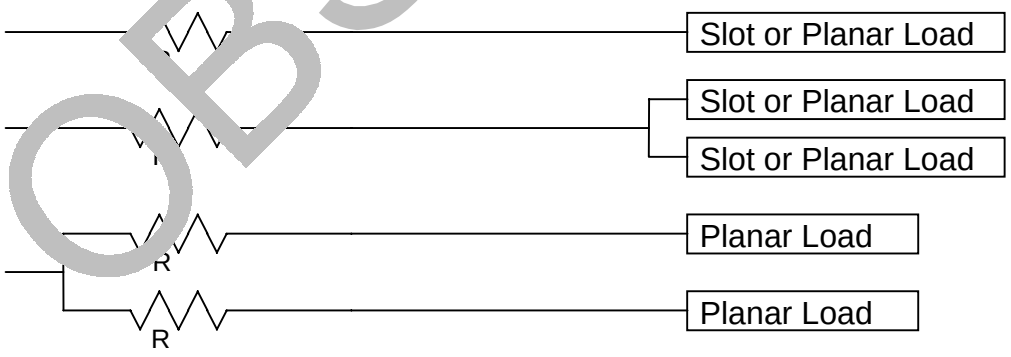
SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Rise (0.4V - 2.0V) and Fall (2.0V-0.4V) time All Outputs	**t**TLH, **t**THL	-	-	1.5	ns	15 pf Load
Output Duty Cycle		45	50	55	%	Measured at 1.5V
Buffer Propagation Delay Bin to Bout	**t**PLH, **t**PHL	-		5	ns	pf Load Measured at 1.5V
Buffer out Skew All B1 and B2 Buffer Outputs	tSKEW	-	-	250	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles MCLK2	ΔP	-	-	±200	ps	-
Jitter Absolute MCLK2	**t**jab	-	±200	-	ps	-
Input Rise/Fall Time S0-S1		-	-	2	us	-
Switching Current Low:	IOL (AC)	-	60	-	mA	VOL = 1.5V
Switching Current High:	IOH (AC)	-	50	-	mA	VOL = 1.5V
VDD = 5V± 10%, B1VDD = 3.3V ± 10%, TA = 0°C to 70°C						

OUTPUT LOADING OPTIONS VERSUS IOL (AC), IOH (AC)



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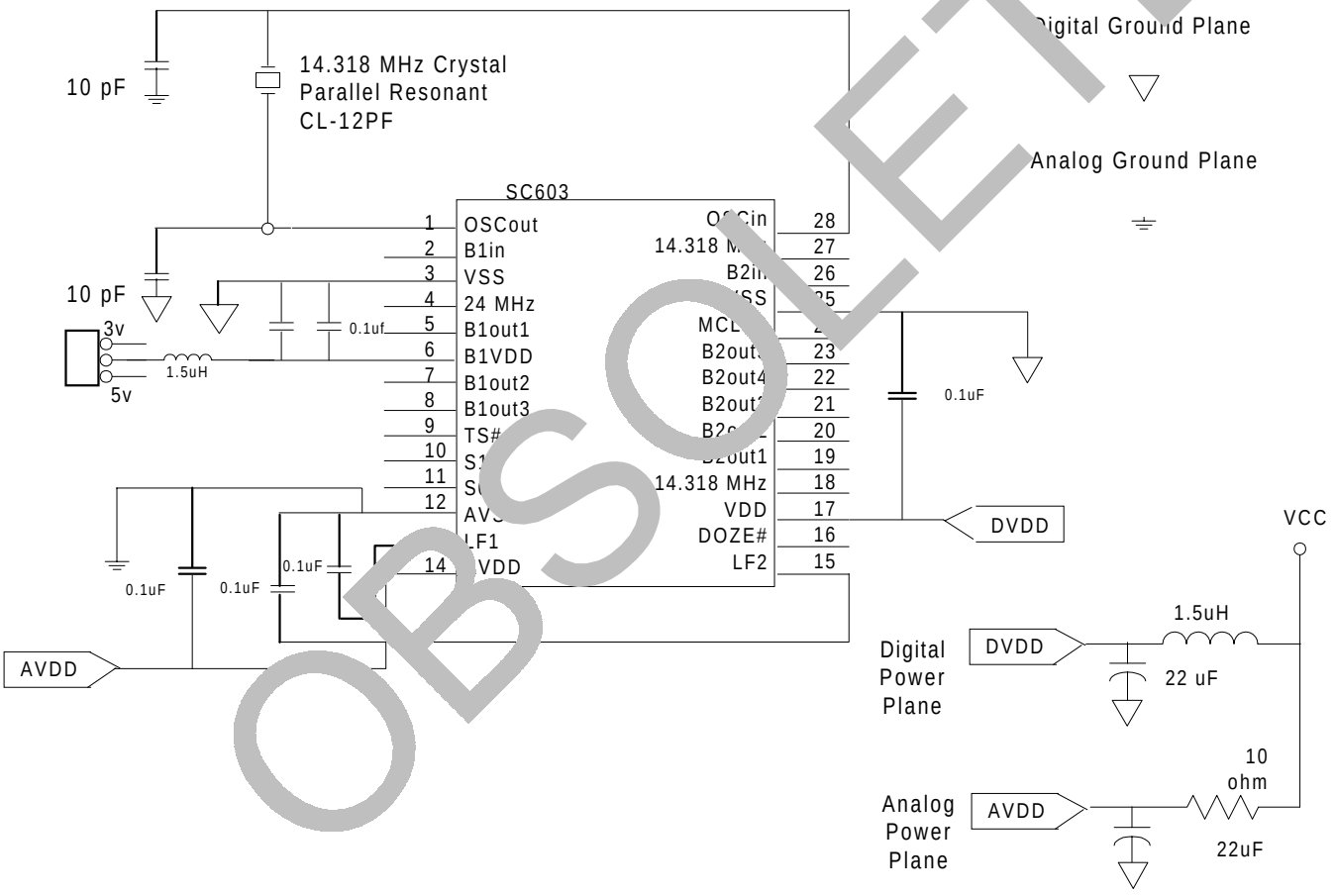
APPLICATION SUGGESTION

NOTE 1: Connect analog ground (AVSS) to PC Board ground through one point only.

NOTE 2: Caps connected to pins 6, 14, and 17 should be as close as possible to their VDD pins.

NOTE 3: If VDD at clock generator ramps up more than 100 MV DC within a 5 us time period (from turning disk drive off, etc.). The values of the DVDD and AVDD filter components should be increased.



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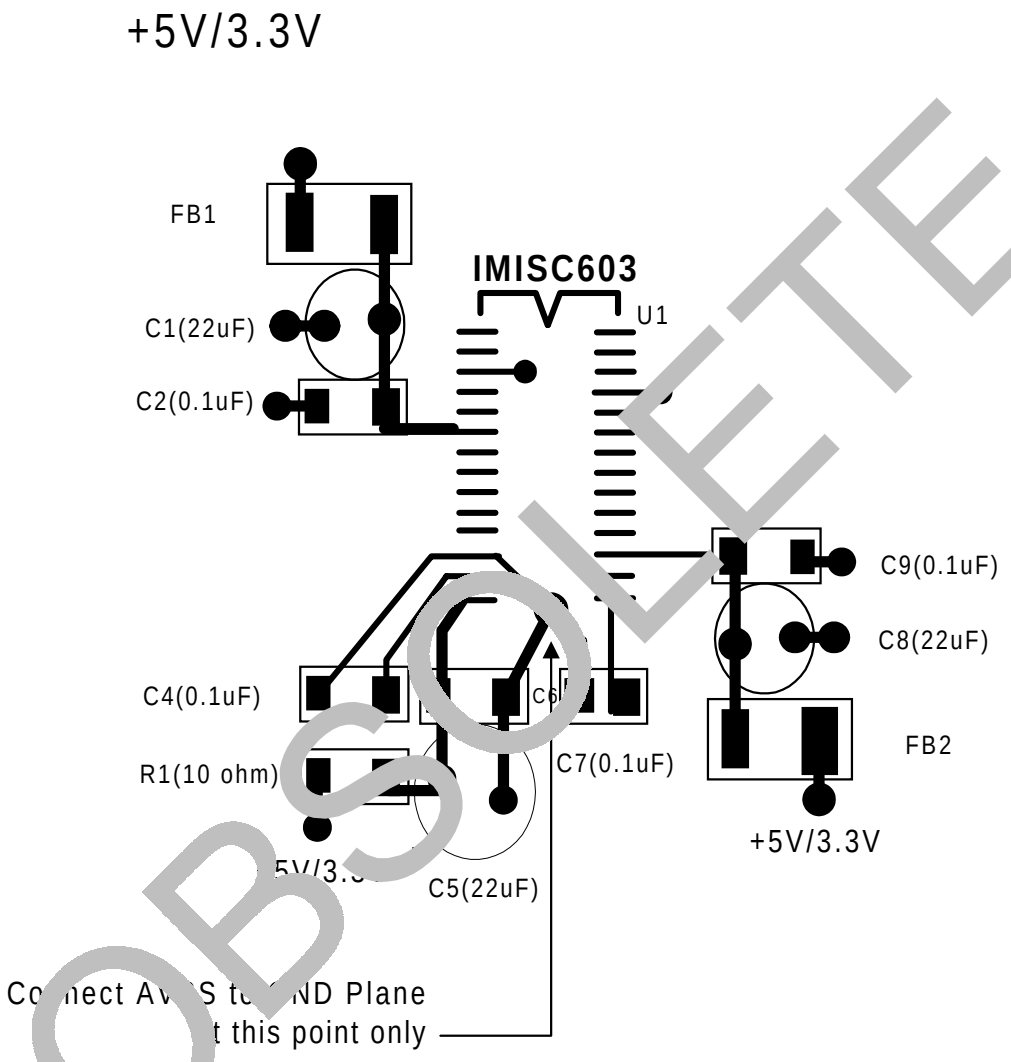
PCB LAYOUT SUGGESTION



NOTES

1) Power supply bypass cap (0.1µF) must be positioned close to VDD pins to be effective.
2) LF caps must be low leakage, such as multilayer ceramic Z5U or X7r material.

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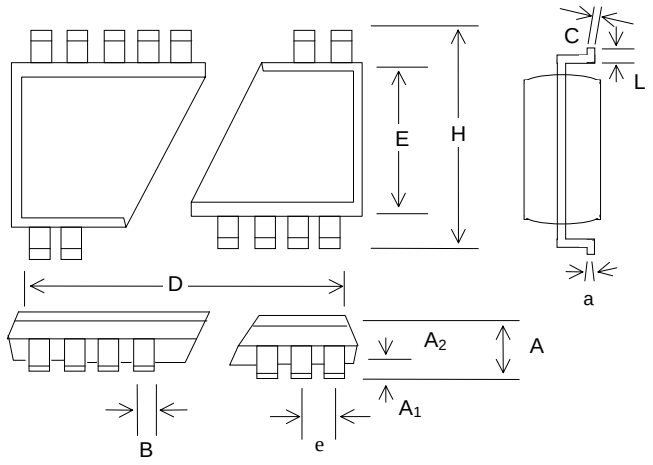
PACKAGE DRAWING AND DIMENSIONS



28 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.0	0.00	0.05	0.13	0.21
A2	0.066	.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.00	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
	0.0256 BSC			0.65 BSC		
	0.301`	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.0	0.030	0.037	0.55	0.75	0.95

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC603AYB	28 Pin SSOP	mmercial, 0°C to + 70°C

Marking: Example: IMI
SC YB
Date Co e
ot #

IMISC6 B

Flow
B = Commercial, 0°C to + 70° C

Package
Y = SSOP

Revision

IMI Device Number