# IMISC493   SYSTEM CLOCK CHIP

October 1, 1995

PRODUCT FEATURES

- Supports Pentium™ asynchronous PCI system board designs using mobile Triton core logic
- Integrates system clocks and distribution buffers
- Operates from 5V or 3.3V supply
- Separate B1 buffer VDD supports mixed 5V/3.3V outputs
- Doze and power down low power operating modes
- 60 mA buffer switching current
- 28 Pin SSOP package for minimum board space

FREQUENCY SELECTION

S1	S0	MCLK	
		DOZE# = 1	DOZE# = 2
0	0	66.66	33.3
0	1	50	33.3
1	0	60	33.3
1	1	40	33.3

BLOCK DIAGRAM
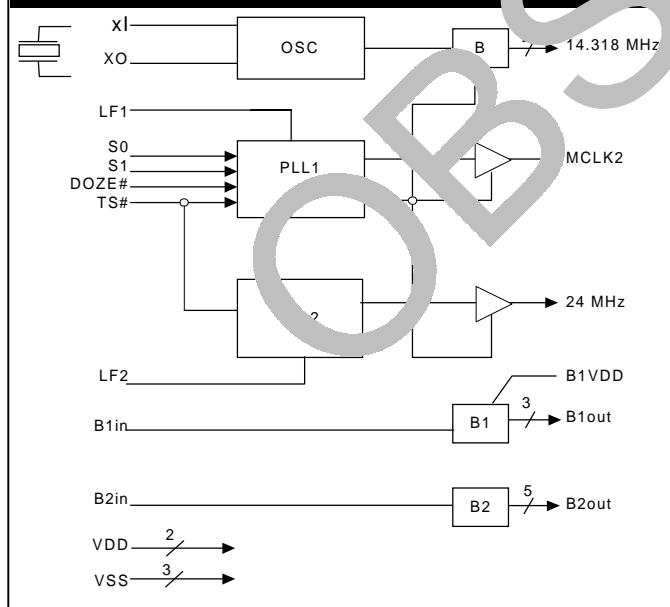
APPLICATIONS

Two 3.3V operating modes support new low voltage components on the CPU bus. Operating the B1 buffer at 3.3V (B1VDD) and routing the CPU clock through B1 distributes a 3.3V signal to the CPU bus. 60mA of switching current is provided if the buffer is operated at 5 volts, or 30 mA at 3 volts. Two output drivers are connected to B1out1 to provide low skew drive for the CPU and cache controller.

Both buffers can distribute the CPU signal at 3.3V if both the core logic VDD and B1VDD=3.3V. With this configuration, the CPU signal can be distributed to 8 traces with up to 2 planar loads per trace.

CONNECTION DIAGRAM

OSCout	1	28	OSCin
B1in	2	27	14.318 MHz
VSS	3	26	B2in
24 Mhz	4	25	VSS
B1out1	5	24	MCLK2
B1VDD	6	23	B2out5
B1out2	7	22	B2out4
B1out3	8	21	B2out3
TS#	9	20	B2out2
S1	10	19	B2out1
S0	11	18	14.318 MHz
AVSS	12	17	VDD
LF1	13	16	DOZE#
AVDD	14	15	LF2

*This feature added on product Revision C.

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PIN DESCRIPTION

OSCin OSCout- These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCin may also serve as input for an externally generated reference signal.

S0 and S1- Standard frequency select inputs. These inputs control the high speed MCLK, frequency selection. All these inputs have internal pull-ups. MCLK switches smoothly to changes in these inputs.

The output frequency selection is shown on page 1.

MCLK2 - Master clock output. Programmable output frequencies can be selected using S0-S1 inputs.

DOZE# - DOZE control pin. When DOZE# is high, the clock chip operates in the standard mode. When this pin goes low, output frequencies are switched to the preprogrammed DOZE frequencies. Switching to DOZE frequencies occurs smoothly to allow tracking by CPU internal PLL. This pin has an internal pull-up.

B1in and B2in - On-chip buffer inputs. These are CMOS inputs that switch at VDD/2. These pins have internal pull-up.

B1out - Buffered outputs of B1 buffer. Switching current and output high level voltage controlled by B1VDD. B1out1 is connected to two output cells.

B2out - Buffered outputs of B2 buffer. Switching current and output high level controlled by VDD.

24 MHz - SIO clock output.

TS# - Logic low on this input tristates all PLL outputs if S1=S0 = logic high. PLL's are settled to reduce power and all circuitry is reset. Other states of S1 and S0 put circuit in a test mode. This pin has an internal pull-up.

14.318 MHz- 14.318 MHz output. Buffered output from on-chip reference oscillator or externally provided reference.

LF1 and LF2 - These are the phase detector outputs for the clock generator. They are single-ended, tristate outputs for use as loop error signal. A 0.1uF capacitor to ground should be connected from this pin to form the loop filter. Grounding LF puts PLL in low power mode.

VSS- Circuit ground

VDD- Positive power supply

AVDD- Analog positive power supply

AVSS- Analog circuit ground

B1VDD - 3.3V/5V logic level control for B1 buffer. B1VDD cannot be greater than VDD.

MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS < (Vin \text{ or } Vout) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

Voltage Relative to VSS	-.03 to 6V
Voltage Relative to VDD	0.3V
Ambient Temperature:	-0°C to + 70°C
Storage Temperature:	-65°C to +150°C
Recommended Operating Range	3V - 6V

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	
Input High Voltage	VIH	2.0	-	-	Vdc	TS#, DOZE#, and S0-S1 Inputs
Input High Voltage	VIH	0.7VDD				B1in and B2in Inputs
Input Low Current with Pull up or Pull-down	IIL	-	-	5 / ±50	uA	OE, S0-S1 Inputs
Input High Current with Pull-up or Pull-down	IIH	-	-	5 / ±50	uA	OE, S0-S1 Inputs
IOL = 12 mA Output Low Voltage IOL = 6mA	VOL	-	-	0.4	Vdc	B1out1
						All Other Outputs
IOH = 12 mA Output High Voltage IOH=6mA	VOH	2.4	-	-	Vdc	B1out1
						All Other Outputs
Tri-State Leakage Current	IOZ	-	-	10	uA	LF1 and LF2
Dynamic Supply Current	ICC	-	-	30*	mA	MCLK2 = 50 MHz
Short Circuit Current	ICC(PD)	-	-	-	µA	TS# = low, S1=S0= High
Short Circuit Current	ISC	25	-	-	mA	
						VDD = B1VDD = 3.3v ± 10% TA = 0°C to +70°C

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PLL FREQUENCY SYNTHESIZER

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time All Outputs	**t**TLH, **t**THL	-	-	1.5*	ns	15 pf Load
Output Duty Cycle		45	50	55	%	Measured at 1.5V
Buffer Propagation Delay Bin to Bout	**t**PLH, **t**PHL	-	4.7*	-	ns	15 pf Load Measured at 1.5V
Buffer out Skew All B1 and B2 Buffer Outputs	tSKEW	-	-	250	ps	15pf Load Measured at 1.5V B1in = B2in, VDD = 5V, B1VDD = 3.3V
ΔPeriod Adjacent Cycles MCLK2	ΔP	-	±200	-	ps	-
Jitter Absolute MCLK2	**t**jab	-	±200	-	ps	-
Input Rise/Fall Time S0-S1		-	-	2	us	-
Switching Current Low:	IOL (AC)	-	60**	-	mA	VOL = 1.5V
Switching Current High:	IOH (AC)	-	50**	-	mA	VOL = 1.5V
						VDD = B1VDD = 3.3V $\pm$ 10%, TA = 0°C to 70°C

* For VDD = + 5V $\pm$ 10% operation only.
** IOL (AC) and IOH (AC) are reduced by 45% if VDD (B2 Buffer) or B1VDD (B1 Buffer) = + 3.3V. B1out1 supplies twice the current of other outputs.

OUTPUT LOADING OPTIONS VERSUS IOL (AC), IOH (AC)

Clock Output ——〜〜〜—— Slot or Planar Load   30 or 60 MA Drive O.K.

Clock Output ——〜〜〜—— Planar Load / Planar Load   30 or 60 MA Drive O.K.

Clock Output —〜〜〜— Slot or Planar Load / —〜〜〜— Slot or Planar Load   60 MA Drive O.K. (B1out1 at 3V). 30 MA (other outputs at 3V) on 66 MHz CPU Clocks requires careful design.
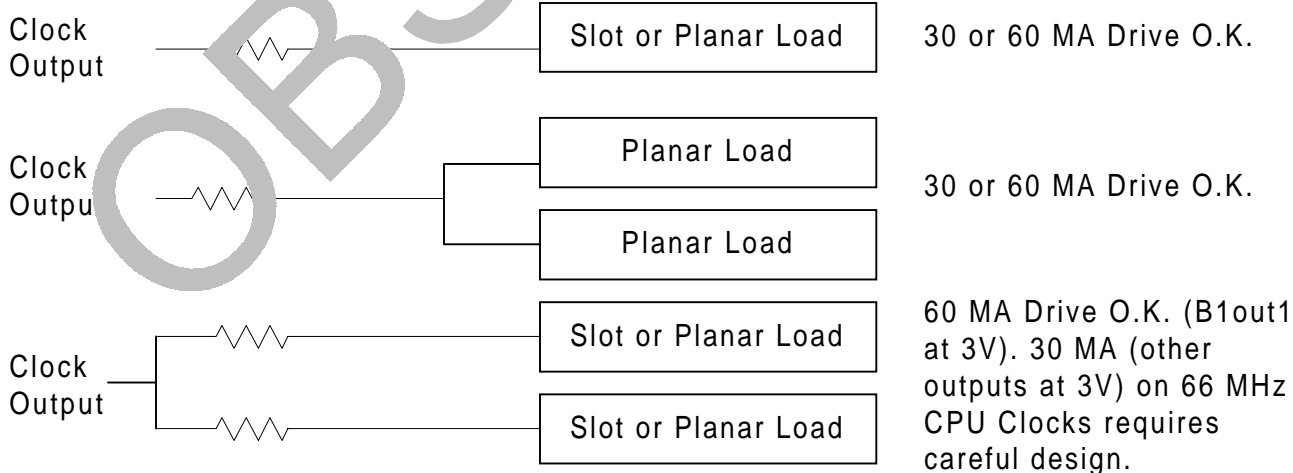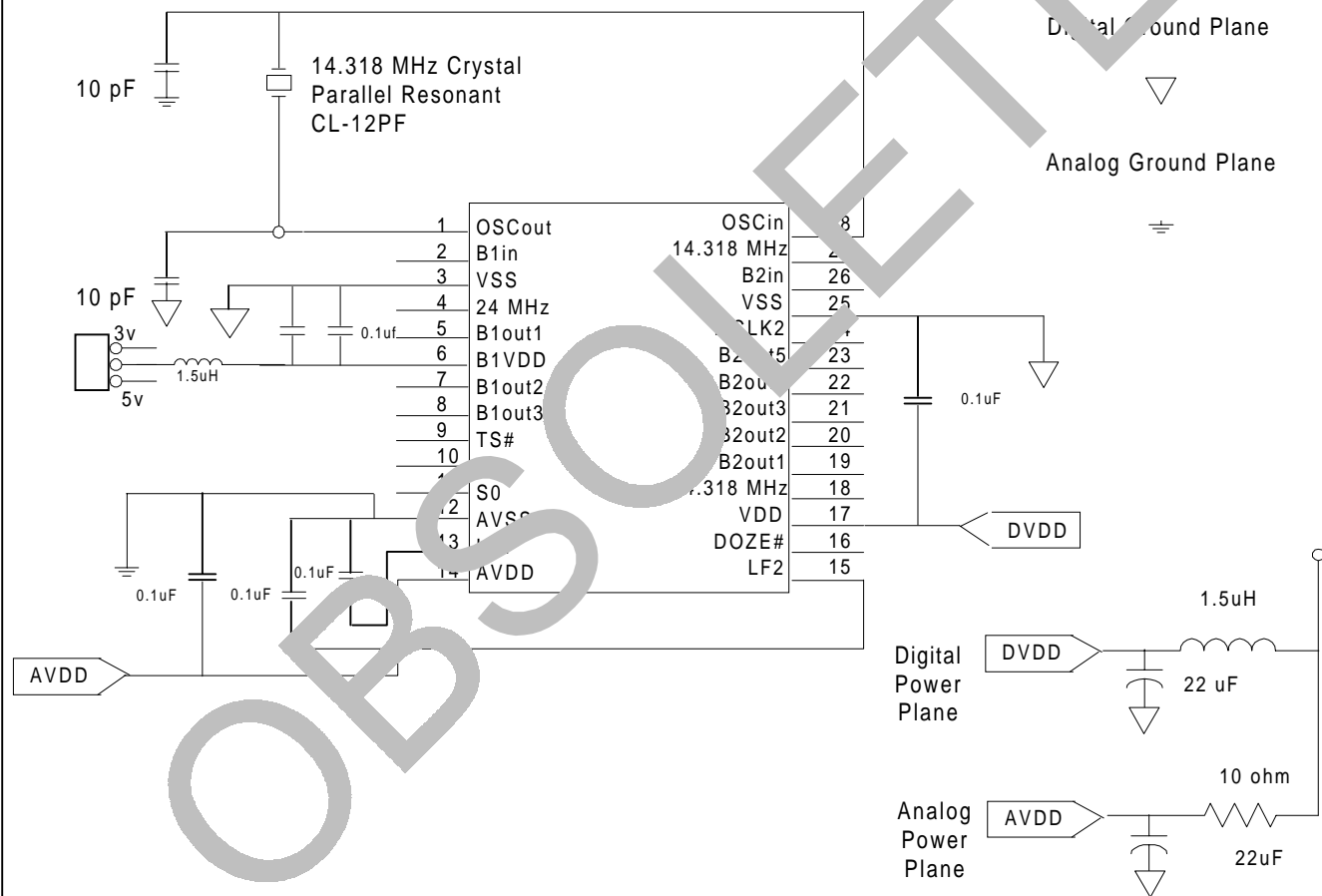
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APPLICATION SUGGESTION

NOTE 1: Connect analog ground (AVSS) to PC Board ground through one point only.

NOTE 2: Caps connected to pins 6, 14, and 17 should be as close as possible to their VDD pins.
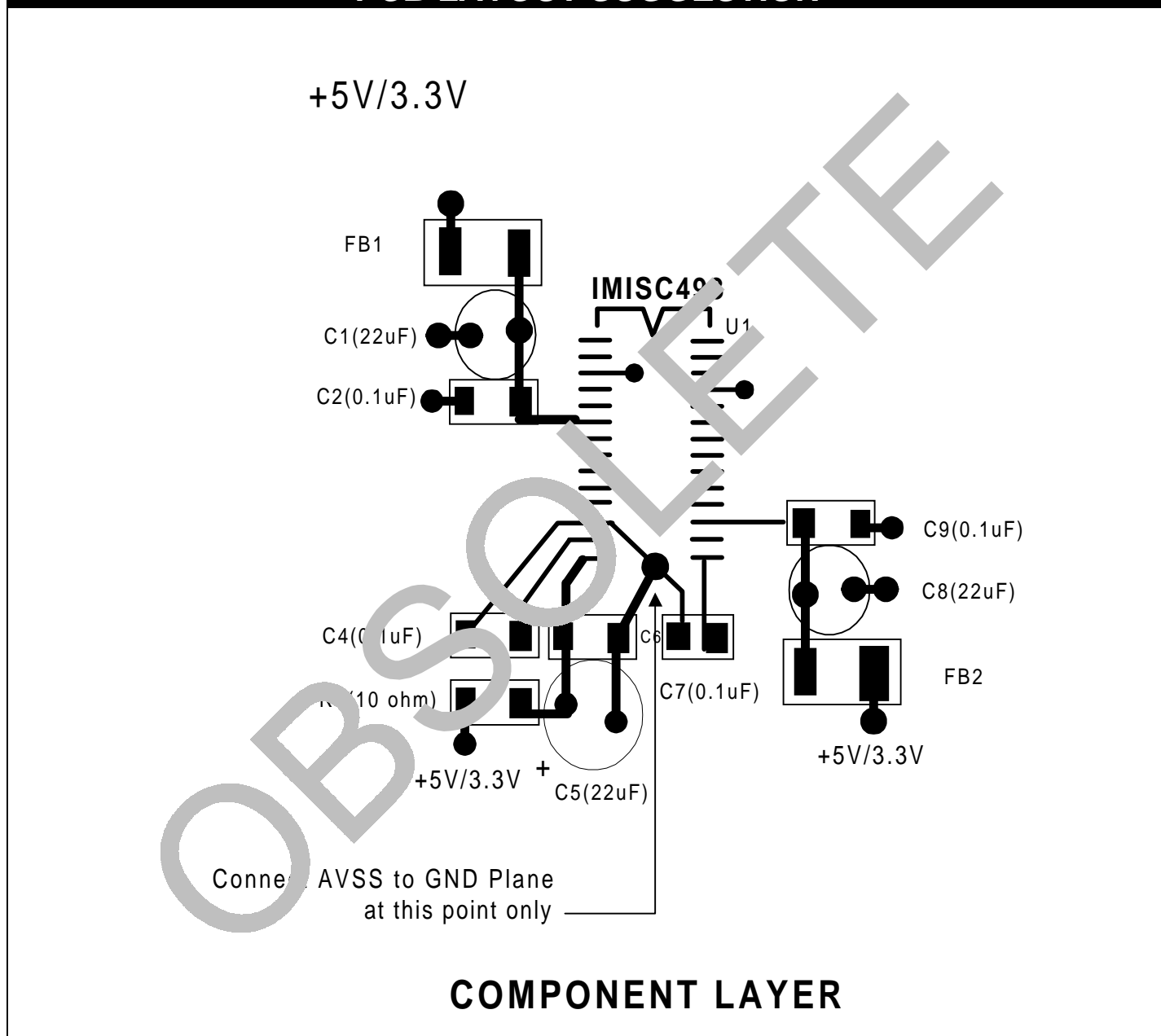
NOTE 3: If VDD at clock generator ramps up more than 100 MV DC within a 5 us time period (from turning disk drive off, etc.). The values of the DVDD and AVDD filter components should be increased.

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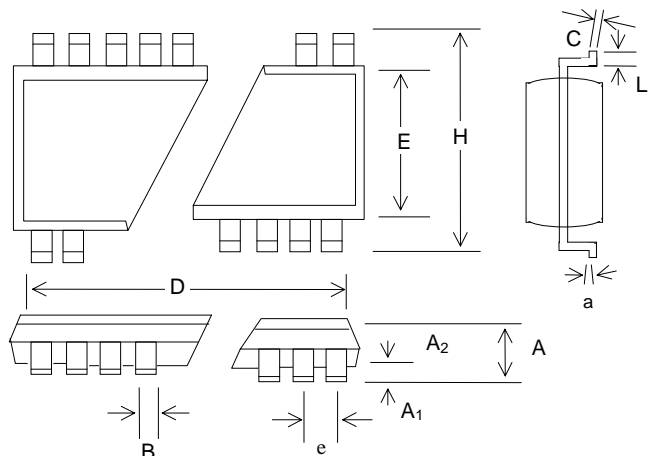
PCB LAYOUT SUGGESTION

COMPONENT LAYER

NOTES

1)   Power supply bypass cap (0.1µF) must be positioned close to VDD pins to be effective.

2)   LF caps must be low leakage, such as multilayer ceramic Z5U or X7r material.

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PACKAGE DRAWING AND DIMENSIONS

28 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.08	0.073	0.78	1.75	1.8	1.99
A$_1$	0.002	0.005	0.008	0.05	0.1	0.21
A2	0.066	0.68	0.70	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC493xYB	28 Pin SSOP	Commercial, 0°C to + 70°C

NOTE: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
         SC493xYB
         Date Code
         Lot #

IMISC493xYB

         Flow
         B = Commercial, 0°C to + 70° C
         Package
         Y = SSOP
         Revision
         IMI Device Number

OBSOLETE

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