IMISC481D SYSTEM CLOCK CHIP

May 29, 1996

CMOS LSI
PLL FREQUENCY SYNTHESIZER

PRODUCT FEATURES

- Supports Pentium™ system boards with onboard audio peripherals
- Supports synch/semisynchronous PCI bus
- Operates from 5V or 3.3V supply
- Separate CPU clock buffer VDD supports mixed 5V/3.3V outputs
- 60 mA buffer switching current
- Tristate, synch stop clock, and power down modes
- 34 Pin SSOP package for minimum board space

FREQUENCY TABLE

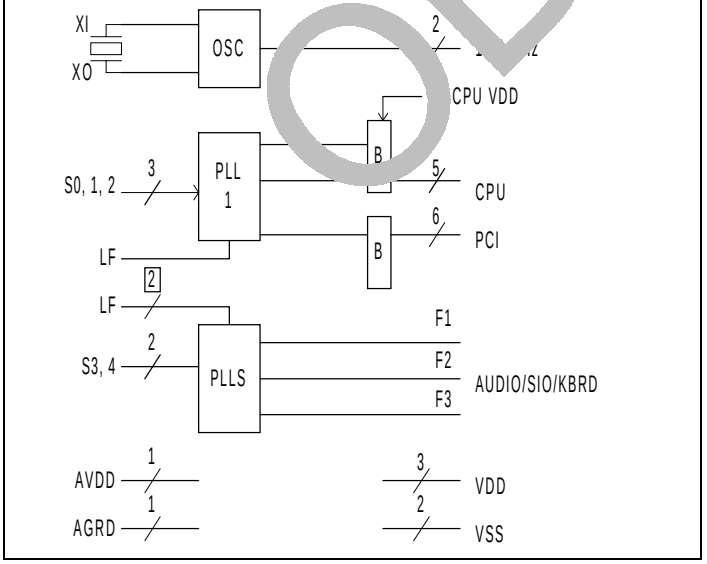
S2	S1	S0	CPU	PCI
0	0	0	55	27.6
0	0	1	66.6	33.3
0	1	0	50	25
0	1	1	60	30
1	0	0	F	33.3*
1	0	1	EXT	EXT/2
1	1	0	TS	TS
1	1	1	SL	SL

*Operates only at VDD = 5V

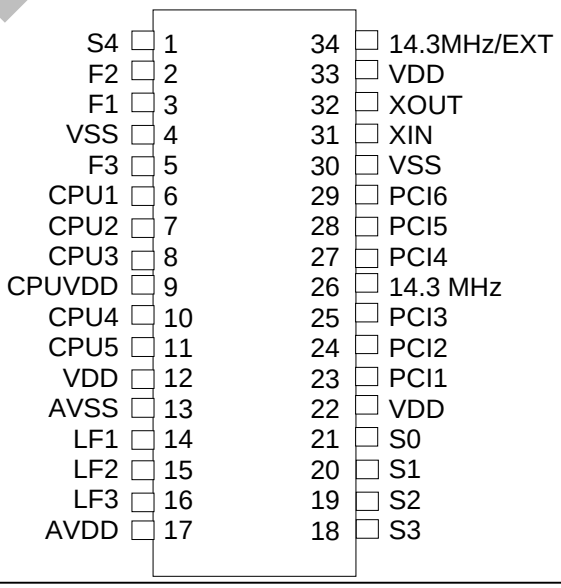
AUDIO/PERIPHERAL CLOCKS

S4	S3	F1	F2	F3
0	0	14.3	12.28	40
0	1	14.3	11.28	40
1	0	48	24	40
1	1	14.3	8.19	40

BLOCK DIAGRAM



CONNECTION DIAGRAM



APPLICATIONS

Pentium™ Systems with multimedia audio capability integrated on the system board.

INTERNATIONAL MICROCIRCUITS, INC. 525 LOS COCHES ST.
MILPITAS, CA 95035 TEL: 408-263-6300 ext. 275 FAX 408-263-6571
Rev. 1.0

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PIN DESCRIPTION

Xin, Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.

S0, S1, and S2 - Standard frequency select inputs. these inputs control the high speed CPU and PCI clock frequency selection. These inputs have internal pull-ups. The output frequency selection is shown on page 1. Selecting the SL (Synchronous Low) state in the frequency table causes the CPU and PCI outputs to remain low after their next regular transition to the low state. Changing from the SL state to a frequency selection state causes the clocks to start after a 3 ms delay to allow for PLL locking. The clocks start at their next simultaneous positive transition. Selecting the tristate causes all CPU, PCI and fixed outputs to enter the tristate condition and the PLLs and Oscillators to stop dissipating power. In the EXT state an externally generated frequency inserted into the 14.3 MHz/EXT Pin is distributed. As shown in the Frequency Select Table.

CPU - Master clock output for CPU frequency generation. Programmable output frequencies can be selected using S0, S1, and S2 inputs as shown on page 1. CPU4 and CPU 5 have double strength drive capability. CPU 1, 2, and 3 have normal drive capability.

PCI - Multiple PCI clock outputs from the PCI clock distribution buffer. Programmable output frequencies are determined by the S0, S1, and S2 inputs as shown on page 1. These clocks are derived from the same PLL as the CPU clock outputs.

14.3 MHz - Buffered output of on-chip reference oscillator or externally supplied reference frequency.

14.3 MHz/EXT - Second oscillator output. Becomes CLK input when EXT mode is selected.

S3 and S4 - Frequency select inputs for clock outputs F1, F2, and F3. These inputs have internal pull-ups to VDD.

F1, F2, and F3 - Frequency outputs for audio, V.S.B, SCSI and SIO. Frequencies selected by S3 and S4 are shown on page 1.

LF1, LF2, LF3 - These are the loop filter outputs for the clock generators. A 0.1 uF capacitor should be connected from this pin to the AVSS pin to form the loop filter. Grounding LF stops the PLL and reduces power dissipation.

VSS - Circuit Digital ground.

VDD - Circuit digital positive power supply.

AVSS - Analog circuit positive power supply.

AVDD - Analog circuit positive power supply.

CPUVDD - 3.3V/5V logic level control for ECPU and CPU outputs. Voltage cannot be greater than VDD.

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 6V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	-55ºC to +125ºC
Recommended Operating Range:	3V -6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input HighCurrent with Pull-up or Pull-down	IIH			5	µA	S0-S4 Inputs
Input Low Current with Pull-up or Pull-down	I			±50		S0-S4 Inputs
Output Low Voltage — IOL = 12 ma	VOL			0.4	Vdc	CPU 1, 2, and 3 Outputs
Output Low Voltage — IOL = 6mA	VOL			0.4	Vdc	All Other Outputs
Output High Voltage — IOH = 12 m	VOH	2.4	-	-	Vdc	CPU 1, 2, and 3 Outputs
Output High Voltage — IO A	VOH	2.4	-	-	Vdc	All Other Outputs
Tri-State leakage Current	Ioz	-	-	10	µA	LF1, LF2, and LF3
Dynamic Supply Current	Icc	-	TBD		mA	CPU = 66.6 MHz, PCI = 33 MHz
Static Supply Current	Icc (PD)	-	TBD	-	µA	-
Short Circuit Current	ISC	25	-	-	mA	-

B1 VDD = 3.3 volts, VDD = 5volts +/- 10% TA = 0ºC to +70ºC

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SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time All Outputs	tTLH, tTHL	-	-	1.5*	ns	15 pf Load
Output Duty Cycle	-	45	50/50	55	%	Measured at 1.5V
CPU to PCI Propagation Delay	tPLH2, tPHL2	0	2	4	n	15 pf Load Measured at 1.5V
Buffer out Skew All CPU and PCI Buffer Outputs	tSKEW	-	-	250	ps	15 pf Load Measured at 1.5V B1in = B2in
ΔPeriod Adjacent Cycles CPU	ΔP	-	±200	-	ps	-
Jitter Absolute CPU	tjab	-		200	ps	-
Input Rise/Fall Time S0-S4			-	2	µs	-
Switching Current Low	IOL (AC)	-	30 ------- 60	-	mA	CPU 1, 2, and 3 Outputs @VOL = 1.5V All Other Outputs
Switching Current High	IOH (AC)	-	28 ------- 50	-	mA	CPU 1, 2, and 3 Outputs @VOL = 1.5V All Other Outputs

B1 VDD = 3.3 Volts VDD = 5 volts +/- 10% TA = 0ºC to 70º C

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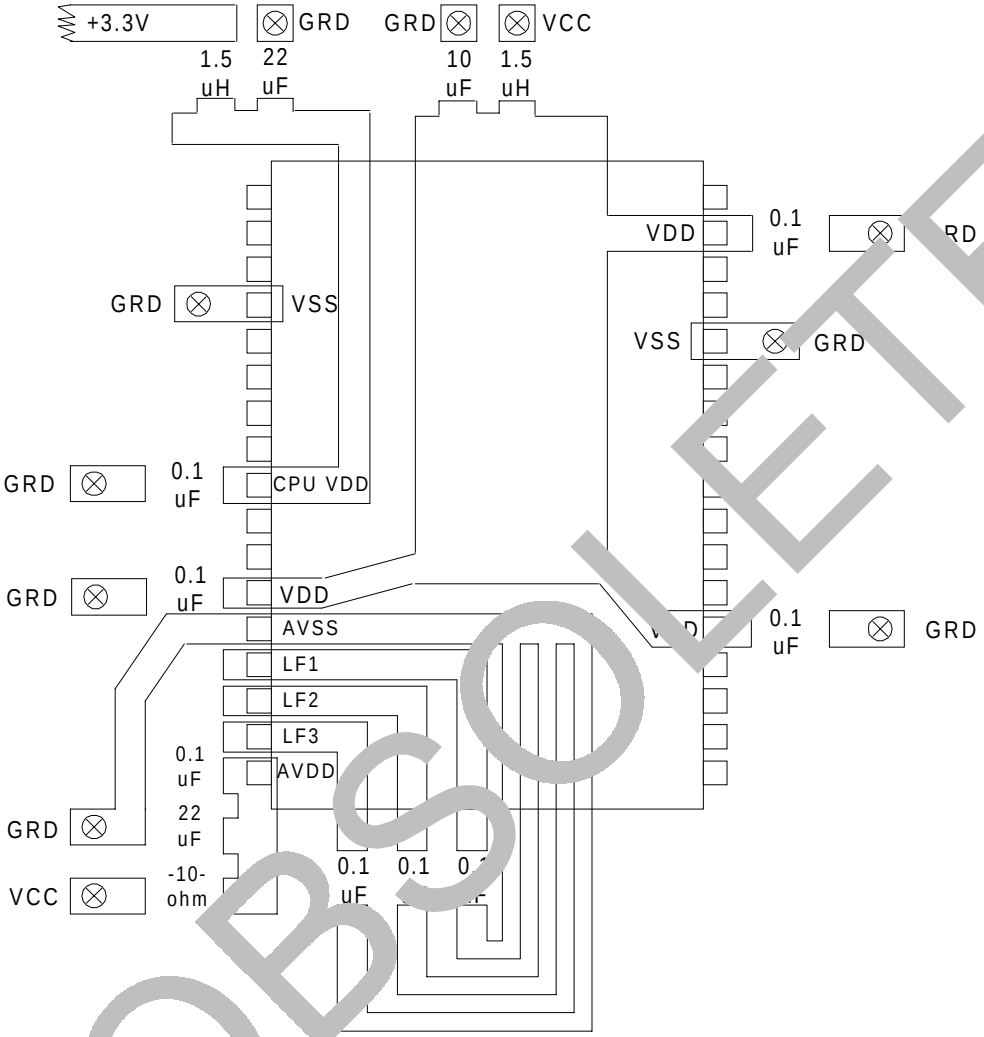
PCB LAYOUT SUGGESTION



NOTES

NOTES:
1. LF CAP MUST BE CONNECTED TO AVSS PIN, NOT GROUND PLANE. IT'S CONNECTION SHOULD NOT BE IN PATH OF CURRENT FLOW FROM AVSS TO GRD.
2. POWER SUPPLY BYPASS CAPS (O.1UF) MUST BE POSITIONED CLOSE TO VDD PINS TO BE EFFECTIVE.
3. TOP LAYER TRACES AND FILTERING TO AVDD / AGRD SEPARATED FROM TRACES TO VDD /VSS PRODUCE BEST PERFORMANCE FOR IMI CLOCK GENERATORS.
4. LF CAPS MUST BE LOW LEAKAGE SUCH AS MULTILAYER CERAMIC Z5U OR X7R MATERIAL.
5. PIN 9 CONNECTION CHANGES WHEN MIXED 5V/3.3V OPERATION IS NOT DESIRED.

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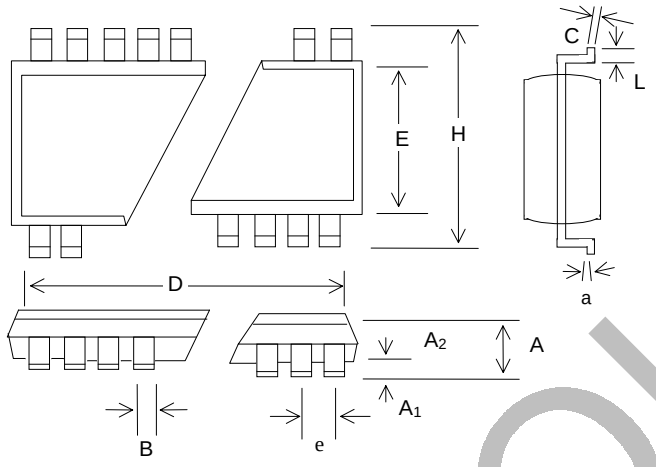
PACKAGE DRAWING AND DIMENSIONS



34 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.97	0.101	0.104	2.46	2.56	2.64
A_1	0.005	0.009	0.0115	0.127	0.22	0.29
A2	0.090	0.092	0.094	2.29	2.34	2.39
B	0.014	0.01	0.019	0.35	0.41	0.48
C	0.0 1	0.010	0.0125	0.23	0.25	0.32
D	0.701	0.706	0.711	17.81	17.93	18.06
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.040 BSC			1.016 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	4º	8º	0º	4º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC481DYB	34 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
C481DYB
Date Code, Lot #

IMISC481DY

Flow
B = Commercial, 0ºC to + 70ºC

Package
Y = SSOP

Revision

IMI Device Number

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