



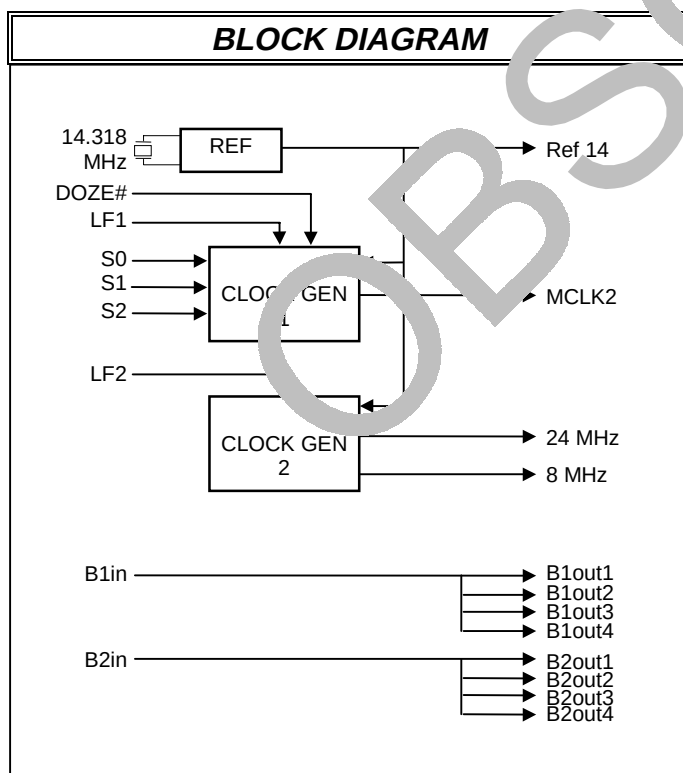
Motherboard Clock Chip

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PRODUCT FEATURES

- Generates all essential clock signals for the Motherboards
- 4V to 7V operating supply range
- Supports 8086, 80286, 80386 and 80486 including S Series® and Pentium™ based designs
- Supports ISA, VESA and PCI based designs
- Supports GREEN PC applications
- On-chip dual QUAD buffers
- Integrates CPU clock and buffered 14.318 Mhz output
- Wide range of selectable output frequencies including 80, 66.6, 60, 50, 40, 33.3, 16 and 8 Mhz
- Doze mode for low power consumption
- single, low cost crystal (14.318 Mhz) used as reference frequency
- Smooth and glitch-free switching during DOZE# to be active
- 50% duty cycle
- TTL or CMOS compatible outputs
- Low, short and long term jitter
- 28 PDIP and 28 Pin SSOP (209 mil body) packages options

BLOCK DIAGRAM



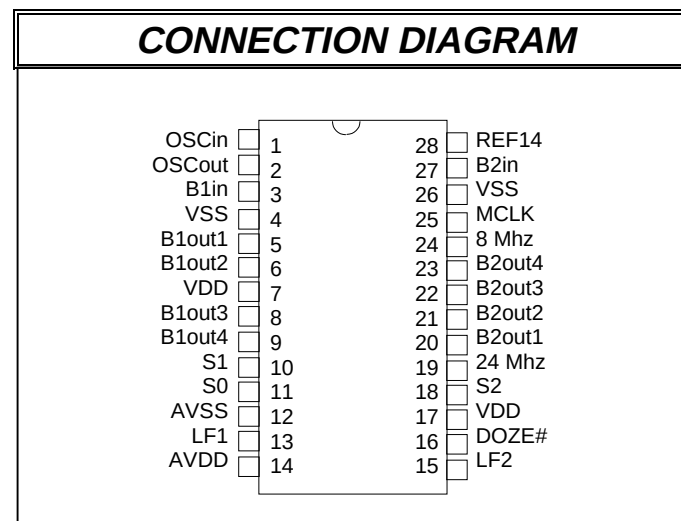
PRODUCT DESCRIPTION

The IMISC468 is a clock chip for Motherboards. The IMISC468 includes two independent VCO's and uses a single 14.318 Mhz external crystal to generate all essential clock signals. The IMISC468 is designed to generate CPU clock options of 80 Mhz, 66.6 Mhz, 60 Mhz, 50 Mhz, 40 Mhz, 33.3 Mhz, 16 Mhz and 8 Mhz, giving flexibility to the user. The frequency selection on the MCLK outputs is determined by the S0-S2 pins. A second fixed frequency clock generator provides 24 Mhz and 8 Mhz. In addition, the REF14 output provides a buffered (14.318 Mhz) output. DOZE# pin gives additional flexibility to the user for Green PC applications. Activating the doze# pin smoothly switches the MCLK output to preprogrammed DOZE frequencies. Deactivating the DOZE input allows the CPU output to return to full speed. On-chip buffers provide the needed buffering for PCI or VESA applications.

FREQUENCY TABLE (MHz)

INPUTS			MCLK OUTPUT	
	S1	S0	DOZE# = 1	DOZE# = 0
0	0	0	66.6	16
0	0	1	80	16
0	1	0	60	33.3
0	1	1	30	8
1	0	0	33.3	8
1	0	1	40	8
1	1	0	50	16
1	1	1	25	8

CONNECTION DIAGRAM





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PIN DESCRIPTION					
PIN No.	Pin Name	PWR	I/O	TYPE	Description
1	OSCin	VDD	I	PAD	These pins form an on-chip referenced oscillator when connected to terminal of an external parallel resonant crystal (nominally 14.318 Mhz). OSCin may also serve as input for an externally generated reference signal.
2	OSCout	VDD	O	PAD	
3	B1in	VDD	I	PAD	On-chip buffer inputs. These pins have internal pull-ups.
27	B2in	VDD	I	PAD	
5, 6, 8, 9	B1out1, B1out2, B1out3, B1out4	VDD	O	BUF	Buffered output pins of B1in. These buffers are capable to sink or source 12 ma. they can be used to buffer critical clock lines for PCI or VESA applications.
10, 11, 18	S0:2	VDD	I	PAD	Standard frequency select inputs. These inputs control the high speed CLK frequency selection. S0-S2 inputs controls the CPU clock frequencies. All these inputs have internal pull-ups.
4, 26	VSS	-	-	PWR	Ground pins for the device.
7,17	VDD	-	-	PWR	Positive Power Supply.
12	AVSS	-	-	PWR	Analog circuit ground.
13, 15	LF1, LF2	VDD	-	PAD	These are the phase detector outputs for the clock generators. They are single-ended, tri-state output for use as loop error signal. A 0.1 uF capacitor to ground should be connected from this pin to form the loop filter.
16	DOZE#	VDD	I	PAD	DOZE control pin. When DOZE# is high, the clock chip operates in the standard mode. When this pin goes low, output frequencies are switched to the pre-programmed DOZE frequencies. Switching to DOZE frequencies occur smoothly to allow tracking by 486 CPU internal PLL. this pin has an internal pull-up.
19	24 Mhz	VDD	O	BUF	24 Mhz floppy drive clock output.
20, 21, 22, 23	B2out1, B2out2, B2out3, B2out4	VDD	O	BUF	Buffered output pins of B2in. These buffers are capable to sink or source 12 ma. They can be used to buffer critical clock lines for PCI or VESA applications.
24	8 Mhz	VDD	O	BUF	8 Mhz keyboard clock output.
25	CLK	VDD	O	BUF	Master clock output. Programmable output frequencies can be selected using S0-S2 inputs.
28	REF14	VDD	O	BUF	14.31818 Mhz output. Buffered output of on-chip reference oscillator or externally provided referenced.



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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 7V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0°C to + 125°C
Operating Temperature:	0°C to +70°C
Recommended Operating Range:	4V - 7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be contained to the range:

$$VSS \leq V_{in} \text{ or } V_{out} \leq VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	-	Vdc	S0-S2 Inputs
Input High Voltage	VIH	2.0	-	-	Vdc	S0-S2 Inputs
Input Low Voltage	VIL	-	-	0.8	Vdc	B1in, B2in Inputs
Input High Voltage	VIH	2.0	-	-	Vdc	B1in, B2in Inputs
Input Low Current with Pull-up or Pull-down	IIL	-	-	5 ± 50	μA	S0-S2 Input
Input High Current with Pull-up or Pull-down	IIH	-	-	5 ± 50	μA	
Output Low Voltage IOL = 12 mA	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH = 12 mA	VOH	2.4	-	-	Vdc	All Outputs
Tri-State Leakage Current	ICL	-	-	10	μA	LF1, LF2
Dynamic Supply Current	ICC	-	-	35	mA	VDD@5V, MCLK2 = 50 Mhz
Short Circuit Current	ISC	25	-	-	mA	

VDD = 5V $\pm$ 10%, TA = 0°C to + 70°C



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SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) Time All Outputs	t _{TLH} , t _{THL}	-	-	2	nS	30 pf Load
Duty Cycle MCLK and REF14		-	50/50	45/55	%	
Propagation Delay Bin to Bout	t _{PLH} , t _{PHL}	2.0	3.2	4.2	nS	15 pf Load Measured at 1.4V
Buffer out Skew B1out1-B1out4 or B2out1-B2out4	t _{SKEW}	-	-	250	ps	15 pf Load Measured at 1.4V
Jitter One Sigma MCLK and REF14	t _{j1s}	-	-	± 2	%	As compared with clock period
Jitter Absolute MCLK and REF14	t _{jab}	-	-	± 5	%	As compared with clock period
Input Rise/Fall Time S0-S2		-	-	2	us	note1

VDD = 5V ± 10%, TA = 0°C to + 70°C

OSCILLATOR CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Transconductance	gm	10	330	-	millimhos	@ 14.3 Mhz
Output Impedance	Z _o	-	200	800	ohms	@ 14.3 Mhz
Input Capacitance	C _i	8	13	18	pf	
Output Capacitance	C _o	-	6	9	pf	
DC Bias Voltage	VB	1.5	VDD/2	3.5	Volt	
Start-up Time	t _s	-	-	10	ms	@ 14.3 Mhz
Input Rise Time OSCIN	ICLK _r	-	-		us	
Input Fall Time OSCIN	ICLK _f	-	-	2	us	

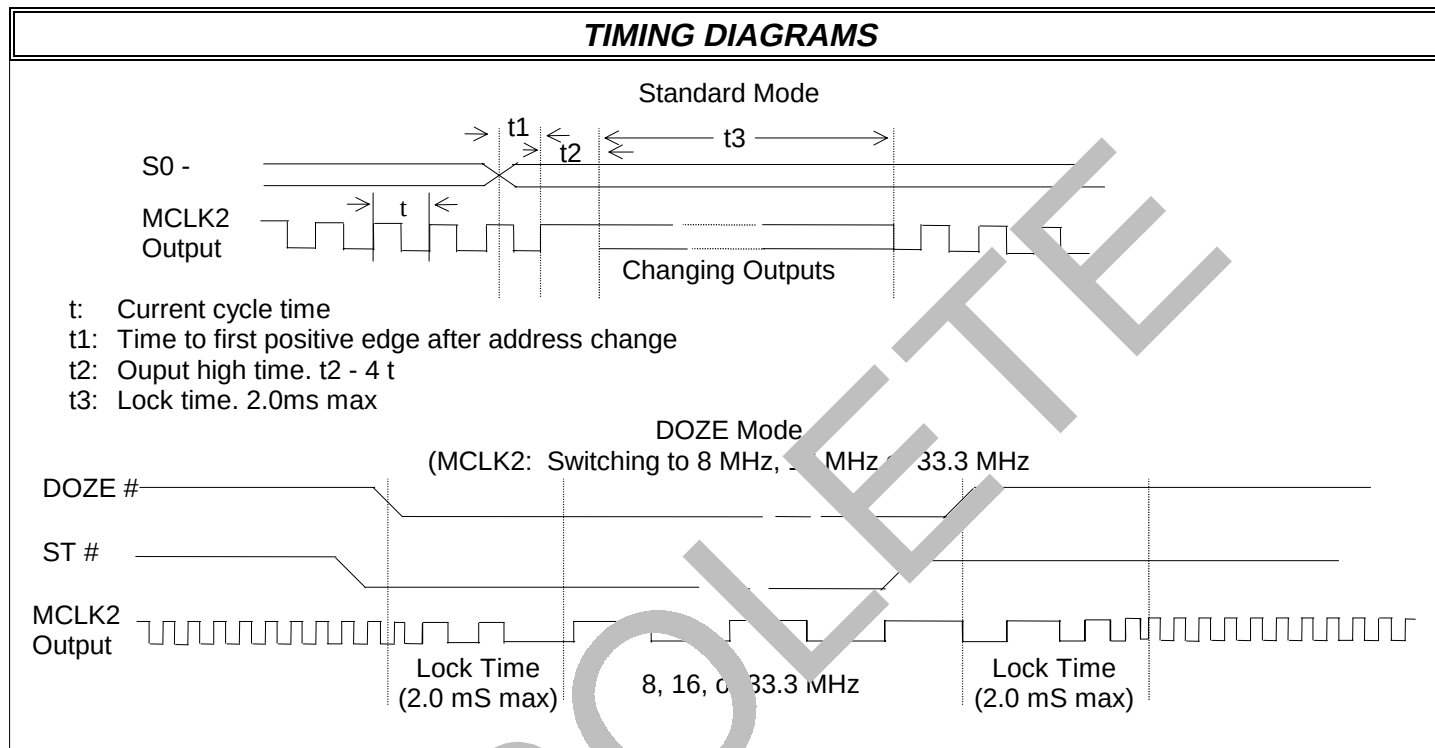
VDD = 5V ± 10%, TA = 0°C to + 70°C



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TIMING DIAGRAMS



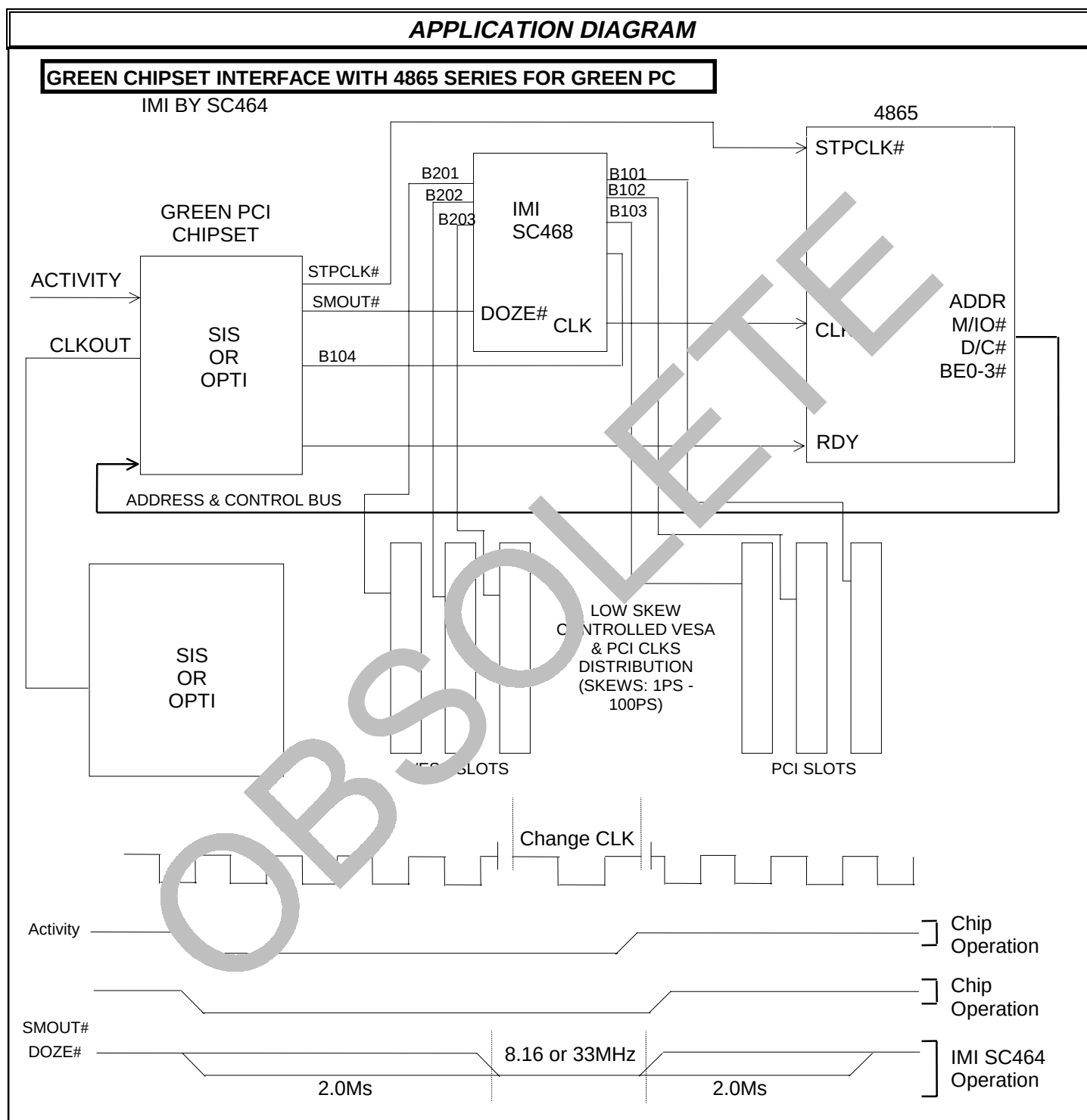


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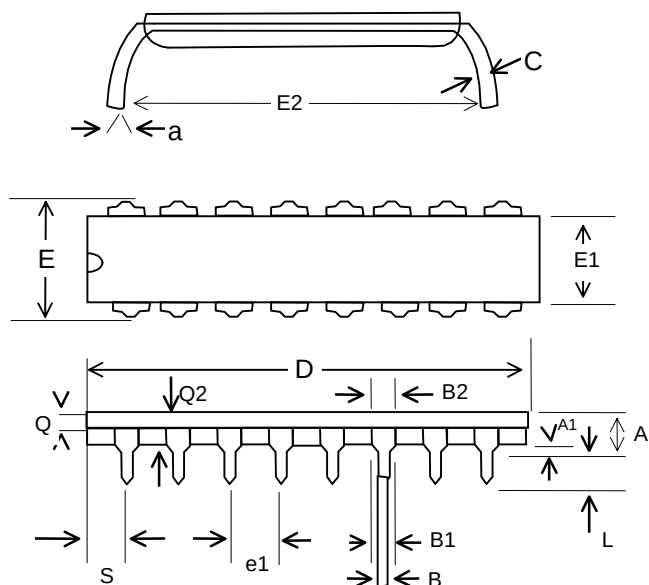




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PACKAGE DRAWING AND DIMENSIONS



28 PIN SKINNY PLASTIC DIP DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.50	-	-	4.57
A ₁	0.020	-	-	0.51	-	-
B	0.015	0.020	0.025	0.38	0.46	0.51
B ₁	0.045	0.050	0.055	1.14	1.27	1.40
B ₂	0.035	0.040	0.045	0.89	1.02	1.14
C	0.008	0.010	0.012	0.20	0.25	0.30
D	0.360	1.365	1.370	34.54	34.67	34.80
E	0.300	-	0.325	7.62	-	8.255
E ₁	0.282	0.282	0.284	7.11	7.16	7.2
E ₂	0.282	0.284	0.286	7.16	7.21	7.25
e ₁	0.000 BSC			2.54 BSC		
L	0.125	0.130	0.135	3.18	3.30	3.43
a	0°	7°	15°	0°	7°	15°
Q ₂	0.055	0.060	0.065	1.40	1.52	1.65
S	-	0.130	-	-	3.30	-
S	0.028	0.033	0.038	0.71	0.84	0.97

28 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.08	0.073	0.078	1.73	1.8	1.99
A ₁	0.002	0.005	0.008	0.05	0.13	0.21
A ₂	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95



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ORDERING INFORMATION		
Part Number	Package Type	Production Flow
IMISC468APB	Plastic Dip	Commercial, 0°C to +70°C
IMISC468AYB	SSOP	

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC468APB
Date Code, Lot #

IMISC468APB

Flow

B = Commercial, 0°C to + 70°C

Package

P = Plastic Dip

Y = SSOP

Revision

IMI Device Number