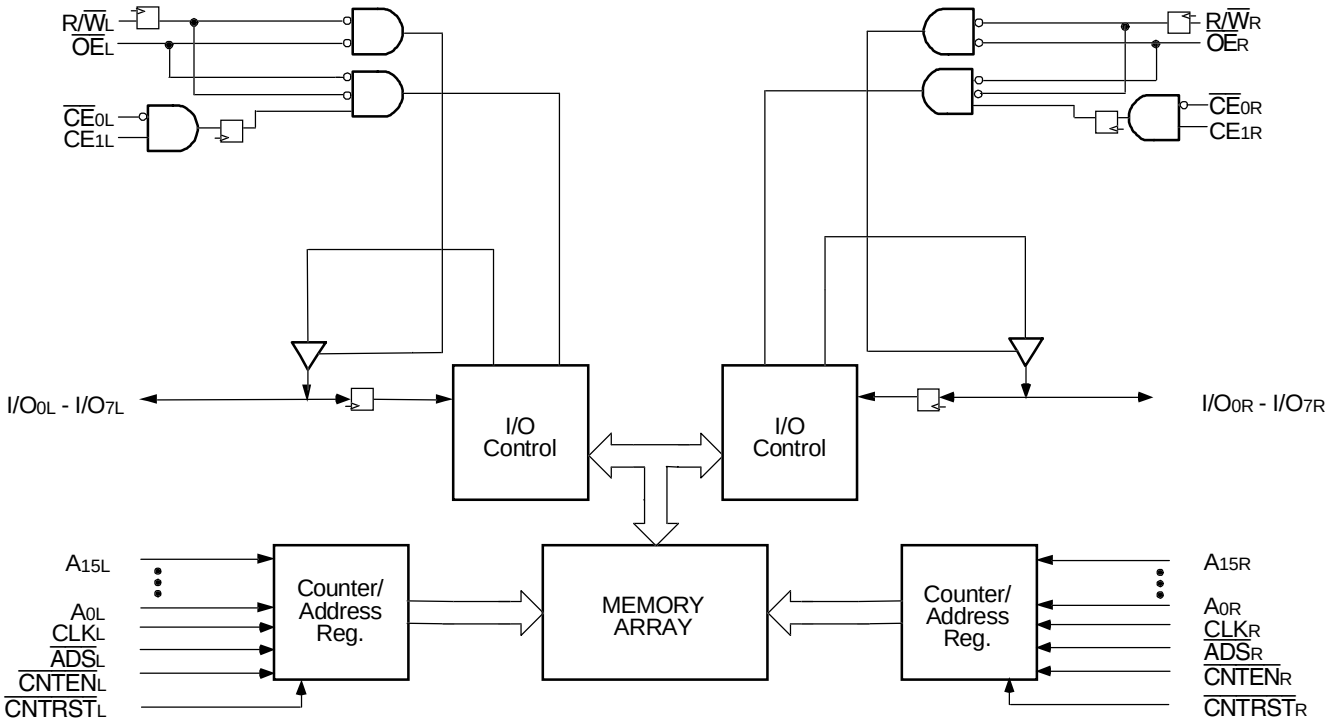
HIGH-SPEED 64K x 8 SYNCHRONOUS DUAL-PORT STATIC RAM

PRELIMINARY
IDT70908S/L

Features:

- **True Dual-Ported memory cells which allow simultaneous access of the same memory location**
- **High-speed clock to data access**
  - *Commercial: 20/25/30ns (max.)*
- **Low-power operation**
  - *IDT70908S*
    Active: 950mW (typ.)
    Standby: 5mW (typ.)
  - *IDT70908L*
    Active: 950mW (typ.)
    Standby: 1mW (typ.)
- **Flow-Through output mode.**
- **Counter enable and reset features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Full synchronous operation on both ports**
  - *4ns setup to clock and 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 20ns clock to data out*
  - *Self-timed write allows fast cycle time*
  - *25ns cycle time, 40MHz operation*
- **Separate upper-byte and lower-byte control for multiplexed bus and bus matching compatibility**
- **TTL- compatible, single 5V (±10%) power supply**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Available in 84-pin Pin Grid Array (PGA) and 100-pin Thin Quad Flatpack (TQFP) packages**

Functional Block Diagram



3200 drw 01

JUNE 1999

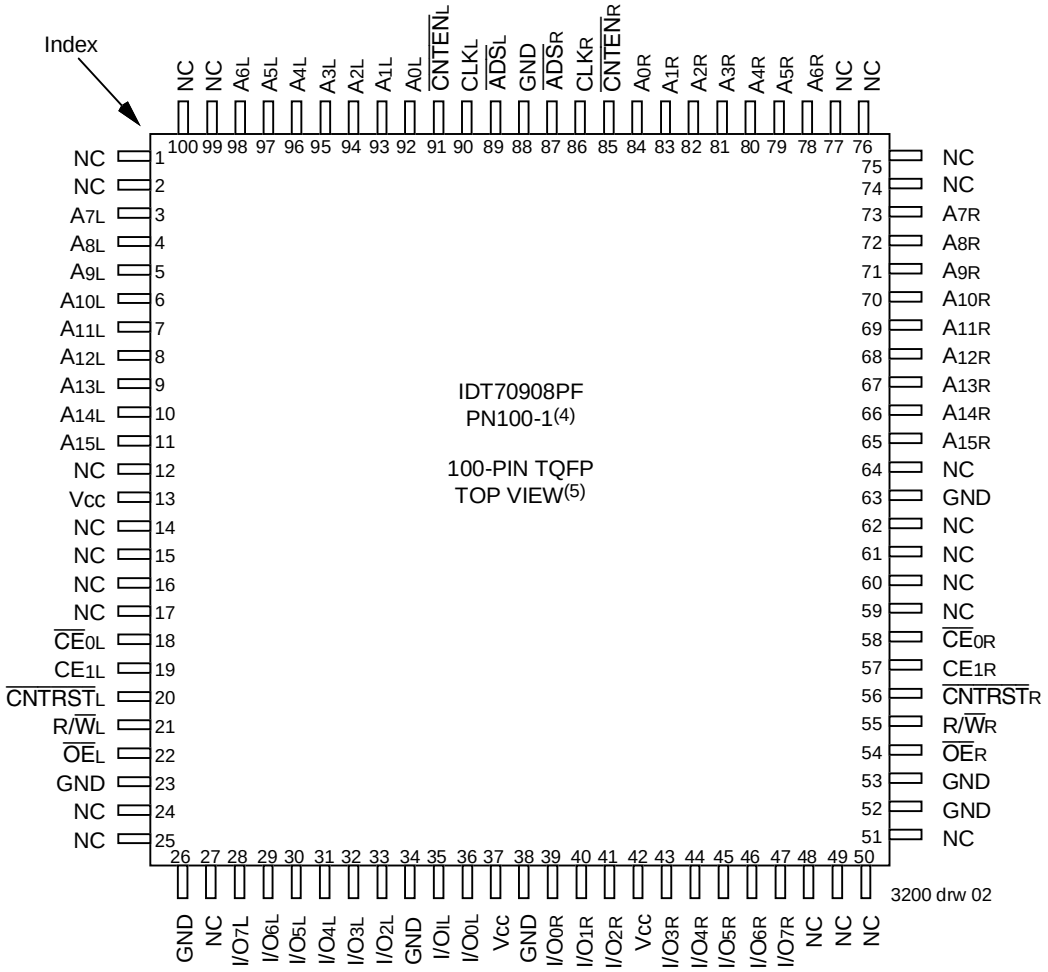
©1999 Integrated Device Technology, Inc.

Description:

The IDT70908 is a high-speed 64K x 8 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70908 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 950mW of power.

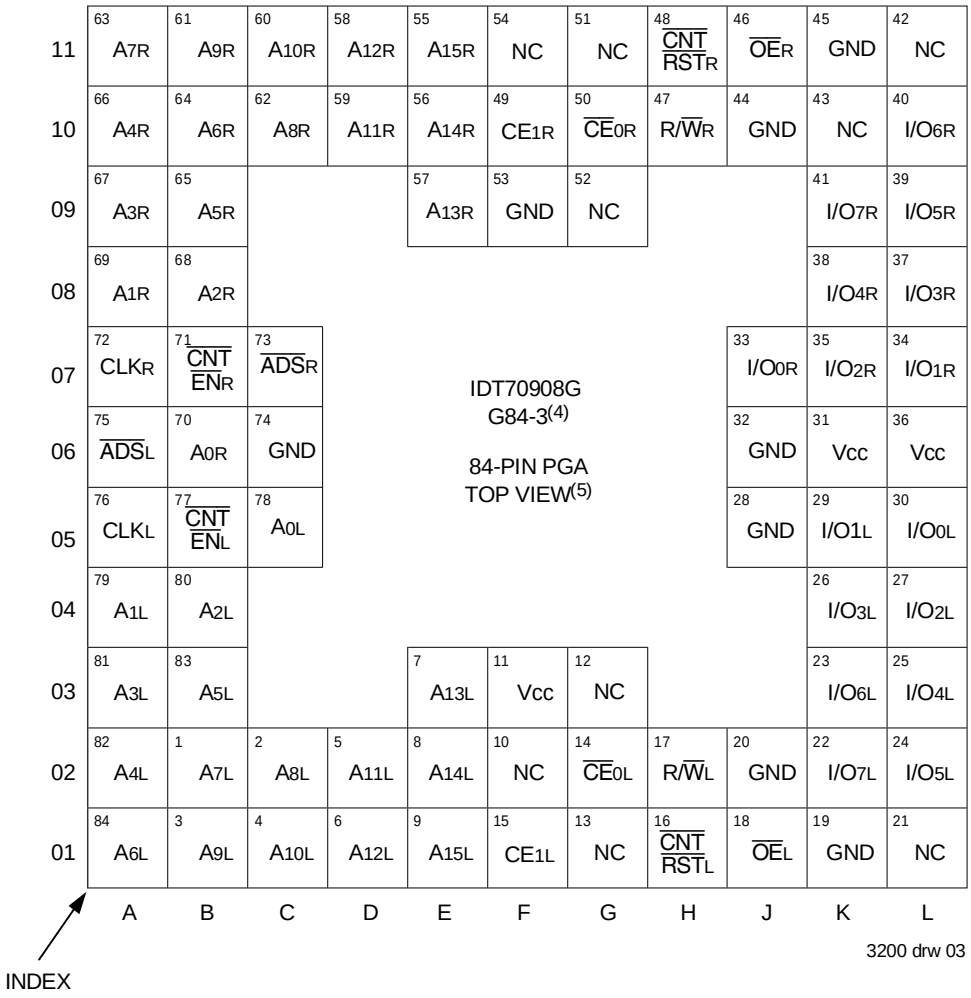
Pin Configurations[1,2,3]



NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations[1,2,3] (con't.)



	A	B	C	D	E	F	G	H	J	K	L
11	63 A7R	61 A9R	60 A10R	58 A12R	55 A15R	54 NC	51 NC	48 $\overline{CNT}$/$\overline{RST}$R	46 $\overline{OE}$R	45 GND	42 NC
10	66 A4R	64 A6R	62 A8R	59 A11R	56 A14R	49 CE1R	50 $\overline{CE}$0R	47 R/$\overline{W}$R	44 GND	43 NC	40 I/O6R
09	67 A3R	65 A5R			57 A13R	53 GND	52 NC			41 I/O7R	39 I/O5R
08	69 A1R	68 A2R								38 I/O4R	37 I/O3R
07	72 CLKR	71 $\overline{CNT}$/$\overline{EN}$R	73 $\overline{ADS}$R						33 I/O0R	35 I/O2R	34 I/O1R
06	75 $\overline{ADS}$L	70 A0R	74 GND						32 GND	31 Vcc	36 Vcc
05	76 CLKL	77 $\overline{CNT}$/$\overline{EN}$L	78 A0L						28 GND	29 I/O1L	30 I/O0L
04	79 A1L	80 A2L								26 I/O3L	27 I/O2L
03	81 A3L	83 A5L			7 A13L	11 Vcc	12 NC			23 I/O6L	25 I/O4L
02	82 A4L	1 A7L	2 A8L	5 A11L	8 A14L	10 NC	14 $\overline{CE}$0L	17 R/$\overline{W}$L	20 GND	22 I/O7L	24 I/O5L
01	84 A6L	3 A9L	4 A10L	6 A12L	9 A15L	15 CE1L	13 NC	16 $\overline{CNT}$/$\overline{RST}$L	18 $\overline{OE}$L	19 GND	21 NC

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 1.12in x 1.12in x .16in
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}$L, CE1L	$\overline{CE}$R, CE1R	Chip Enable
R/$\overline{W}$L	R/$\overline{W}$R	Read/Write Enable
$\overline{OE}$L	$\overline{OE}$R	Output Enable
A0L - A15L	A0R - A15R	Address
I/O0L - I/O7L	I/O0R - I/O7R	Data Input/Output
CLKL	CLKR	Clock
$\overline{ADS}$L	$\overline{ADS}$R	Address Strobe
$\overline{CNTEN}$L	$\overline{CNTEN}$R	Counter Enable
$\overline{CNTRST}$L	$\overline{CNTRST}$R	Counter Reset
VCC		Power
GND		Ground

3200 tbl 01

Truth Table I—Read/Write and Enable Control(1,2,3)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	R/$\overline{W}$	I/O_{0-7}	Mode
X	↑	H	X	X	High-Z	Deselected
X	↑	X	L	X	High-Z	Deselected
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

3200 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control(1,2)

Address	Previous Address	CLK	ADS	CNTEN	CNTRST	I/O	Mode
X	X	↑	H	H	L	$D_{I/O(0)}$	Counter Reset to Address 0
An	X	↑	L(3)	H	H	$D_{I/O(n)}$	External Address Utilized
X	An	↑	H	H	H	$D_{I/O(n)}$	External Address Blocked—Counter Disabled
X	An	↑	X	L(4)	H	$D_{I/O(n+1)}$	Counter Enable—Internal Address Generation

3200 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{CE}_0$, $\overline{LB}$, $\overline{UB}$, and $\overline{OE}$ = V_{IL}; CE_1 and R/$\overline{W}$ = V_{IH}.
3. ADS is independent of all other signals including $\overline{CE}_0$ and CE_1.
4. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{CE}_0$ and CE_1.

Recommended Operating Temperature and Supply Voltage[1,2]

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3200 tbl 04

NOTES:
1. This is the parameter T_A
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Maximum DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[1]	V
V_{IL}	Input Low Voltage	-0.5[2]	—	0.8	V

3200 tbl 05

NOTES:
1. V_{TERM} must not exceed V_{CC} + 10%.
2. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

3200 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 10%.

Capacitance[1]

(T_A = +25°C, f = 1.0MHz) TQFP Only

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10	pF

3200 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	70908S/L		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

3200 tbl 08

NOTE:
1. At Vcc ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(6,7) (Vcc = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		70908X20 Com'l Only Typ.(4)	70908X20 Com'l Only Max.	70908X25 Com'l Only Typ.(4)	70908X25 Com'l Only Max.	70908X30 Com'l Only Typ.(4)	70908X30 Com'l Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL} Outputs Open f = f_{MAX}(1)	COM'L	S	210	390	200	345	190	325	mA
				L	210	350	200	305	190	285	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}(1)	COM'L	S	50	135	50	110	50	110	mA
				L	50	115	50	90	50	90	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(3) Active Port Outputs Open, f=f_{MAX}(1)	COM'L	S	140	270	130	230	120	220	mA
				L	140	240	130	200	120	190	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0(2)	COM'L	S	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V(5) $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Open, f = f_{MAX}(1)	COM'L	S	130	245	120	205	110	195	mA
				L	130	225	120	185	110	175	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	

3200 tbl 09

NOTES:

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. Vcc = 5V, T_A = 25°C for Typ, and are not production tested. $I_{CC\,DC}$(f=0) = 150mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and $CE_{1X} \geq V_{CC}$ - 0.2V
   $\overline{CE}_X \geq V_{CC}$ - 0.2V means $\overline{CE}_{0X} \geq V_{CC}$ - 0.2V or $CE_{1X} \leq$ 0.2V
   "X" represents "L" for left port or "R" for right port.
6. 'X' in part number indicate power rating (S or L).
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3200 tbl 10

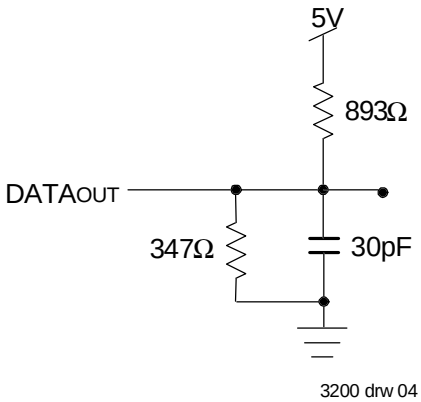


Figure 1. AC Output Test load.

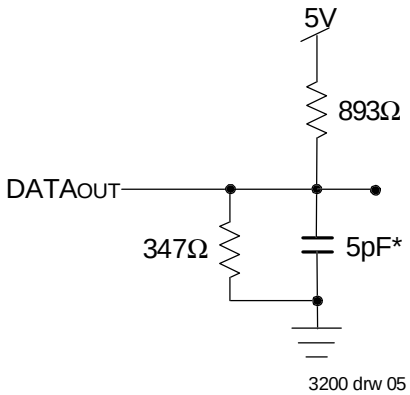


Figure 2. Output Test Load (For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

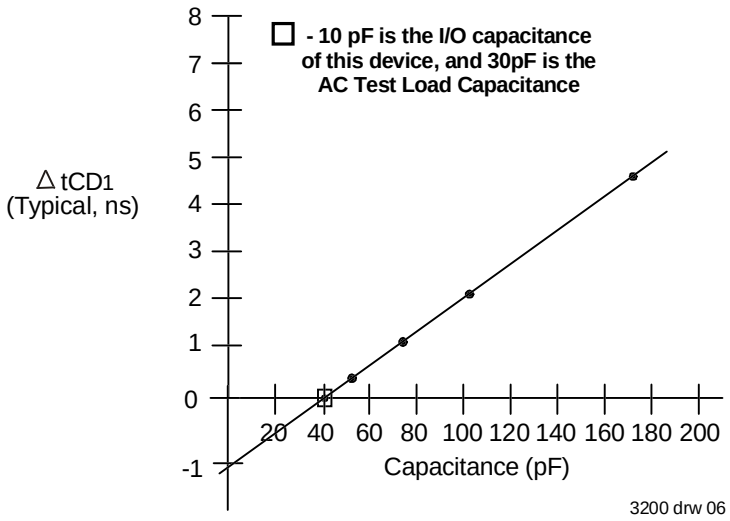


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[2,3,4]

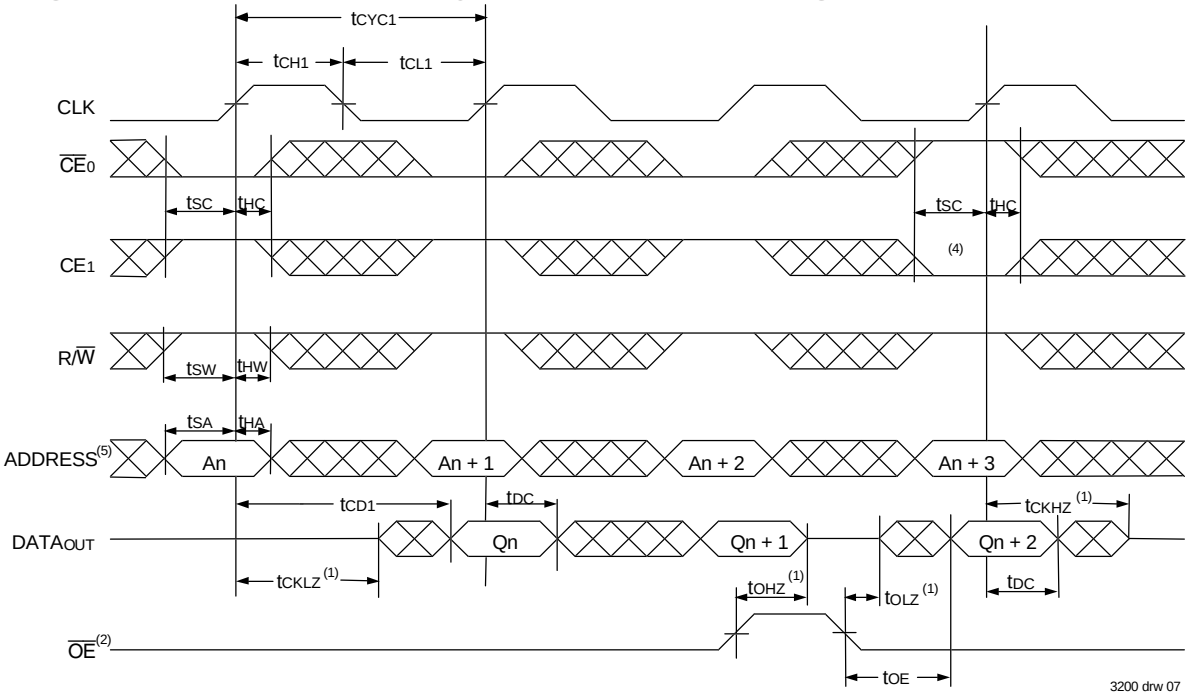
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		70908X20 Com'l Only		70908X25 Com'l Only		70908X30 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)[2]	25	—	30	—	35	—	ns
t_{CH1}	Clock High Time (Flow-Through)[2]	12	—	12	—	12	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[2]	12	—	12	—	12	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	4	—	4	—	4	—	ns
t_{HA}	Address Hold Time	1	—	1	—	1	—	ns
t_{SC}	Chip Enable Setup Time	4	—	4	—	4	—	ns
t_{HC}	Chip Enable Hold Time	1	—	1	—	1	—	ns
t_{SW}	R/$\overline{W}$ Setup Time	4	—	4	—	4	—	ns
t_{HW}	R/$\overline{W}$ Hold Time	1	—	1	—	1	—	ns
t_{SD}	Input Data Setup Time	4	—	4	—	4	—	ns
t_{HD}	Input Data Hold Time	1	—	1	—	1	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	4	—	4	—	4	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	1	—	1	—	1	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	4	—	4	—	4	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	1	—	1	—	1	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	4	—	4	—	4	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	1	—	1	—	1	—	ns
t_{OE}	Output Enable to Data Valid	—	12	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z[1]	2	—	2	—	2	—	ns
t_{OHZ}	Output Disable to Output High-Z[1]	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[2]	—	20	—	25	—	30	ns
t_{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1]	2	9	2	9	2	9	ns
t_{CKLZ}	Clock High to Output Low-Z[1]	2	—	2	—	2	—	ns
Port-to-Port Delay								
t_{CWDD}	Write Port Clock High to Read Data Delay	—	40	—	40	—	50	ns
t_{CCS}	Clock-to-Clock Setup Time	—	15	—	15	—	20	ns

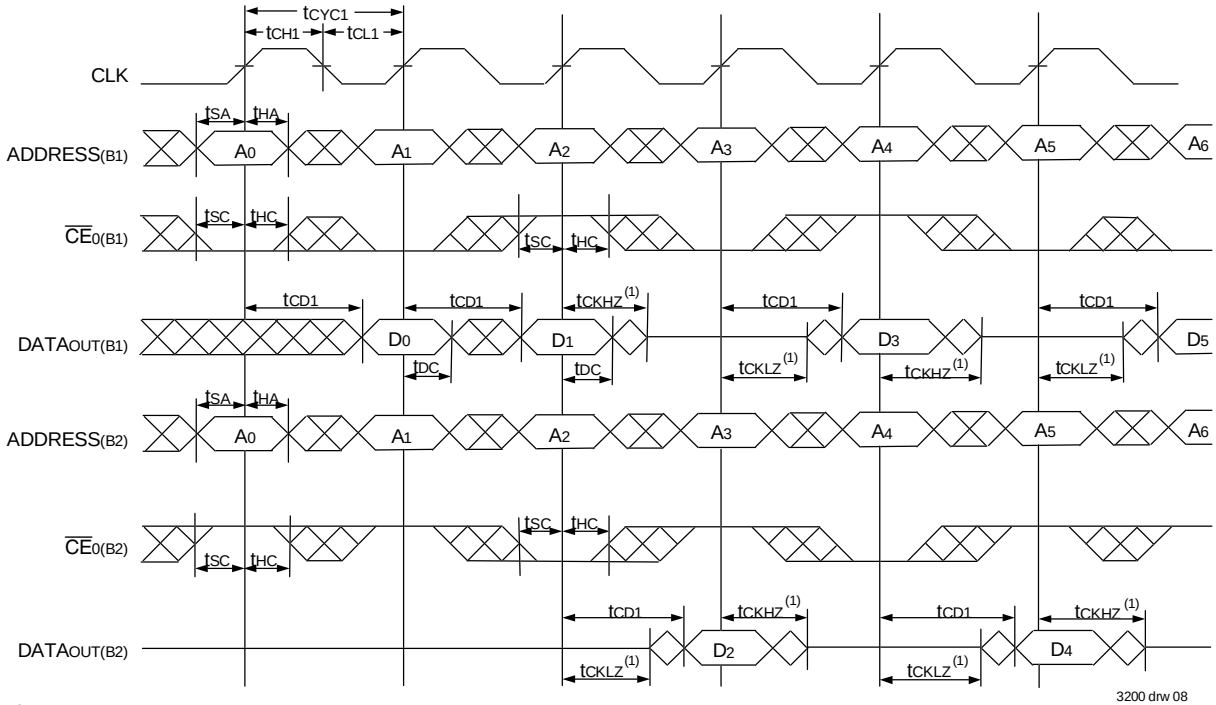
3200 tbl 11

NOTES:
1. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$).
3. 'X' in part number indicates power rating (S or L).
4. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Read Cycle for Flow-Through Output(3)



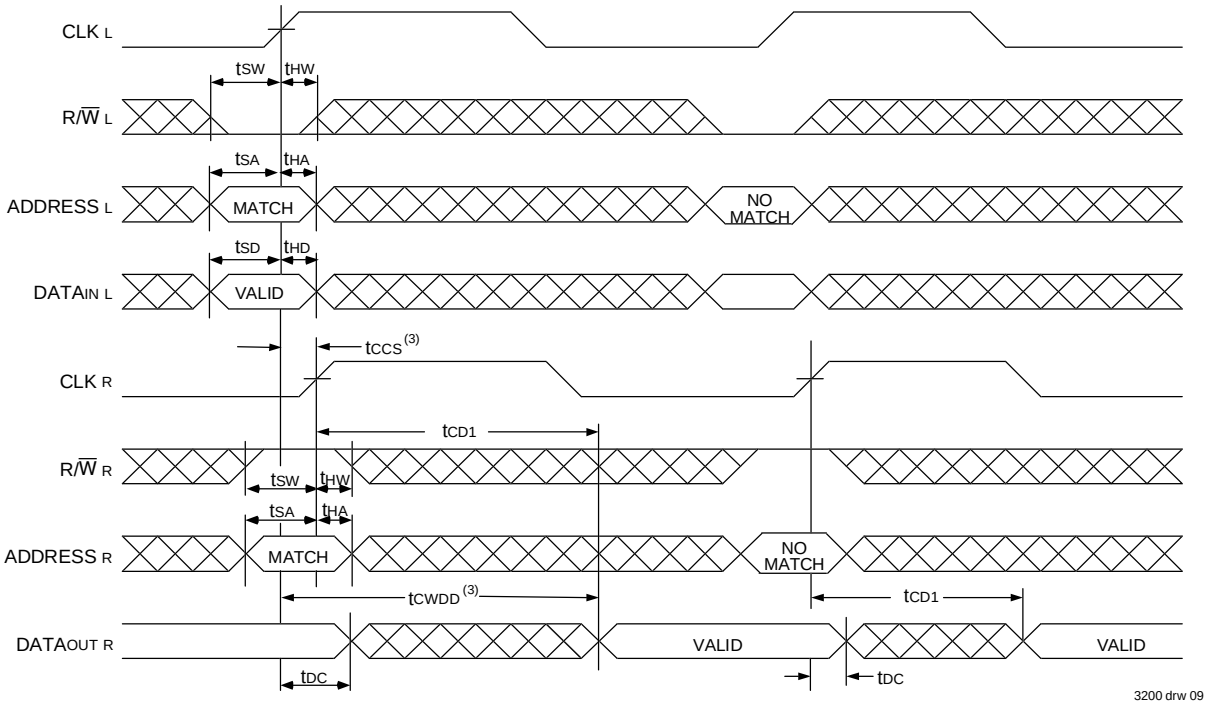
Timing Waveform of a Bank Select Flow-Through Read(6,7)



NOTES:

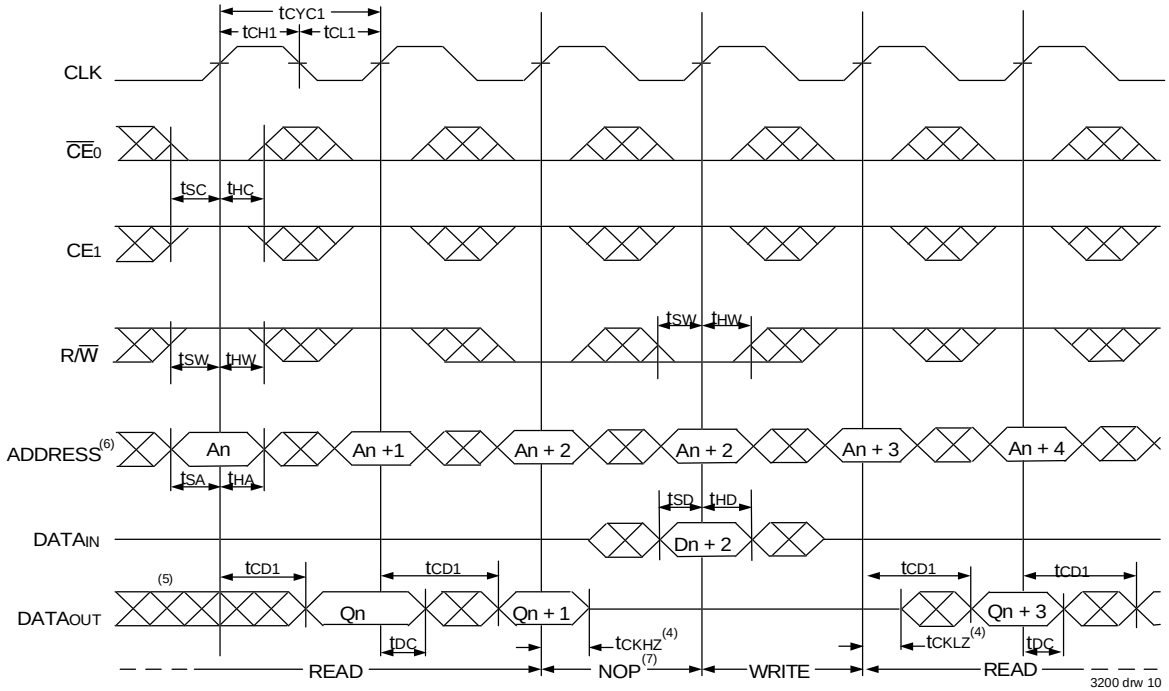
1. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
4. The output is disabled (High-impedance state) by $\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}.
5. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70908 for this waveform.
   $ADDRESS_{(B1)}$ = $ADDRESS_{(B2)}$ in this situation.
7. $\overline{CE}_{0(B2)}$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.

Timing Waveform of Left Port Write to Flow-Through Right Port Read(1,2)



3200 drw 09

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(1)

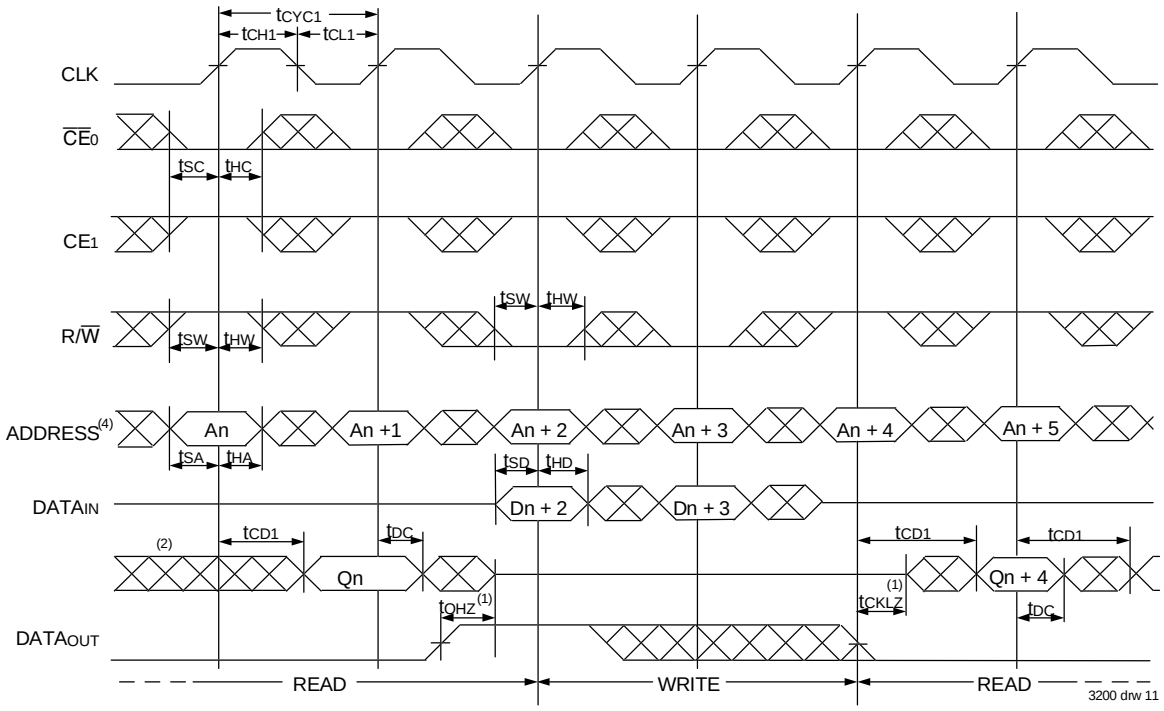


3200 drw 10

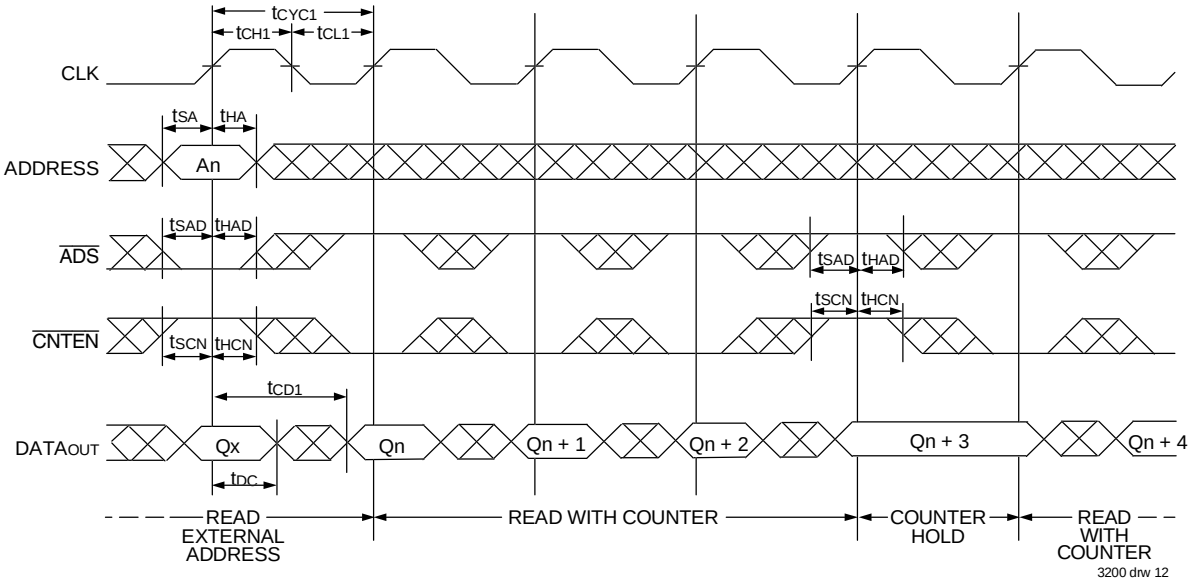
NOTES:

1. $\overline{CE}_0$ and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH.
2. $\overline{OE}$ = VIL for the Right Port, which is being read from. $\overline{OE}$ = VIH for the Left Port, which is being written to.
3. If tCCS ≤ maximum specified, then data from right port READ is not valid until the maximum specified for tCWDD.
   If tCCS > maximum specified, then data from right port READ is not valid until tCCS + tCD1. tCWDD does not apply in this case.
4. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
5. Output state (High, Low, or High-impedance is determined by the previous cycle control signals.
6. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
7. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to gaurantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)



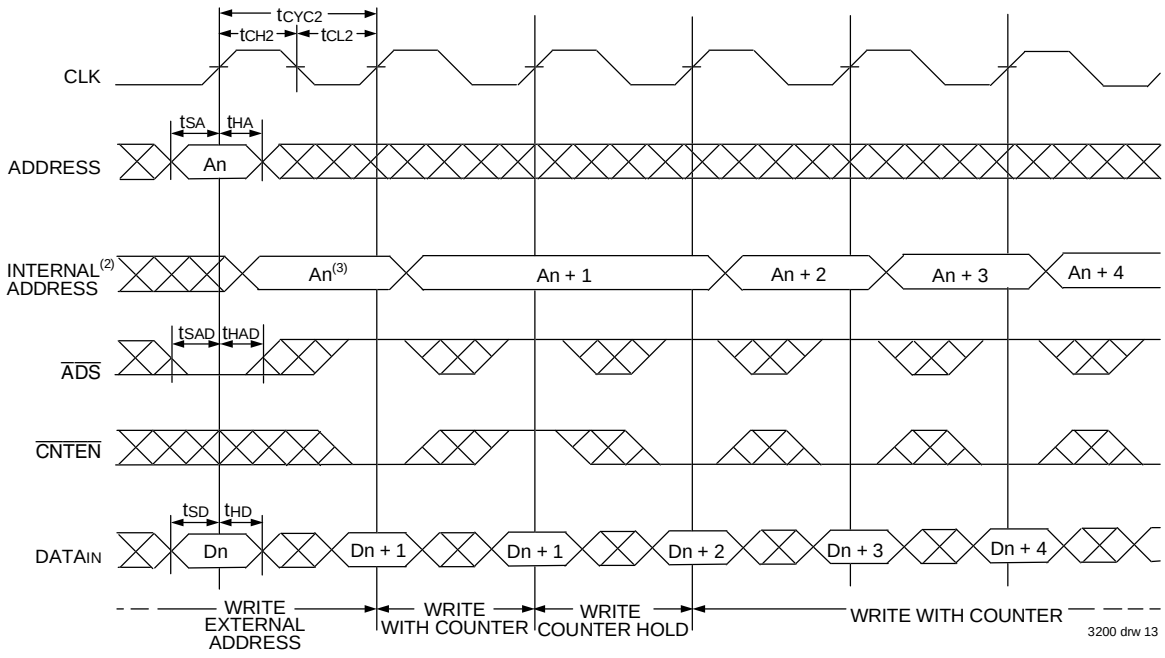
Timing Waveform of Flow-Through Read with Address Counter Advance(3)



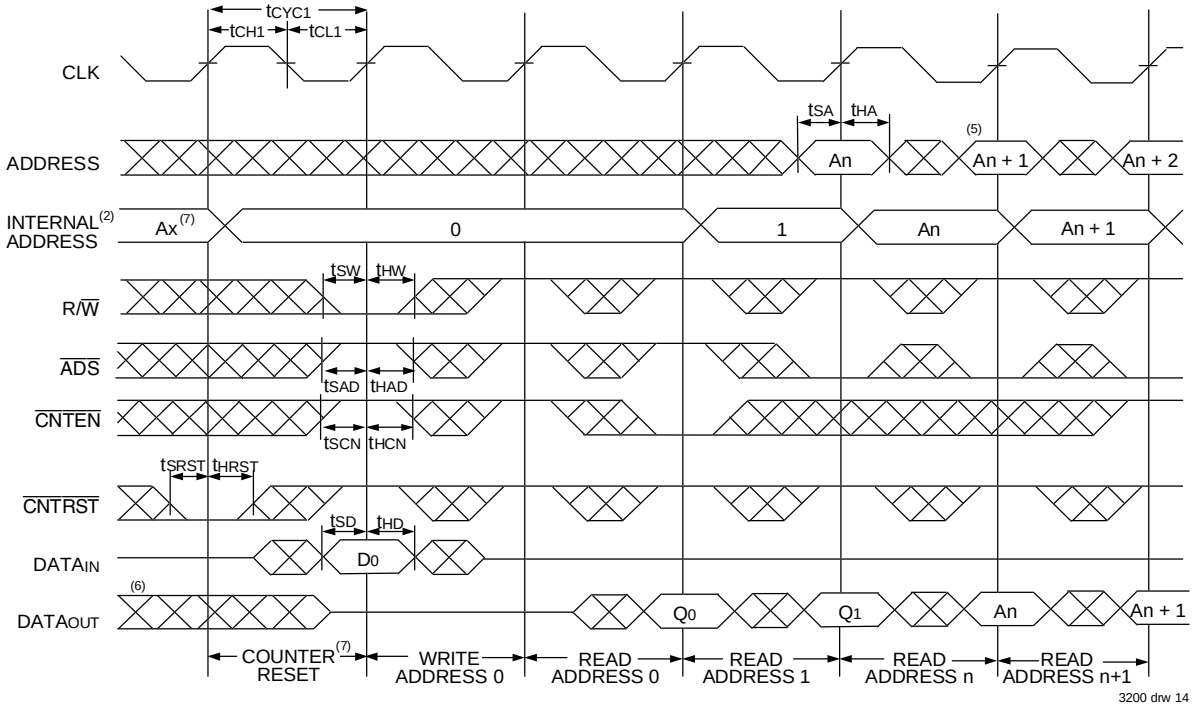
NOTES:

1. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance is determined by the previous cycle control signals.
3. $\overline{CE_0}$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since ADS = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.

Timing Waveform of Write with Address Counter Advance(1)



Timing Waveform of Counter Reset(4)



NOTES:

1. $\overline{CE_0}$ and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$= V_{IH}.
2. The Internal Address is equal to the External Address when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
3. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.
4. $\overline{CE_0}$ = V_{IL}; CE_1 = V_{IH}.
5. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
7. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset. $ADDR_0$ will be accessed. Extra cycles are shown here simply for clarification.

Functional Description

The IDT70908 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address input registers and data output registers for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70908's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70908 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The 70908 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 16-bit or wider applications.

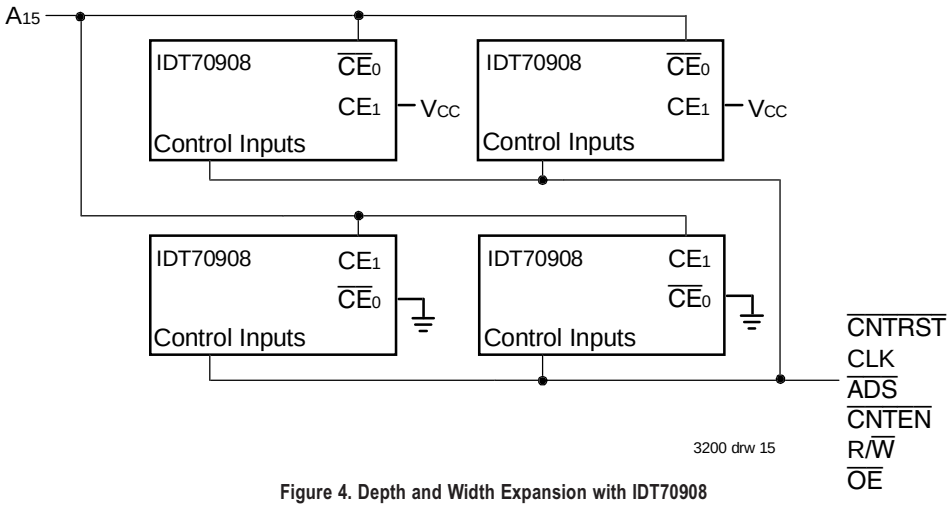
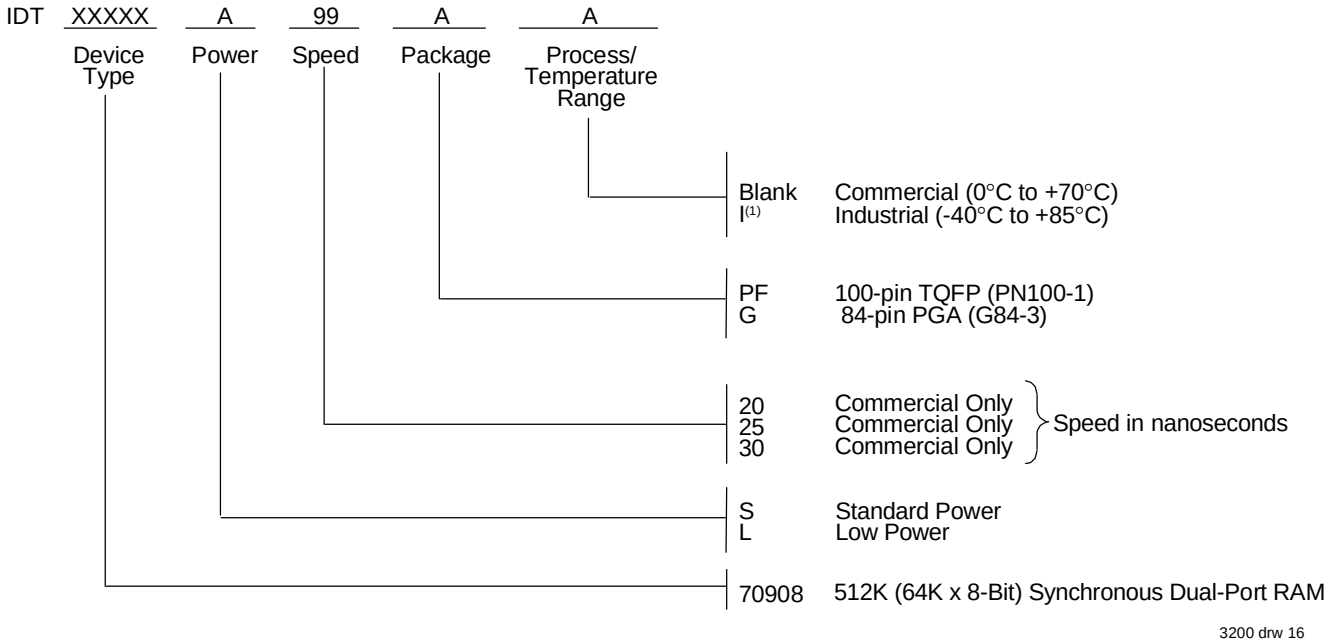


Figure 4. Depth and Width Expansion with IDT70908

Ordering Information



3200 drw 16

NOTE:
1. Industrial temperature range is available.
   For specific speeds, packages and powers contact your sales office.

Preliminary Datasheet:

"PRELIMINARY' datasheets contain descriptions for products that are in early release.

Datasheet Document History:

1/12/99:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Added additional notes to pin configurations
	Page 13 Added Depth and Width Expansion note
6/7/99 :	Changed drawing format
	Page 4 Deleted note 5 for Table II

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
831-754-4613
DualPortHelp@idt.com

The IDT logo is a registered trademark of Integrated Device Technology, Inc.