



Features

- 32K x 36 or 64K x 18 Organizations
- 0.5 Micron CMOS Technology
- Synchronous Pipeline Mode Of Operation with Self-Timed Late Write
- Single Differential PECL Clock compatible with LVTTL Levels
- Single +3.3V Power Supply and Ground
- Common I/O & LVTTL I/O Compatible
- Registered Addresses, Write Enables, Synchronous Select and Data Ins
- Registered Outputs
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 X 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order

Description

The IBM043611RLA and IBM041811RLA 1Mb SRAMs are Synchronous Pipeline Mode, high performance CMOS Static Random Access Memories that are versatile, wide I/O, and achieve 5nanosecond cycle times. Dual differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K Clock, all Addresses, Write-Enables, Sync Select and Data Ins are registered internally. Data Outs are updated from output registers off the next rising edge of the K Clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a single +3.3V power supply and is compatible with LVTTL I/O interfaces.

X36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA8	SA7	NC	SA4	SA3	V _{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA9	SA6	V _{DD}	SA5	SA2	NC
D	DQ23	DQ18	V _{SS}	NC	V _{SS}	DQ17	DQ12
E	DQ19	DQ24	V _{SS}	$\overline{SS}$	V _{SS}	DQ11	DQ16
F	V _{DDQ}	DQ20	V _{SS}	$\overline{G}$	V _{SS}	DQ15	V _{DDQ}
G	DQ21	DQ25	$\overline{SBWc}$	NC	$\overline{SBWb}$	DQ10	DQ14
H	DQ26	DQ22	V _{SS}	NC	V _{SS}	DQ13	DQ9
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	DQ27	DQ31	V _{SS}	K	V _{SS}	DQ4	DQ8
L	DQ32	DQ28	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQ7	DQ3
M	V _{DDQ}	DQ33	V _{SS}	$\overline{SW}$	V _{SS}	DQ2	V _{DDQ}
N	DQ34	DQ29	V _{SS}	SA1	V _{SS}	DQ6	DQ1
P	DQ30	DQ35	V _{SS}	SA0	V _{SS}	DQ0	DQ5
R	NC	SA14	M1*	V _{DD}	M2*	SA10	NC
T	NC	NC	SA13	SA12	SA11	NC	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{SS} and V_{DD}, respectively.

X18 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA8	SA7	NC	SA4	SA3	V _{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA9	SA6	V _{DD}	SA5	SA2	NC
D	DQ9	NC	V _{SS}	NC	V _{SS}	DQ8	NC
E	NC	DQ10	V _{SS}	$\overline{SS}$	V _{SS}	NC	DQ7
F	V _{DDQ}	NC	V _{SS}	$\overline{G}$	V _{SS}	DQ6	V _{DDQ}
G	NC	DQ11	$\overline{SBWb}$	NC	NC	NC	DQ5
H	DQ12	NC	V _{SS}	NC	V _{SS}	DQ4	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQ13	V _{SS}	K	V _{SS}	NC	DQ3
L	DQ14	NC	NC	$\overline{K}$	$\overline{SBWa}$	DQ2	NC
M	V _{DDQ}	DQ15	V _{SS}	$\overline{SW}$	V _{SS}	NC	V _{DDQ}
N	DQ16	NC	V _{SS}	SA1	V _{SS}	DQ1	NC
P	NC	DQ17	V _{SS}	SA0	V _{SS}	NC	DQ0
R	NC	SA15	M1	V _{DD}	M2	SA11	NC
T	NC	SA13	SA14	NC	SA12	SA10	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{SS} and V_{DD}, respectively.



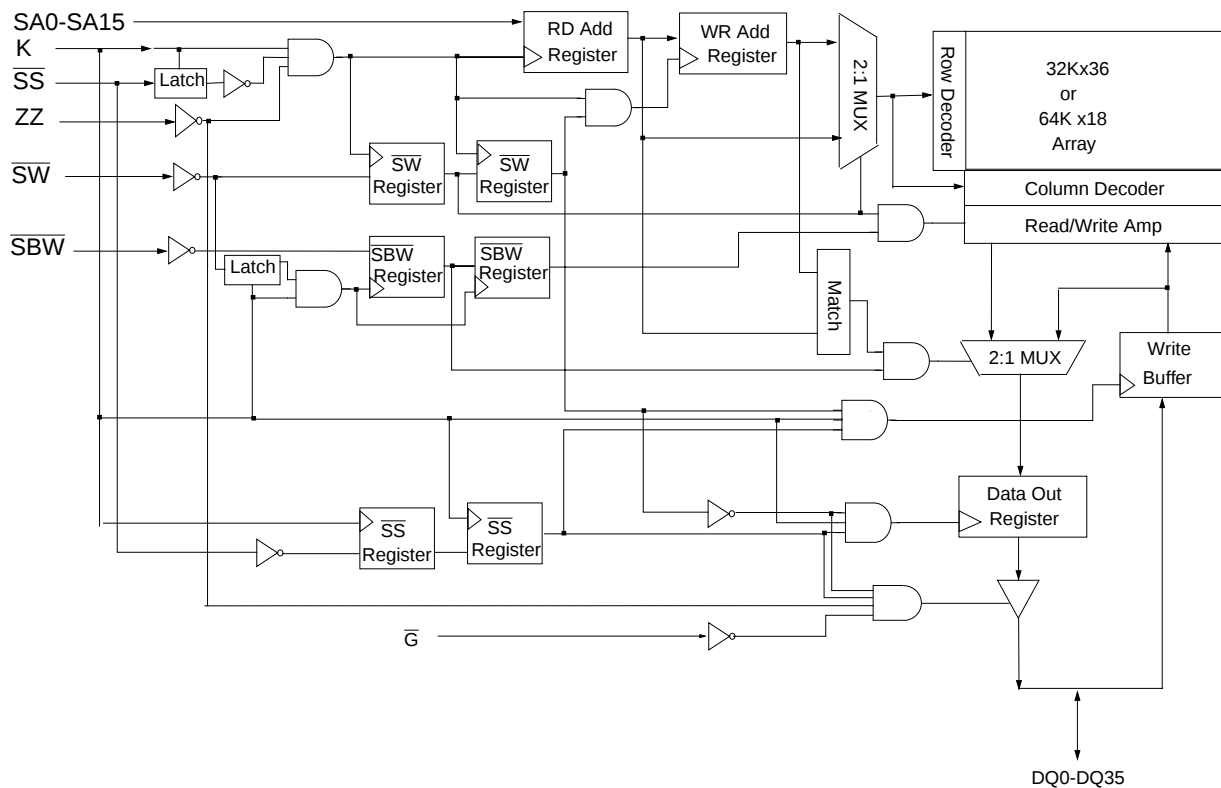
Preliminary

IBM043611RLAB
IBM041811RLAB
32K X 36 & 64K X 18 SRAM

Pin Description

SA0-SA15	Address Input	TDO	IEEE 1149 Test Output
DQa,DQb,DQc,DQd	Data I/O (DQ0-8,DQ9-17,DQ18-26,DQ27-35)	$\overline{SS}$	Synchronous Select
K, $\overline{K}$	Differential PECL CLocks (LVTTTL Compatible)	M1, M2	Clock Mode Inputs
$\overline{SW}$	Write Enable, global	V_{DD}	Power Supply (+3.3V)
$\overline{SBWa}$	Write Enable, Byte a (DQ0 to DQ8)	V_{SS}	Ground
$\overline{SBWb}$	Write Enable, Byte b (DQ9 to DQ17)	V_{DDQ}	Output Power Supply
$\overline{SBWc}$	Write Enable, Byte c (DQ18 to DQ26)	$\overline{G}$	Asynchronous Output Enable
$\overline{SBWd}$	Write Enable, Byte d (DQ27 to DQ35)	ZZ	Asynchronous Sleep Mode
TMS,TDI,TCK	IEEE 1149 Test Inputs	NC	No Connect

Block Diagram



SRAM FEATURES

Late Write

Late Write function allows for write data to be registered one cycle after addresses and controls. This feature eliminates one bus-turnaround cycle necessary when going from a Read to a Write operation. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. In the case a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with the address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array data occurs on a byte by byte basis. When one byte is written during a write cycle, read data from the last written address will have new byte data from the write buffer and remaining bytes from the SRAM array.

Mode Control

Mode control pins: M1 and M2 are used to select four different JEDEC standard read protocols. This SRAM only supports the single clock pipeline (M1 = V_{SS} , M2 = V_{DD}) protocol. Mode control inputs must be set with power up and must not change during SRAM operation.

Sleep Mode

Sleep mode is accomplished by switching asynchronous signal ZZ high. When the SRAM is in Sleep Mode, the outputs will go to a High-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes normal operation.

Power-Up/ Power-Down Sequencing

The Power supplies need to be powered up in the following manner: V_{DD} , V_{DDQ} and Inputs. The power down sequencing must be the reverse. V_{DDQ} must never be allowed to exceed V_{DD} .

Ordering Information

Part Number	Organization	Speed	Leads
IBM041811RLAB - 5	64K x 18	2.5ns Access / 5 ns Cycle	7 X 17 BGA
IBM041811RLAB - 6	64K x 18	3.0ns Access / 6ns Cycle	7 X 17 BGA
IBM041811RLAB - 7	64K x 18	3.5ns Access / 7ns Cycle	7 X 17 BGA
IBM043611RLAB - 5	32K x 36	2.5ns Access / 5 ns Cycle	7 X 17 BGA
IBM043611RLAB - 6	32K x 36	3.0ns Access / 6ns Cycle	7 X 17 BGA
IBM043611RLAB - 7	32K x 36	3.5ns Access / 7ns Cycle	7 X 17 BGA



Clock Truth Table

K	ZZ	SS	SW	SBW $\bar{a}$	SBW $\bar{b}$	SBW $\bar{c}$	SBW $\bar{d}$	DQ (n)	DQ (n+1)	MODE	Notes
L→H	L	L	H	X	X	X	X	X	D _{OUT} 0-35	Read Cycle All Bytes	2
L→H	L	L	L	L	H	H	H	X	D _{IN} 0-8	Write Cycle 1st Byte	
L→H	L	L	L	H	L	H	H	X	D _{IN} 9-17	Write Cycle 2nd Byte	
L→H	L	L	L	H	H	L	H	X	D _{IN} 18-26	Write Cycle 3rd Byte	1
L→H	L	L	L	H	H	H	L	X	D _{IN} 27-35	Write Cycle 4th Byte	1
L→H	L	L	L	L	L	L	L	X	D _{IN} 0-35	Write Cycle All Bytes	2
L→H	L	L	L	H	H	H	H	X	High-Z	Abort Write Cycle	
L→H	L	H	X	X	X	X	X	X	High-Z	Deselect Cycle	
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode	

1. x36 only.
2. for x18 organization use D_{OUT}/D_{IN} 0-17 only.

Output Enable Truth Table

Operation	$\bar{G}$	DQ
Read	L	D _{OUT} 0-35
Read	H	High-Z
Sleep (ZZ=H)	X	High-Z
Write ($\bar{S}W=L$)	X	High-Z
Deselect ($\bar{S}S=H$)	X	High-Z

Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V _{DD}	-0.5 to 4.6	V	1
Output Power Supply Voltage	V _{DDQ}	-0.5 to 4.6	V	1
Input Voltage	V _{IN}	-0.5 to V _{DD} +0.5	V	1
Output Voltage	V _{OUT}	-0.5 to V _{DD} +0.5	V	1
Operating Temperature	T _A	0 to +70	°C	1
Junction Temperature	T _J	110	°C	1
Storage Temperature	T _{STG}	-55 to +125	°C	1
Short Circuit Output Current	I _{OUT}	25	mA	1
Latchup Current	I _{LI}	>200	mA	

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions ($T_A=0$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.15	3.3	3.60	V	1
Output Driver Supply Voltage	V_{DDQ}	3.15	3.3	3.60	V	1
Input High Voltage	V_{IH}	2.2	—	$V_{DD}+0.3$	V	1, 2
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3
PECL Clock Input High Voltage	$V_{IH} - PECL$	2.135	—	2.420	V	1, 2
PECL Clock Input Low Voltage	$V_{IL} - PECL$	1.490	—	1.825	V	1, 3
Output Current	I_{OUT}	—	5	8	mA	

1. All voltages referenced to V_{SS} . All V_{DD} , V_{DDQ} and V_{SS} pins must be connected.
 2. $V_{IH}(\text{Max})DC = V_{DD} + 0.3\text{ V}$, $V_{IH}(\text{Max})AC = V_{DD} + 1.5\text{ V}$ (pulse width $\leq 4.0\text{ns}$).
 3. $V_{IL}(\text{Min})DC = -0.3\text{ V}$, $V_{IL}(\text{Min})AC = -1.5\text{ V}$ (pulse width $\leq 4.0\text{ns}$).

Capacitance ($T_A=0$ to $+70^\circ\text{C}$, $V_{DD}=3.3 -5\% + 10\% \text{ V}$, $f=1\text{MHz}$)

Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	C_{IN}	$V_{IN} = 0\text{V}$	5	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	$V_{OUT} = 0\text{V}$	5	pF

DC Electrical Characteristics ($T_A=0$ to $+70^\circ\text{C}$, $V_{DD}=3.3 -5\% + 10\% \text{ V}$)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current - X36 ($I_{OUT} = 0$, $V_{IN} = V_{IH}$ or V_{IL} , ZZ & $SS = V_{IL}$)	I_{DD5} I_{DD6} I_{DD7}	— — —	630 540 470	mA	1
Average Power Supply Operating Current - X18 ($I_{OUT} = 0$, $V_{IN} = V_{IH}$ or V_{IL} , ZZ & $SS = V_{IL}$)	I_{DD5} I_{DD6} I_{DD7}	— — —	590 500 440	mA	1
Power Supply Standby Current ($SS = V_{IH}$, or $ZZ = V_{IH}$ All other inputs = V_{IH} or V_{IL} , $I_{OUT} = 0$)	I_{SB}	—	25	mA	1
Input Leakage Current, any input ($V_{IN} = V_{SS}$ or V_{DD})	I_{LI}	-1	+1	μA	
Output Leakage Current ($V_{OUT} = V_{SS}$ or V_{DD} , DQ in High-Z)	I_{LO}	-1	+1	μA	
Output High "H" Level Voltage ($I_{OH}=-8\text{mA}$ @ 2.4V)	V_{OH}	2.4	—	V	
Output Low "L" Level Voltage ($I_{OL}=+8\text{mA}$ @ 0.4V)	V_{OL}	—	0.4	V	

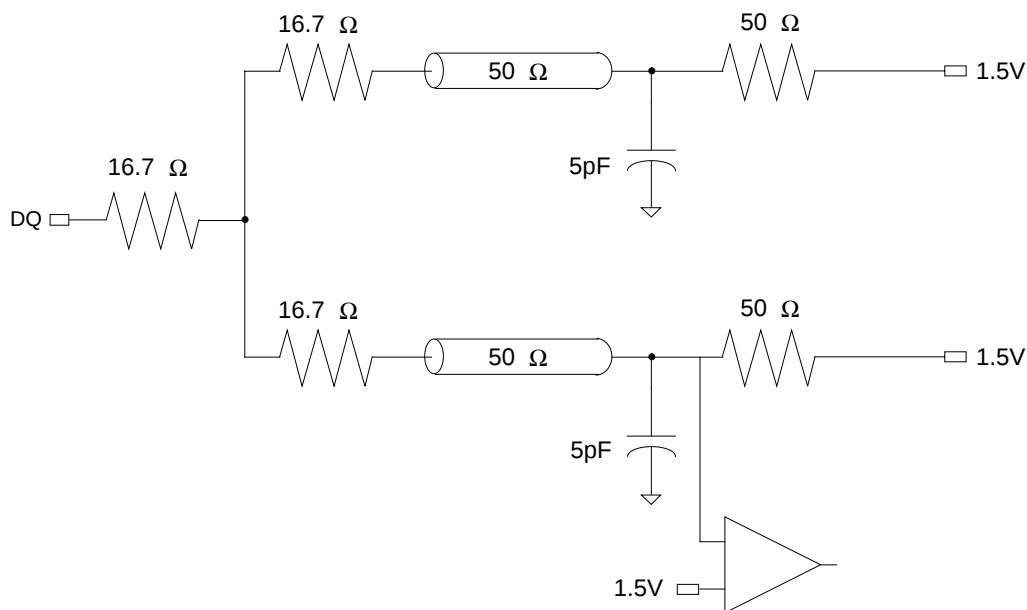
1. I_{OUT} = Chip Output Current.

AC Test Conditions ($T_A=0$ to $+70^{\circ}\text{C}$, $V_{DD}, V_{DDQ}=3.3$ -5% + 10% V)

Parameter	Symbol	Conditions	Units	Notes
Input High Level	V_{IH}	3.0	V	
Input Low Level	V_{IL}	0.0	V	
PECL Clock Input High Voltage	$V_{IH(PECL)}$	2.4	V	
PECL Clock Input Low Voltage	$V_{IL(PECL)}$	1.5	V	
Input Rise Time	T_R	1.0	ns	
Input Fall Time	T_F	1.0	ns	
PECL Clock Input Rise Time	$T_{R(PECL)}$	0.5	ns	
PECL Clock Input Fall Time	$T_{F(PECL)}$	0.5	ns	
Input and Output Timing Reference Level (except K, $\bar{K}$)		1.5	V	
PECL Clock Reference Level		K and $\bar{K}$ Cross Point	V	
Output Load Conditions				1

1. See AC Test Loading on page 7.

AC Test Loading



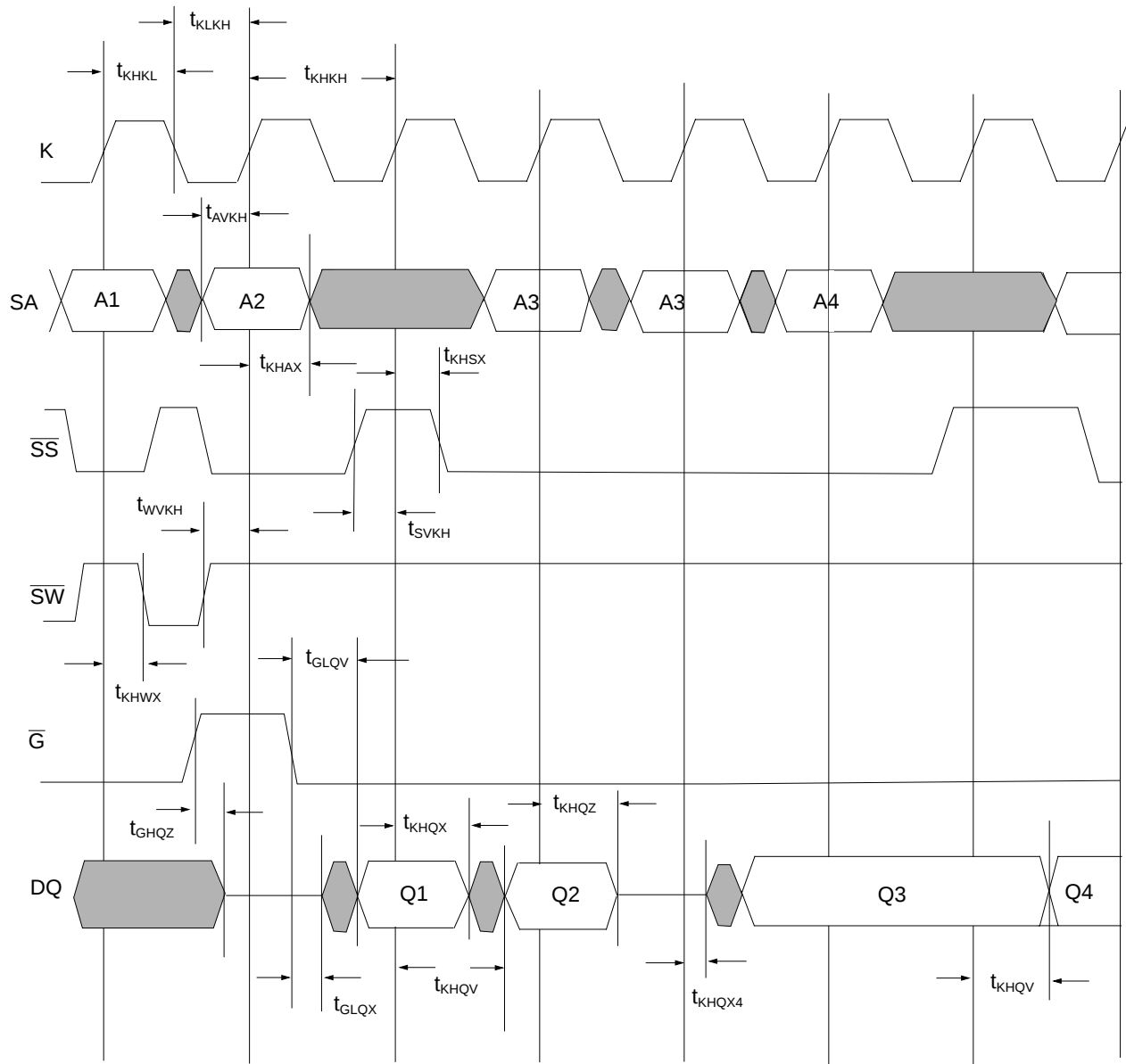
AC Characteristics ($T_A=0$ to $+70^\circ\text{C}$, V_{DD} , $V_{DDQ}=3.3$ -5% + 10% V)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{KHKH}	5.0	—	6.0	—	7.0	—	ns	
Clock High Pulse Width	t_{KHKL}	1.5	—	1.5	—	1.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	1.5	—	1.5	—	1.5	—	ns	
Clock to Output Valid	t_{KHQV}	—	2.5	—	3.0	—	3.5	ns	1
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	0.5	—	ns	
Address Hold Time	t_{KHAX}	1.0	—	1.0	—	1.0	—	ns	
Sync Select Setup Time	t_{SVKH}	0.5	—	0.5	—	0.5	—	ns	
Sync Select Hold Time	t_{KHSX}	1.0	—	1.0	—	1.0	—	ns	
Write Enables Setup Time	t_{WVKH}	0.5	—	0.5	—	0.5	—	ns	
Write Enables Hold Time	t_{KHWX}	1.0	—	1.0	—	1.0	—	ns	
Data In Setup Time	t_{DVKH}	0.5	—	0.5	—	0.5	—	ns	
Data In Hold Time	t_{KHDX}	1.0	—	1.0	—	1.0	—	ns	
Data Out Hold Time	t_{KHQX}	0.5	—	0.5	—	0.5	—	ns	1
Clock High to Output High-Z	t_{KHQZ}	—	2.5	—	3.0	—	3.5	ns	1
Clock High to Output Active	t_{KHQX4}	1.0	—	1.0	—	1.0	—	ns	1, 2
Output Enable to High-Z	t_{GHQZ}	—	2.5	—	3.0	—	3.5	ns	1
Output Enable to Low-Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	ns	1
Output Enable to Output Valid	t_{GLQV}	—	2.5	—	3.0	—	3.5	ns	1
Sleep Mode Recovery Time	t_{ZZR}	5	—	6	—	7	—	ns	
Sleep Mode Enable Time	t_{ZZE}	—	5	—	6	—	7	ns	

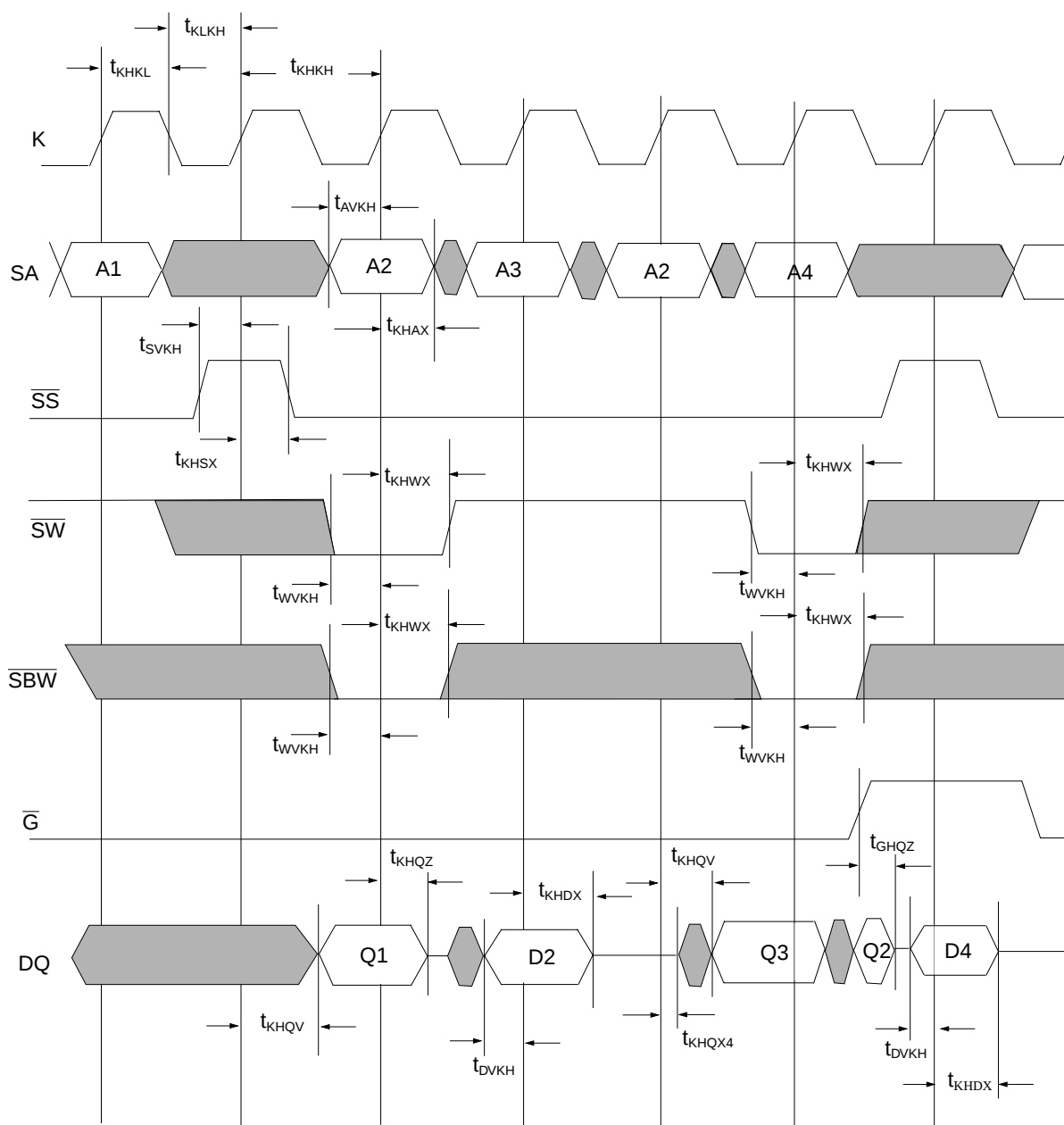
1. See AC Test Loading on page 7.

2. Tested without guardbands. 08ns if guardbands are applied.

Timing Diagram (Read and Deselect Cycles)



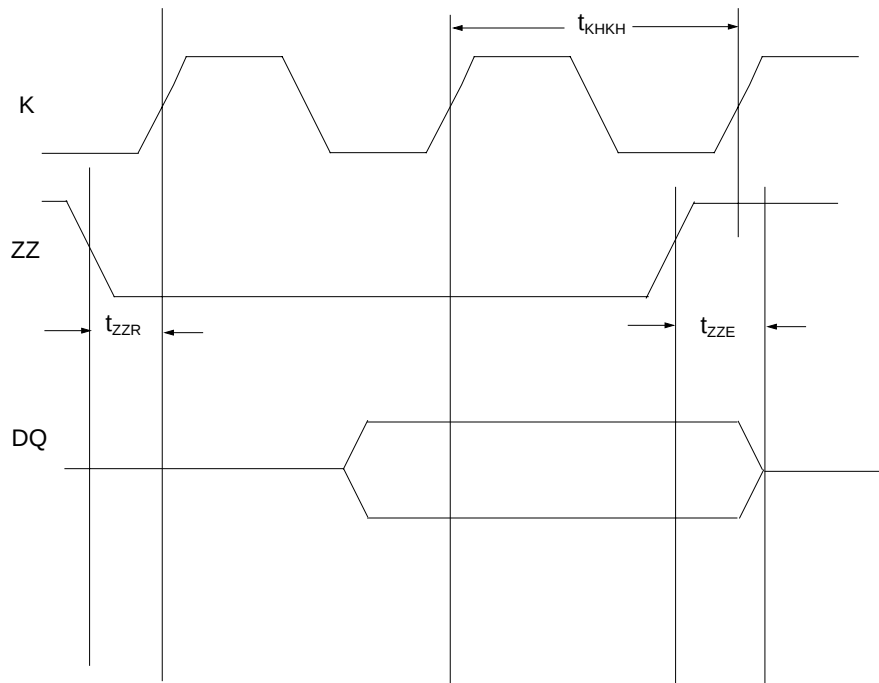
Timing Diagram (Read Write Cycles)



NOTES:

1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

Timing Diagram (Sleep Mode)



IEEE 1149.1 TAP AND BOUNDARY SCAN

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAM contains a TAP controller, Instruction register, Boundary Scan register, Bypass register and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

Caution: TCK, TMS, TDI inputs must be biased to a valid logic level, even if JTAG is not used.

JTAG Recommended DC Operating Conditions ($T_A=0$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.2	—	$V_{DD}+0.3$	V	1
JTAG Input Low Voltage	V_{IL1}	-0.3	—	0.8	V	1
JTAG Output High Level	V_{OH1}	2.4	—	—	V	1, 2
JTAG Output Low Level	V_{OL1}	—	—	0.4	V	1, 3
1. All JTAG Inputs/Outputs are LVTTTL Compatible only. 2. $I_{OH1} = -8\text{mA}$ at 2.4V. 3. $I_{OL1} = +8\text{mA}$ at 0.4V.						

JTAG AC Test Conditions ($T_A=0$ to $+70^{\circ}\text{C}$, $V_{DD}=3.3 -5\% + 10\% \text{ V}$)

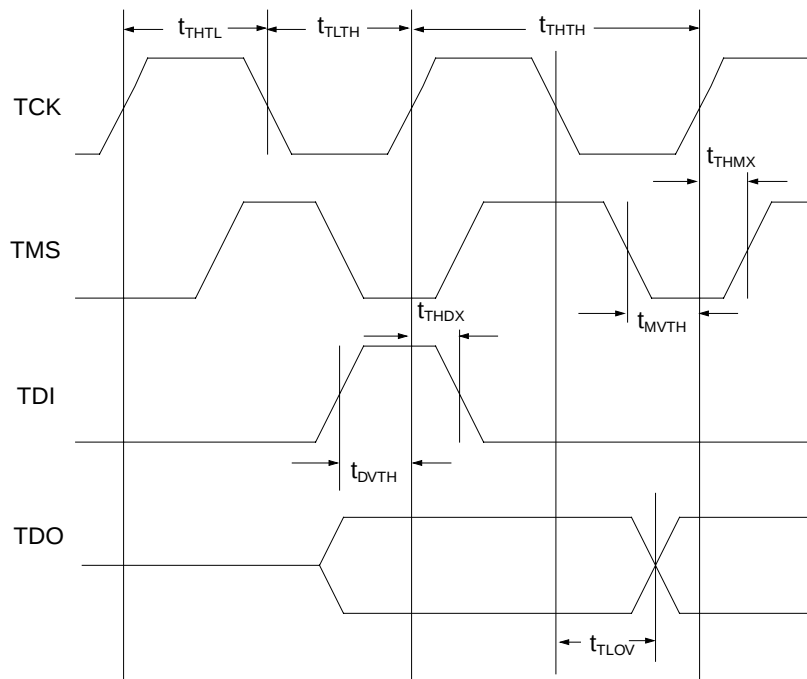
Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V_{IH1}	3.0	V	
Input Pulse Low Level	V_{IL1}	0.0	V	
Input Rise Time	T_{R1}	2.0	ns	
Input Fall Time	T_{F1}	2.0	ns	
Input and Output Timing Reference Level		1.5	V	1
1. See AC Test Loading on page 7.				

JTAG AC Characteristics ($T_A=0$ to $+70^\circ\text{C}$, $V_{DD}=3.3$ -5% + 10% V)

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	t_{THTH}	20	—	ns	
TCK High Pulse Width	t_{HTL}	7	—	ns	
TCK Low Pulse Width	t_{LTH}	7	—	ns	
TMS Setup	t_{MVTH}	4	—	ns	
TMS Hold	t_{THMX}	4	—	ns	
TDI Setup	t_{DVTH}	4	—	ns	
TDI Hold	t_{THDX}	4	—	ns	
TCK Low to Valid Data	t_{TLOV}	—	7	ns	1

1. See AC Test Loading on page 7.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size X18	Bit Size X36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

* The Boundary Scan chain consists of the following bits:

- 36 or 18 bits for Data Inputs Depending on X18 or X36 Configuration
- 15 bits for SA0 - SA14 for X36, 16 bits for SA0 - SA15 for X18
- 4 bits for SBW_a - SBW_d in X36, 2 bits for SBW_a and SBW_b in X18
- 8 bits for K, $\bar{K}$, SS, $\bar{G}$, SW, ZZ, M1 and M2
- 7 bits for Place Holders

* K and $\bar{K}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit(0)
64K X18	0000	001 000 0011	000001	000 101 001 00	1
32K X36	0000	000 110 0100	000001	000 101 001 00	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	2
010	SAMPLE-Z	1
011	BYPASS	3
100	SAMPLE	4
101	PRIVATE	3, 5
110	BYPASS	3
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initialized to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. This instruction is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

List of IEEE 1149.1 standard violations:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d



Preliminary

IBM043611RLAB
IBM041811RLAB
32K X 36 & 64K X 18 SRAM

Boundary Scan Order (X36)

(PH =Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQ15	6F	49	DQ22	2H
2	SA0	4P	26	DQ16	7E	50	DQ26	1H
3	SA12	4T	27	DQ11	6E	51	$\overline{\text{SBWc}}$	3G
4	SA10	6R	28	DQ12	7D	52	PH**	4D
5	SA11	5T	29	DQ17	6D	53	$\overline{\text{SS}}$	4E
6	ZZ	7T	30	SA3	6A	54	PH*	4G
7	DQ0	6P	31	SA2	6C	55	PH**	4H
8	DQ5	7P	32	SA5	5C	56	$\overline{\text{SW}}$	4M
9	DQ6	6N	33	SA4	5A	57	$\overline{\text{SBWd}}$	3L
10	DQ1	7N	34	PH*	6B	58	DQ27	1K
11	DQ2	6M	35	PH*	5B	59	DQ31	2K
12	DQ7	6L	36	PH*	3B	60	DQ32	1L
13	DQ3	7L	37	PH*	2B	61	DQ28	2L
14	DQ4	6K	38	SA7	3A	62	DQ33	2M
15	DQ8	7K	39	SA6	3C	63	DQ34	1N
16	$\overline{\text{SBWa}}$	5L	40	SA9	2C	64	DQ29	2N
17	$\overline{\text{K}}$	4L	41	SA8	2A	65	DQ30	1P
18	K	4K	42	DQ18	2D	66	DQ35	2P
19	$\overline{\text{G}}$	4F	43	DQ23	1D	67	SA13	3T
20	$\overline{\text{SBWb}}$	5G	44	DQ24	2E	68	SA14	2R
21	DQ9	7H	45	DQ19	1E	69	SA1	4N
22	DQ13	6H	46	DQ20	2F	70	M1	3R
23	DQ14	7G	47	DQ25	2G			
24	DQ10	6G	48	DQ21	1G			

1. * Input of PH register connected to V_{SS} .

2. ** Input of PH register connected to V_{DD} .

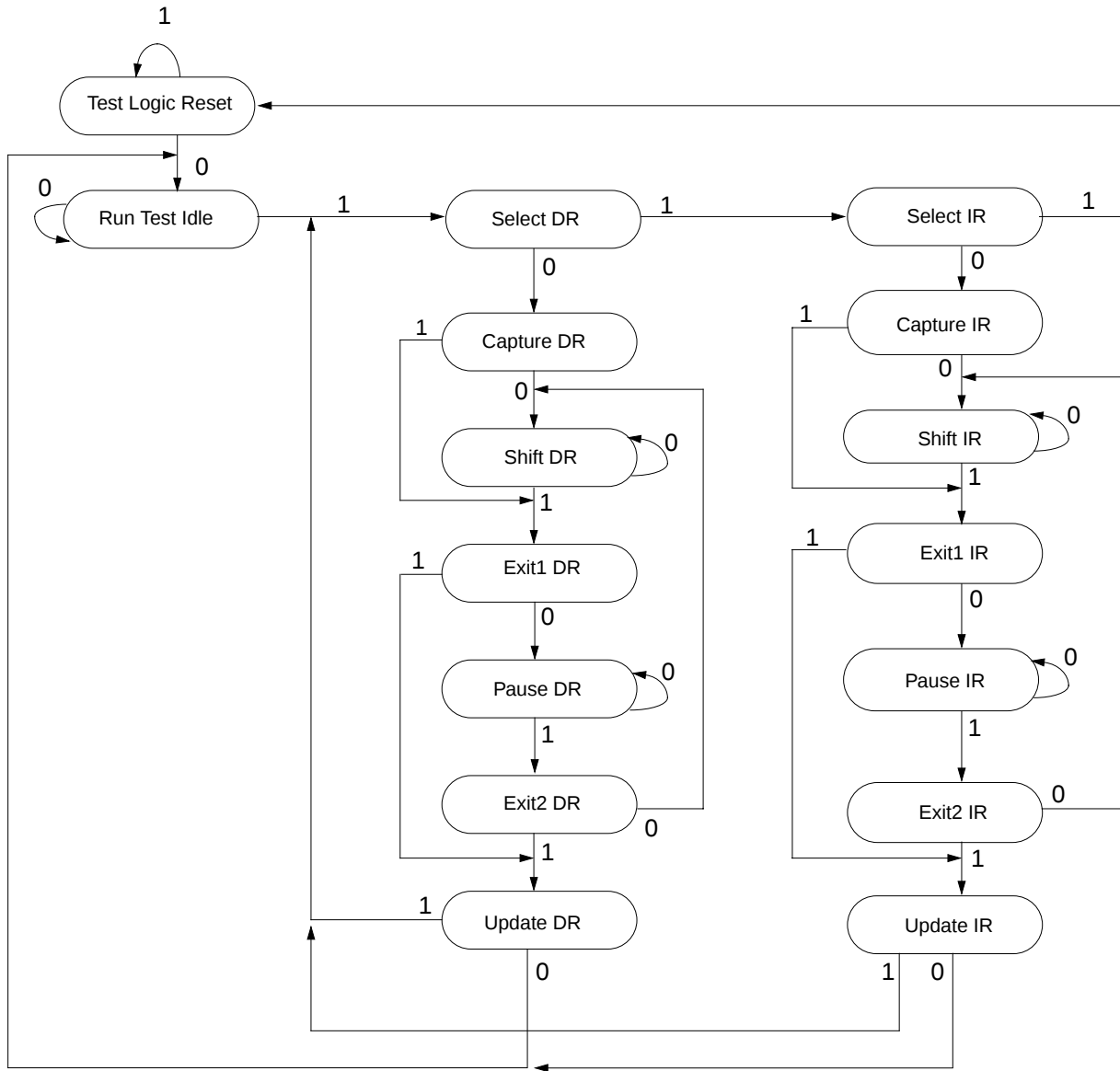
Boundary Scan Order (x18)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	27	PH*	2B
2	SA10	6T	28	SA7	3A
3	SA0	4P	29	SA6	3C
4	SA11	6R	30	SA9	2C
5	SA12	5T	31	SA8	2A
6	ZZ	7T	32	DQ9	1D
7	DQ0	7P	33	DQ10	2E
8	DQ1	6N	34	DQ11	2G
9	DQ2	6L	35	DQ12	1H
10	DQ3	7K	36	$\overline{\text{SBWb}}$	3G
11	$\overline{\text{SBWa}}$	5L	37	PH**	4D
12	$\overline{\text{K}}$	4L	38	$\overline{\text{SS}}$	4E
13	K	4K	39	PH*	4G
14	$\overline{\text{G}}$	4F	40	PH**	4H
15	DQ4	6H	41	$\overline{\text{SW}}$	4M
16	DQ5	7G	42	DQ13	2K
17	DQ6	6F	43	DQ14	1L
18	DQ7	7E	44	DQ15	2M
19	DQ8	6D	45	DQ16	1N
20	SA3	6A	46	DQ17	2P
21	SA2	6C	47	SA14	3T
22	SA5	5C	48	SA15	2R
23	SA4	5A	49	SA1	4N
24	PH*	6B	50	SA13	2T
25	PH*	5B	51	M1	3R
26	PH*	3B			

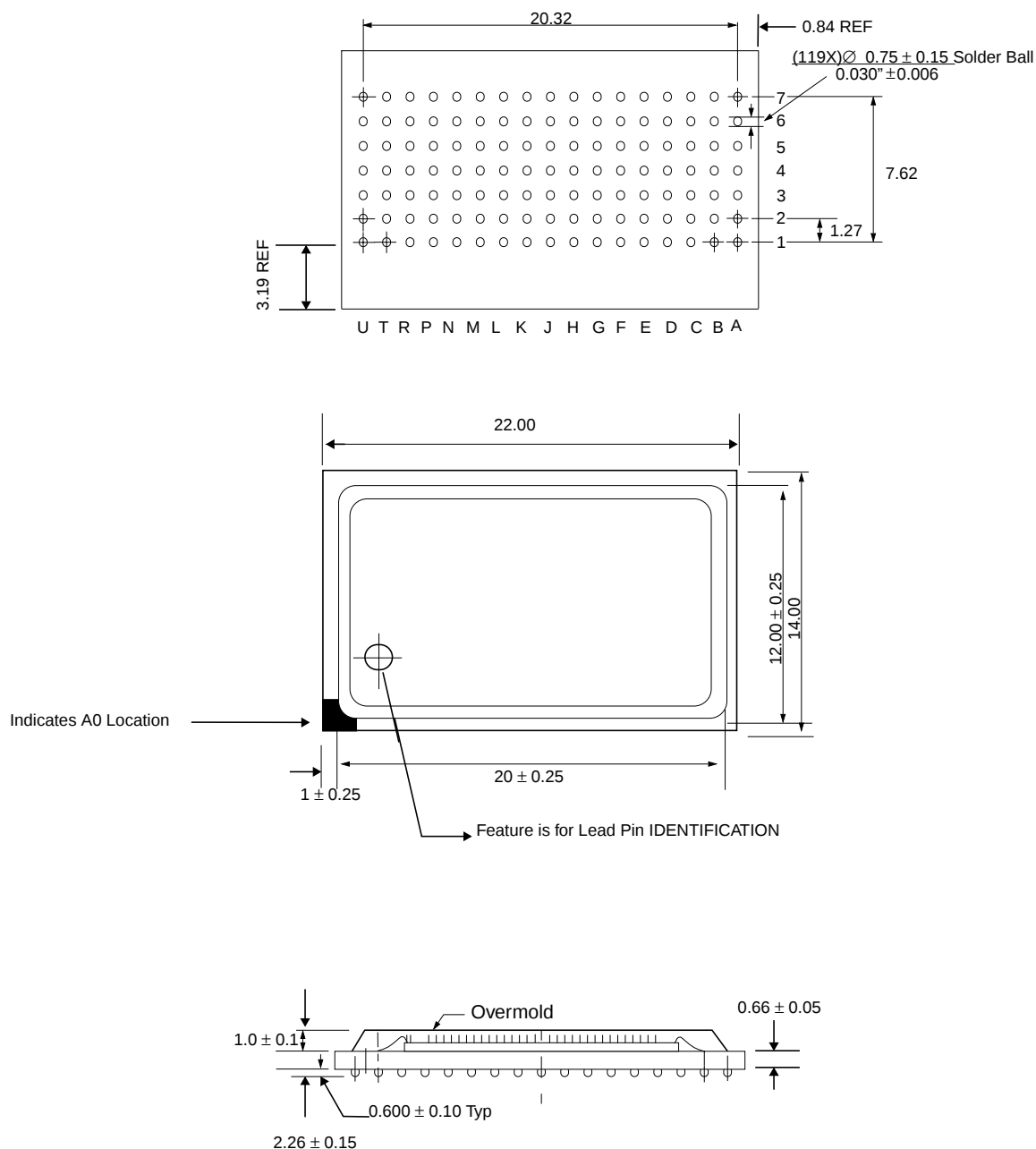
1. * Input of PH register connected to V_{SS} .

2. ** Input of PH register connected to V_{DD} .

TAP Controller State Machine



7 x 17 BGA Dimensions



Note: All dimensions in Millimeters



Preliminary

IBM043611RLAB
IBM041811RLAB
32K X 36 & 64K X 18 SRAM

Revision Log

Rev	Contents of Modification
6/94	Initial Release of the 32K x 36 & 64K x 18 (5/6/7) BGA FLOW THRU Application Spec.
1/95	Addition of SRAM Features section. Changed parameter/signal names for JEDEC compatibility.
2/95	Add package dimensions and identify SA and DQ pins.
4/95	Add Technology Product Names — page 1.
5/95	Fax Server Release.
7/95	WWW release.
8/95	Update power numbers.
4/96	Parameter updates.
6/96	Document reviewed by all groups. Add EC #.



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