Preliminary

32K X 36 & 64K X 18 SRAM

Features

- 32K x 36 or 64K x 18 Organizations
- 0.5 Micron CMOS Technology
- Synchronous Flow-Thru Mode Of Operation with Self-Timed Late Write
- Dual Differential Input and Output Clocks
- Single +3.3V Power Supply and Ground
- GTL/HSTL Input and Output levels
- Registered Addresses, Write Enables, Sync Select and Data Ins.
- Common I/O
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 X 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order
- Programmable Impedance Output Drivers

Description

The IBM043610QLA and IBM04180QLA 1Mb SRAMs are Synchronous Flow-Thru Mode, high performance CMOS Static Random Access Memories that are versatile, wide I/O, and achieve 5 nanosecond cycle times. Dual differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K Clock, all Addresses, Write-Enables, Sync Select and Data Ins are registered internally. Differential clocks C and $\overline{C}$ are used to control the Output Data Hold Time by allowing output data to change after the rising edge of the C clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a single +3.3V power supply and is compatible with GTL/HSTL I/O interfaces.

X36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA8	SA7	NC	SA4	SA3	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA9	SA6	V_{DD}	SA5	SA2	NC
D	DQ23	DQ18	V_{SS}	ZQ	V_{SS}	DQ17	DQ12
E	DQ19	DQ24	V_{SS}	$\overline{SS}$	V_{SS}	DQ11	DQ16
F	V_{DDQ}	DQ20	V_{SS}	$\overline{G}$	V_{SS}	DQ15	V_{DDQ}
G	DQ21	DQ25	$\overline{SBWc}$	$\overline{C}$	$\overline{SBWb}$	DQ10	DQ14
H	DQ26	DQ22	V_{SS}	C	V_{SS}	DQ13	DQ9
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQ27	DQ31	V_{SS}	K	V_{SS}	DQ4	DQ8
L	DQ32	DQ28	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQ7	DQ3
M	V_{DDQ}	DQ33	V_{SS}	$\overline{SW}$	V_{SS}	DQ2	V_{DDQ}
N	DQ34	DQ29	V_{SS}	SA1	V_{SS}	DQ6	DQ1
P	DQ30	DQ35	V_{SS}	SA0	V_{SS}	DQ0	DQ5
R	NC	SA14	M1*	V_{DD}	M2*	SA10	NC
T	NC	NC	SA13	SA12	SA11	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{DD}.

X18 BGA Bump Layout (Top View)

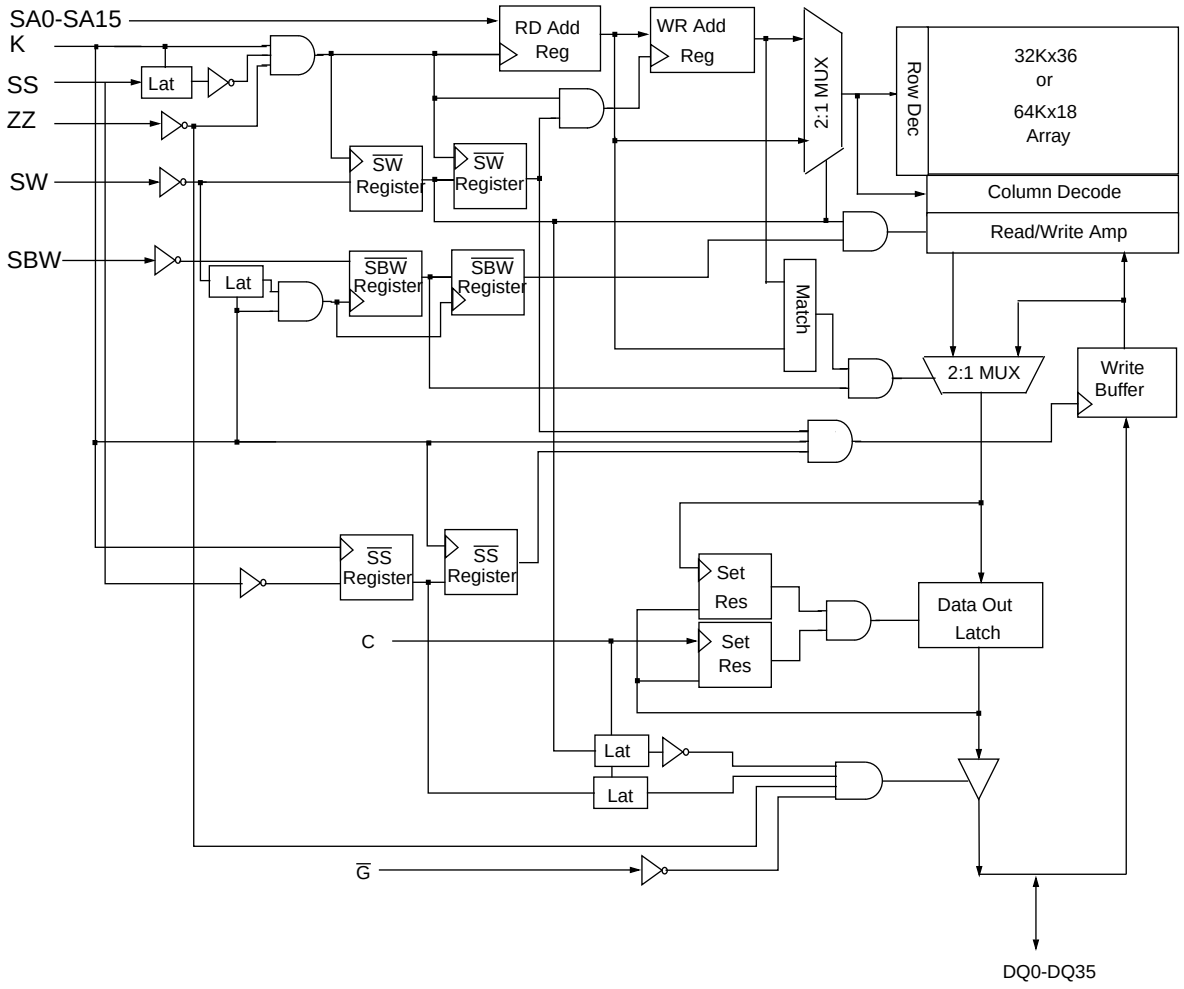
	1	2	3	4	5	6	7
A	V_{DDQ}	SA8	SA7	NC	SA4	SA3	VDDQ
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA9	SA6	V_{DD}	SA5	SA2	NC
D	DQ9	NC	V_{SS}	ZQ	V_{SS}	DQ8	NC
E	NC	DQ10	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQ7
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ6	V_{DDQ}
G	NC	DQ11	$\overline{SBWb}$	$\overline{C}$	NC	NC	DQ5
H	DQ12	NC	V_{SS}	C	V_{SS}	DQ4	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQ13	V_{SS}	K	V_{SS}	NC	DQ3
L	DQ14	NC	NC	$\overline{K}$	$\overline{SBWa}$	DQ2	NC
M	V_{DDQ}	DQ15	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQ16	NC	V_{SS}	SA1	V_{SS}	DQ1	NC
P	NC	DQ17	V_{SS}	SA0	V_{SS}	NC	DQ0
R	NC	SA15	M1	V_{DD}	M2	SA11	NC
T	NC	SA13	SA14	NC	SA12	SA10	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{DD} .

Pin Description

SA0-SA15	Address Input	$\overline{G}$	Asynchronous Output Enable
DQ0-DQ35	Data I/O	$\overline{SS}$	Synchronous Select
K, $\overline{K}$	Differential Input Register Clocks	M1, M2	Clock Mode Inputs - Selects Single or Dual Clock Operation.
C,$\overline{C}$	Differential Output Data Hold Control Clocks	V_{REF}(2)	GTL/HSTL Input Reference Voltage
$\overline{SW}$	Write Enable, Global	V_{DD}	Power Supply (+3.3V)
$\overline{SBWa}$	Write Enable, Byte a (DQ0-DQ8)	V_{SS}	Ground
$\overline{SBWb}$	Write Enable, Byte b (DQ9-DQ17)	V_{DDQ}	Output Power Supply
$\overline{SBWc}$	Write Enable, Byte c (DQ18-DQ26)	ZZ	Asynchronous Sleep Mode
$\overline{SBWd}$	Write Enable, Byte d (DQ27-DQ35)	ZQ	Output Driver Impedance Control
TMS,TDI,TCK	IEEE 1149.1 Test Inputs (LVTTL levels)	NC	No Connect
TDO	IEEE 1149.1 Test Output (LVTTL level)		

Block Diagram



SRAM FEATURES

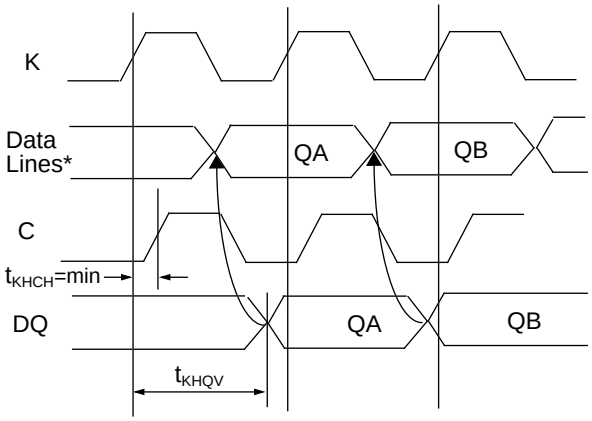
Late Write

Late Write function allows for write data to be registered one cycle after addresses and controls. This feature eliminates one bus-turnaround cycle necessary when going from a Read to a Write operation. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. In the case a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with the address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array data occurs on a byte by byte basis. When one byte is written during a write cycle, read data from the last written address will have new byte data from the write buffer and remaining bytes from the SRAM array.

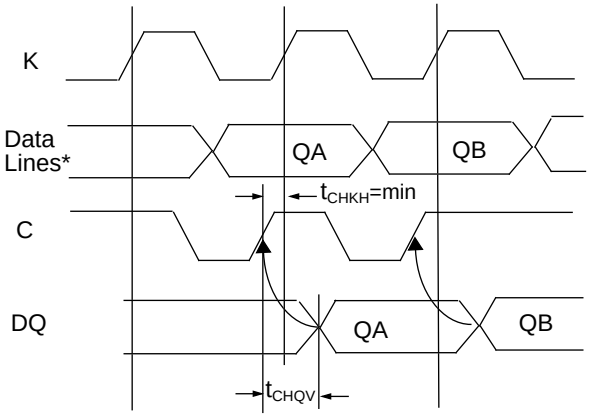
Dual Clock Operation

In Dual Clock Operation, the K Clocks are used to register all synchronous inputs and start the SRAM operation. The C Clocks are used to control the output data timings. During Write ($\overline{SW}$=L) or Deselect ($\overline{SS}$=H) operations, the rising edge of C Clock triggers the time to High-Z. During Read operations the location of the rising edge of the C Clock will determine the output data valid placement by allowing SRAM output data to flow through after the rising edge. When the rising edge of the C Clock occurs early in a Read cycle (e.g. t_{KHCH} = Min.), data from the SRAM will become available at a t_{KHQV} time, as it would in a Flow-Through Read implementation (see Dual Clock Diagram #1 below). As the C Clock rising edge moves away from t_{KHCH} = Min., towards a t_{CHKH} = Min., of the next K Clock rising edge, the output data may become “gated” by the C Clock (see Dual Clock Diagram #2 below). The SRAM access time will then become referenced to the C Clock (i.e. t_{CHQV}). This feature allows SRAM users to fully control the output data hold time over voltage, temperature and process variations, and provide minimum output data latency.

Dual Clock Diagram #1: Output data becomes available as a result of internal data lines flowing through the output latch unrestrained by the C clock.



Dual Clock Diagram #2: Internal data lines await at the output latch for the rising edge of C clock.The C clock enables the output latch and allowsoutput data to become available.



*Data Lines refer to internal data lines connecting to Data Output Latch. See Block Diagram on page 4.

Mode Control

Mode control pins: M1 and M2 are used to select four different JEDEC standard read protocols. This SRAM supports both the Single Clock, Flow-Through (M1 = V_{SS}, M2 = V_{SS}) and Dual Clock Flow-Through protocols (M1 = V_{DD}, M2 = V_{DD}). This data sheet only describes Dual Clock Flow-Through functionality. Mode control inputs must be set with power up and must not change during SRAM operation.

Sleep Mode

Sleep mode is enabled by switching asynchronous signal ZZ High. When the SRAM is in Sleep mode, the outputs will go to a High-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes normal operation.

Programmable Impedance/Power Up Requirements

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow for the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of 25% is between 185Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles and each evaluation may move the output driver impedance level only one step at a time toward the optimum level. The output driver has 16 discrete binary weighted steps. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, therefore, triggering an update. The user may choose to invoke asynchronous $\overline{G}$ updates by providing a $\overline{G}$ setup and hold about the K Clock to guarantee the proper update. There are no power up requirements for the SRAM; however, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 clock cycles followed by a Low-Z to High-Z transition.

Power-Up/ Power-Down Sequencing

The Power supplies need to be powered up in the following manner: V_{DD}, V_{DDQ}, V_{REF} and Inputs. The power down sequencing must be the reverse. V_{DDQ} must never be allowed to exceed V_{DD}.

Ordering Information

Part Number	Organization	Speed	Leads
IBM041810QLAB - 4H	64K x 18	5.9ns Access / 4.5ns Cycle	7 X 17 BGA
IBM041810QLAB - 5F	64K x 18	6.8ns Access / 5ns Cycle	7 X 17 BGA
IBM041810QLAB - 5	64K x 18	7.0ns Access / 5ns Cycle	7 X 17 BGA
IBM041810QLAB - 6	64K x 18	7.5ns Access / 6ns Cycle	7 X 17 BGA
IBM041810QLAB - 7	64K x 18	8.0ns Access / 7ns Cycle	7 X 17 BGA
IBM043610QLAB - 4H	32K x 36	6.4ns Access / 4.5ns Cycle	7 X 17 BGA
IBM043610QLAB - 5F	32K x 36	6.8ns Access / 5ns Cycle	7 X 17 BGA
IBM043610QLAB - 5	32K x 36	7.0ns Access / 5ns Cycle	7 X 17 BGA
IBM043610QLAB - 6	32K x 36	7.5ns Access / 6ns Cycle	7 X 17 BGA
IBM043610QLAB - 7	32K x 36	8.0ns Access / 7ns Cycle	7 X 17 BGA

Clock Truth Table

K, C CLK	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{SBW_A}$	$\overline{SBW_B}$	$\overline{SBW_C}$	$\overline{SBW_D}$	DQ (n)	DQ (n+1)	Mode	Note
L→H	L	L	H	X	X	X	X	D_{OUT} 0-35	X	Read Cycle All Bytes	2
L→H	L	L	L	L	H	H	H	High-Z	D_{IN} 0-8	Write Cycle 1st Byte	
L→H	L	L	L	H	L	H	H	High-Z	D_{IN} 9-17	Write Cycle 2nd Byte	
L→H	L	L	L	H	H	L	H	High-Z	D_{IN} 18-26	Write Cycle 3rd Byte	1
L→H	L	L	L	H	H	H	L	High-Z	D_{IN} 27-35	Write Cycle 4th Byte	1
L→H	L	L	L	L	L	L	L	High-Z	D_{IN} 0-35	Write Cycle All Bytes	2
L→H	L	L	L	H	H	H	H	High-Z	High-Z	Abort Write Cycle	
L→H	L	H	X	X	X	X	X	High-Z	X	Deselect Cycle	
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode	

1. x36 only.
2. for x18 organization use D_{OUT}/D_{IN} 0-17 only.

Output Enable Truth Table

Operation	$\overline{G}$	DQ
Read	L	D_{OUT} 0-35
Read	H	High-Z
Sleep (ZZ=H)	X	High-Z
Write ($\overline{SW}$=L)	X	High-Z
Deselect ($\overline{SS}$=H)	X	High-Z

Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 4.6	V	1
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V	1
Output Voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V	1
Operating Temperature	T_A	0 to +70	°C	1
Junction Temperature	T_J	110	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	25	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.15	3.3	3.60	V	1
Output Driver Supply Voltage	V_{DDQ}	1.14	1.4	1.6	V	1
Input High Voltage	V_{IH}	V_{REF} +0.1	—	V_{DDQ} + 0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	—	V_{REF} -0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.55	0.70	0.90	V	1
Clocks Signal Voltage	$V_{IN - CLK}$	-0.3	—	V_{DDQ} + 0.3	V	1, 4
Differential Clocks Signal Voltage	$V_{DIF - CLK}$	0.1	—	V_{DDQ} + 0.6	V	1, 5
Clocks Common Mode Voltage	$V_{CM - CLK}$	0.55	—	0.90	V	1
Output Current	I_{OUT}	—	5	8	mA	

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DDQ} + 0.3 V, V_{IH}(Max)AC = V_{DD} + 1.5 V (pulse width ≤ 4.0ns).
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns).
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (K, $\overline{K}$, C, $\overline{C}$).
5. $V_{DIF-CLK}$ specifies the minimum Clock differential voltage required for switching.

Capacitance (TA=0 to +70°C, VDD=3.3 –5% + 10% V, f=1MHz)

Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	C_{IN}	V_{IN} = 0V	3	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	V_{OUT} = 0V	4	pF

DC Electrical Characteristics (TA= 0 to +70°C, VDD=3.3 ± 5% V)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current - **X36** (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD4H} I_{DD5F} I_{DD5} I_{DD6} I_{DD7}	— —	750 675 675 580 510	mA	1
Average Power Supply Operating Current - **X18** (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD4H} I_{DD5F} I_{DD5} I_{DD6} I_{DD7}	— —	665 590 590 500 440	mA	1
Power Supply Standby Current (ZZ= V_{IH}, All other inputs = V_{IH} or V_{IL}, I_{OUT} = 0)	I_{SB}	—	25	mA	1
Input Leakage Current, any input (V_{IN} = V_{SS} or V_{DD})	I_{LI}	-1	+1	µA	
Output Leakage Current (V_{OUT} = V_{SS} or V_{DD}, DQ in HIZ)	I_{LO}	-1	+1	µA	
Output “High” Level Voltage (I_{OH}=-6mA @ V_{DDQ} / 2 + 0.3)	V_{OH}	V_{DDQ} / 2 + 0.3	V_{DDQ}	V	2
Output “Low” Level Voltage (I_{OL}=+6mA @ V_{DDQ} / 2 -0.3)	V_{OL}	V_{SS}	V_{DDQ} / 2 -0.3	V	2

1. I_{OUT} = Chip Output Current.
2. Minimum Impedance Output Driver.

Programmable Impedance Output Driver DC Electrical Characteristics

(T_A= 0 to +70°C, V_{DD}=3.3 - 5% + 10% V)

Parameter	Symbol	Min.	Max.	Units	Notes
Output "High" Level Voltage	V_{OH}	V_{DDQ} / 2	V_{DDQ}	V	1, 3
Output "Low" Level Voltage	V_{OL}	V_{SS}	V_{DDQ} / 2	V	2, 3

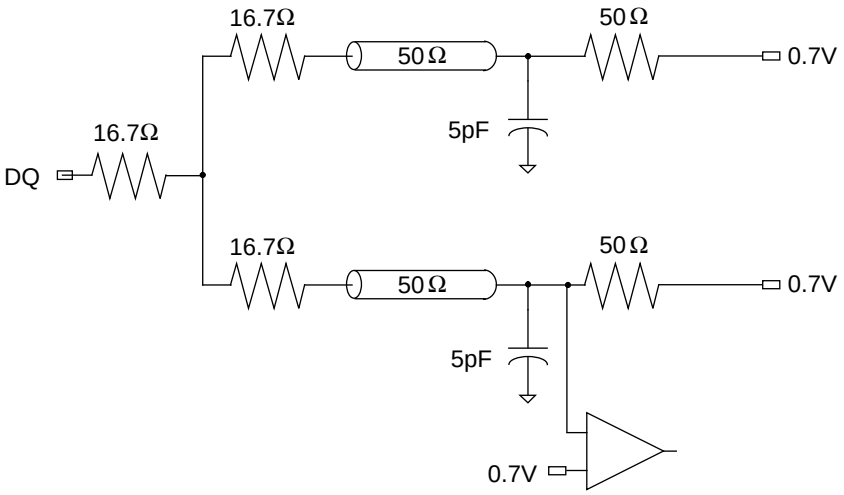
1. I_{OH} = (V_{DDQ} / 2) / (RQ / 5) +/- 25% @ V_{OH} = V_{DDQ} / 2 For: 185Ω ≤ RQ ≤ 350Ω.
2. I_{OL} = (V_{DDQ} / 2) / (RQ / 5) +/- 25% @ V_{OL} = V_{DDQ} / 2 For: 185Ω ≤ RQ ≤ 350Ω.
3. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.5 V.

AC Test Conditions (T_A=0 to +70°C, V_{DD}=3.3 – 5% + 10% V)

Parameter	Symbol	Conditions	Units	Notes
Input High Level	V_{IH}	1.4	V	
Input Low Level	V_{IL}	V_{SS}	V	
Input Reference Voltage	V_{REF}	0.7	V	
Differential Clocks Voltage	$V_{DIF-CLK}$	0.7	V	
Clocks Common Mode Voltage	V_{CM-CLK}	0.7	V	
Input Rise Time	T_R	0.5	ns	
Input Fall Time	T_F	0.5	ns	
I/O Signals Reference Level (except K, C Clocks)		0.7	V	
Clocks Reference Level		Differential Cross Point	V	
Output Load Conditions				1, 2

1. See AC Test Loading figure on page 9.
2. Parameter tested with RQ = 250Ω and V_{DDQ} = 1.4 V.

AC Test Loading

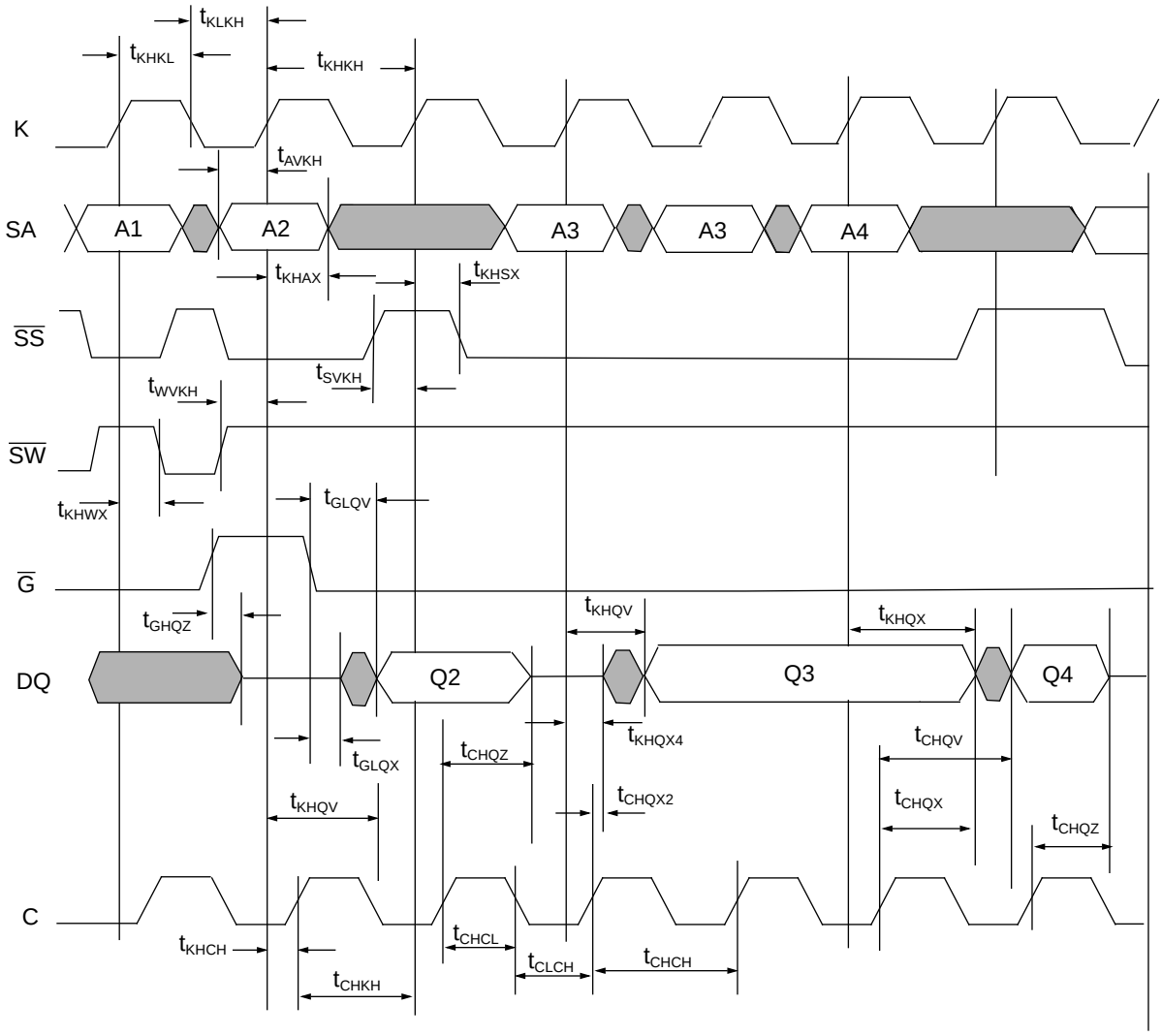


AC Characteristics (T_A=0 to +70°C, V_{DD}=3.3 – 5% + 10% V)

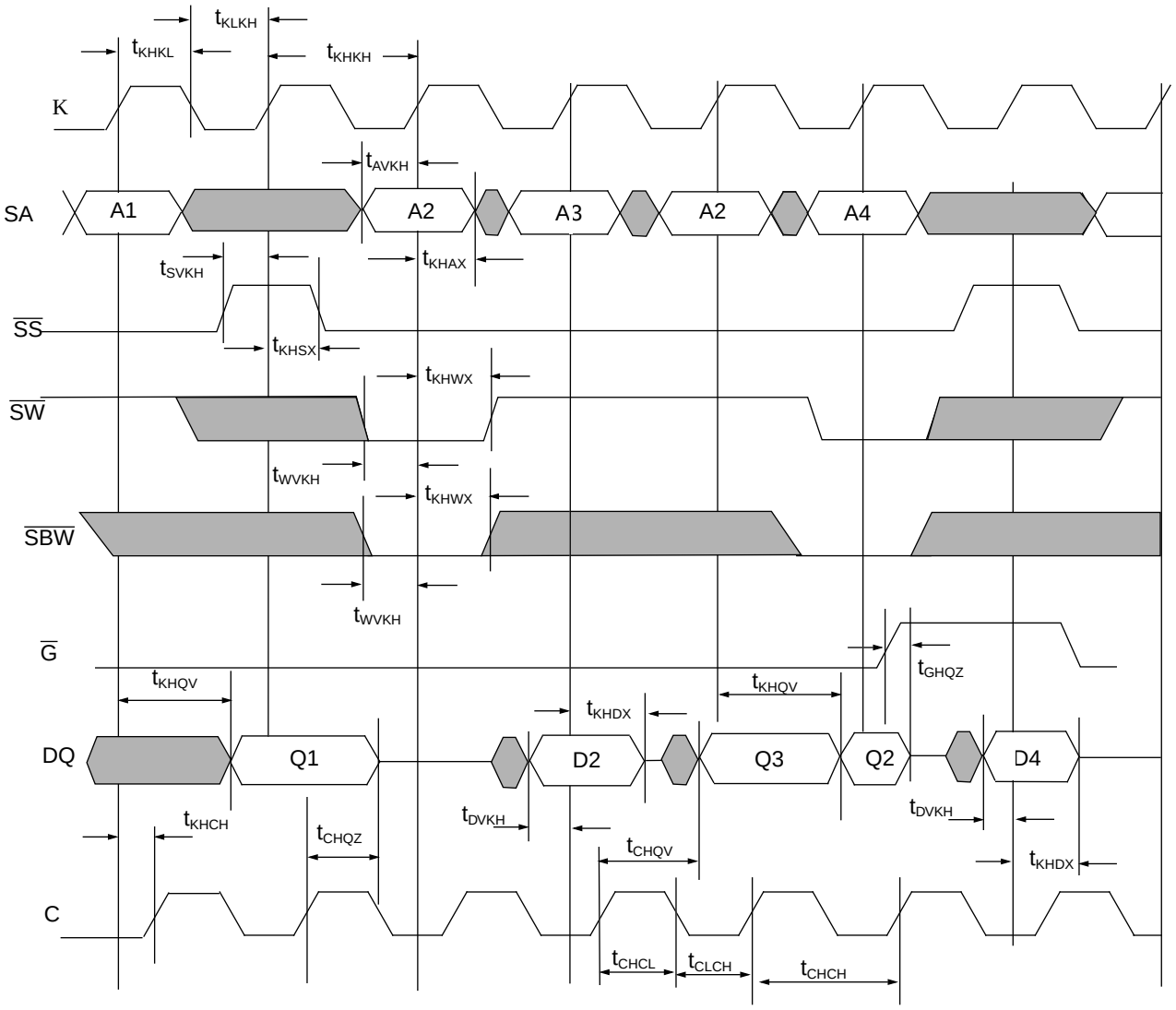
Parameter	Symbol	4H 64K X 18		4H 32K X 36		5F		5		6		7		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
K Clock Cycle Time	t_{KHKH}	4.5	—	4.5	—	5.0	—	5.0	—	6.0	—	7.0	—	ns	
K Clock High Pulse Width	t_{KHKL}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
K Clock Low Pulse Width	t_{KLKH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
C Clock Cycle Time	t_{CHCH}	5.0	—	5.0	—	5.0	—	5.0	—	6.0	—	7.0	—	ns	
C Clock High Pulse Width	t_{CHCL}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
C Clock Low Pulse Width	t_{CLCH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
K to C Clock Delay	t_{KHCH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
C to K Clock Delay	t_{CHKH}	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
K Clock to Output Valid	t_{KHQV}	—	5.9	—	6.4	—	6.8	—	7.0	—	7.5	—	8.0	ns	1
Data Out Hold Time from K Clock	t_{KHQX}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	1, 3
K Clock High to Output Active	t_{KHQX4}	2.5	—	2.5	—	2.5	—	2.5	—	3.0	—	3.0	—	ns	1, 3
C Clock to Output Valid	t_{CHQV}	—	2.6	—	2.7	—	3.0	—	3.0	—	3.0	—	3.5	ns	1, 4
Data Out Hold Time from C clock	t_{CHQX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	1, 4
C Clock High to Output High Z	t_{CHQZ}	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.5	ns	1
C Clock High to Output Active	t_{CHQX2}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	1, 4
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	5
Address Hold Time	t_{KHAX}	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Synchronous Select Setup Time	t_{SVKH}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	5
Synchronous Select Hold Time	t_{KHSX}	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Write Enables Setup Time	t_{WVKH}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	5
Write Enables Hold Time	t_{KHWX}	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Data In Setup Time	t_{DVKH}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	5
Data In Hold Time	t_{KHDX}	0.8	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
Output Enable to Output Valid	t_{GLQV}	—	2.5	—	2.5	—	2.5	—	2.5	—	3.0	—	3.5	ns	1
Output Enable to Low Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	1
Output Enable to High Z	t_{GHQZ}	—	2.3	—	2.3	—	2.5	—	2.5	—	3.0	—	3.5	ns	1
Output Enable Set-up Time	t_{GHKH}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	1, 2
Output Enable Hold TIme	t_{KHGX}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	1, 2
Sleep Mode Recovery TIme	t_{ZZR}	5	—	5	—	5	—	5	—	6	—	7	—	ns	
Sleep Mode Enable TIme	t_{ZZE}	—	5	—	5	—	5	—	5	—	6	—	7	ns	

1. See AC Test Loading figure on page 9.
2. Output Driver Impedance update specifications for $\overline{G}$ induced updates. Write and Deselect cycles will also induce Output Driver updates during High Z.
3. t_{KHQX} and t_{KHQX4} are used in instances where t_{KHCH} = Min. and, therefore, the C Clock may not gate the output data.
4. t_{CHQV}, t_{CHQX} and t_{CHQX2} are used in instances where the output data is gated by the C Clock.
5. 4H sort Setup times tested/verified at 5ns cycle time.

Timing Diagram (Read and Deselect Cycles)



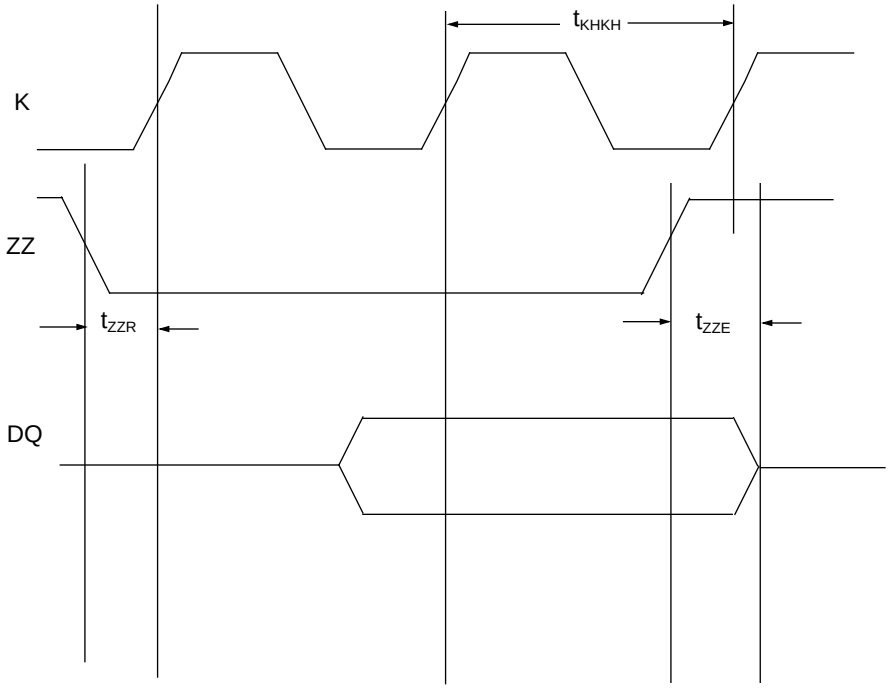
Timing Diagram (Read Followed by Write)



Notes:

1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

Timing Diagram (Sleep Mode)



IEEE 1149.1 Tap And Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAMs contain a TAP controller, Instruction register, Boundary Scan register, Bypass register and ID register.

The TAP controller has a standard 16-state state machine that resets internally upon power-up. Therefore, TRST signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

Caution: TCK, TMS, TDI inputs must be biased to a valid logic level, even if JTAG is not used.

JTAG Recommended DC Operating Conditions (T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.2	—	V_{DD}+0.3	V	1
JTAG Input Low Voltage	V_{IL1}	-0.3	—	0.8	V	1
JTAG Output High Level	V_{OH1}	2.4	—	—	V	1, 2
JTAG Output Low Level	V_{OL1}	—	—	0.4	V	1, 3

1. All JTAG Inputs/Outputs are LVTTL compatible only.
2. I_{OH1} = -8mA at 2.4V.
3. I_{OL1} = +8mA at 0.4V.

JTAG AC Test Conditions (T_A=0 to +70°C, V_{DD}=3.3 -5% + 10% V)

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V_{IH1}	3.0	V	
Input Pulse Low Level	V_{IL1}	0.0	V	
Input Rise Time	T_{R1}	2.0	ns	
Input Fall Time	T_{F1}	2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

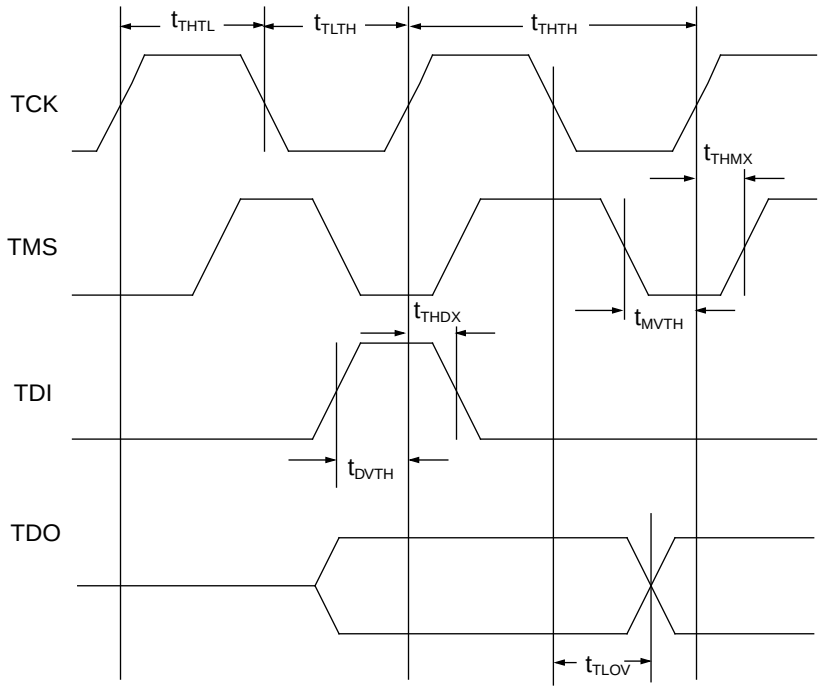
1. See AC Test Loading figure on page 9.

JTAG AC Characteristics (T_A=0 to +70°C, V_{DD}=3.3 -5% + 10% V)

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	t_{THTH}	20	—	ns	
TCK High Pulse Width	t_{THTL}	7	—	ns	
TCK Low Pulse Width	t_{TLTH}	7	—	ns	
TMS Setup	t_{MVTH}	4	—	ns	
TMS Hold	t_{THMX}	4	—	ns	
TDI Setup	t_{DVTH}	4	—	ns	
TDI Hold	t_{THDX}	4	—	ns	
TCK Low to Valid Data	t_{TLOV}	—	7	ns	1

1. See AC Test Loading figure on page 9.

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size X18	Bit Size X36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

* The Boundary Scan chain consists of the following bits:
- 36 or 18 bits for Data Inputs Depending on X18 or X36 Configuration
- 15 bits for SA0 - SA14 for X36, 16 bits for SA0 - SA15 for X18
- 4 bits for $\overline{\text{SBWa}}$ - $\overline{\text{SBWd}}$ in X36, 2 bits for $\overline{\text{SBWa}}$ and $\overline{\text{SBWb}}$ in X18
- 11 bits for K, $\overline{\text{K}}$, C, $\overline{\text{C}}$, ZQ, $\overline{\text{SS}}$, $\overline{\text{G}}$, $\overline{\text{SW}}$, ZZ, M1 and M2
- 4 bits for Place Holders

* K, $\overline{\text{K}}$, C, $\overline{\text{C}}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit (0)
64K X18	0000	001 000 0011	000000	000 101 001 00	1
32K X36	0000	000 110 0100	000000	000 101 001 00	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1, 5
001	IDCODE	2
010	SAMPLE-Z	1, 5
011	BYPASS	3
100	SAMPLE	4, 5
101	PRIVATE	3, 6
110	BYPASS	3
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initialized to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. SRAM must not be in Sleep mode (ZZ = H) when SAMPLE-Z or SAMPLE instructions are invoked.
6. This instruction is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

List of IEEE 1149.1 standard violations:
- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d

Boundary Scan Order (X36)

(PH =Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	**25**	DQ15	6F	**49**	DQ22	2H
2	SA0	4P	**26**	DQ16	7E	**50**	DQ26	1H
3	SA12	4T	**27**	DQ11	6E	**51**	$\overline{\text{SBWc}}$	3G
4	SA10	6R	**28**	DQ12	7D	**52**	ZQ	4D
5	SA11	5T	**29**	DQ17	6D	**53**	$\overline{\text{SS}}$	4E
6	ZZ	7T	**30**	SA3	6A	**54**	$\overline{\text{C}}$	4G
7	DQ0	6P	**31**	SA2	6C	**55**	C	4H
8	DQ5	7P	**32**	SA5	5C	**56**	$\overline{\text{SW}}$	4M
9	DQ6	6N	**33**	SA4	5A	**57**	$\overline{\text{SBWd}}$	3L
10	DQ1	7N	**34**	PH*	6B	**58**	DQ27	1K
11	DQ2	6M	**35**	PH*	5B	**59**	DQ31	2K
12	DQ7	6L	**36**	PH*	3B	**60**	DQ32	1L
13	DQ3	7L	**37**	PH*	2B	**61**	DQ28	2L
14	DQ4	6K	**38**	SA7	3A	**62**	DQ33	2M
15	DQ8	7K	**39**	SA6	3C	**63**	DQ34	1N
16	$\overline{\text{SBWa}}$	5L	**40**	SA9	2C	**64**	DQ29	2N
17	$\overline{\text{K}}$	4L	**41**	SA8	2A	**65**	DQ30	1P
18	K	4K	**42**	DQ18	2D	**66**	DQ35	2P
19	$\overline{\text{G}}$	4F	**43**	DQ23	1D	**67**	SA13	3T
20	$\overline{\text{SBWb}}$	5G	**44**	DQ24	2E	**68**	SA14	2R
21	DQ9	7H	**45**	DQ19	1E	**69**	SA1	4N
22	DQ13	6H	**46**	DQ20	2F	**70**	M1	3R
23	DQ14	7G	**47**	DQ25	2G			
24	DQ10	6G	**48**	DQ21	1G			

1. * Input of PH register connected to V_{SS}.
2. ** Input of PH register connected to V_{DD}.

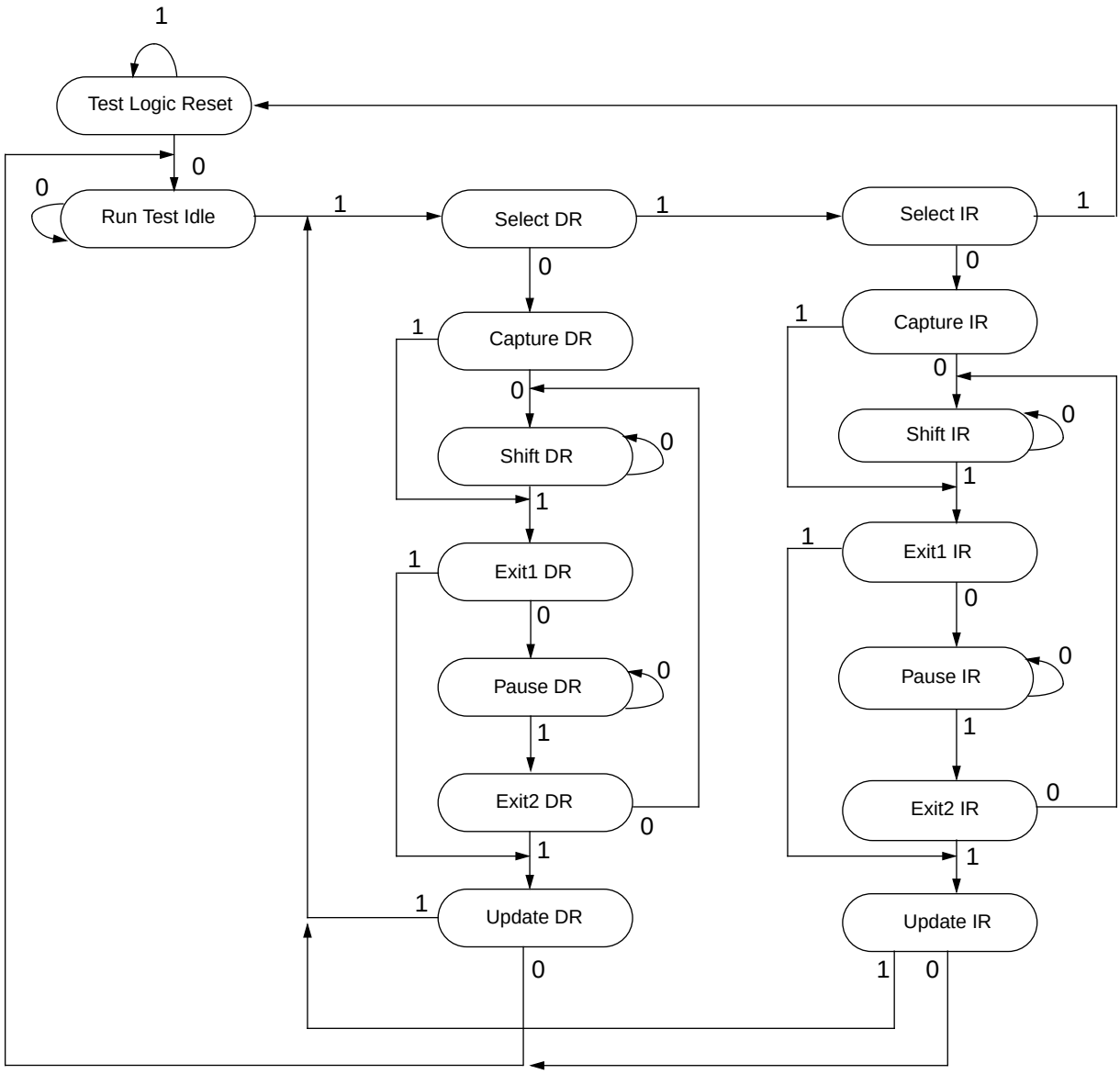
Boundary Scan Order (X18)

(PH =Place Holder)

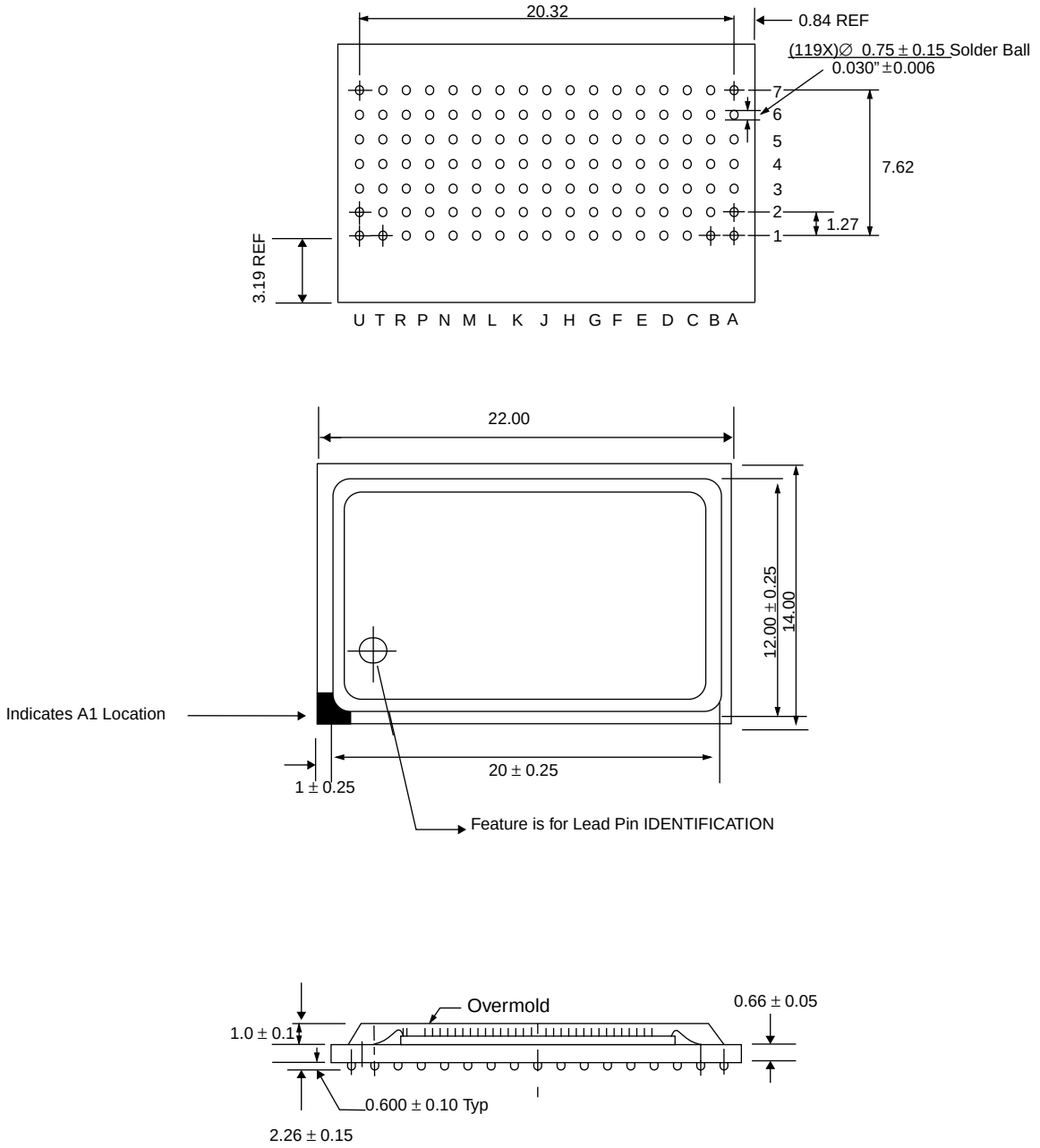
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	**27**	PH*	2B
2	SA10	6T	**28**	SA7	3A
3	SA0	4P	**29**	SA6	3C
4	SA11	6R	**30**	SA9	2C
5	SA12	5T	**31**	SA8	2A
6	ZZ	7T	**32**	DQ9	1D
7	DQ0	7P	**33**	DQ10	2E
8	DQ1	6N	**34**	DQ11	2G
9	DQ2	6L	**35**	DQ12	1H
10	DQ3	7K	**36**	$\overline{\text{SBWb}}$	3G
11	$\overline{\text{SBWa}}$	5L	**37**	ZQ	4D
12	$\overline{\text{K}}$	4L	**38**	$\overline{\text{SS}}$	4E
13	K	4K	**39**	$\overline{\text{C}}$	4G
14	$\overline{\text{G}}$	4F	**40**	C	4H
15	DQ4	6H	**41**	$\overline{\text{SW}}$	4M
16	DQ5	7G	**42**	DQ13	2K
17	DQ6	6F	**43**	DQ14	1L
18	DQ7	7E	**44**	DQ15	2M
19	DQ8	6D	**45**	DQ16	1N
20	SA3	6A	**46**	DQ17	2P
21	SA2	6C	**47**	SA14	3T
22	SA5	5C	**48**	SA15	2R
23	SA4	5A	**49**	SA1	4N
24	PH*	6B	**50**	SA13	2T
25	PH*	5B	**51**	M1	3R
26	PH*	3B			

1. * Input of PH register connected to V_{SS}
2. ** Input of PH register connected to V_{DD}

TAP Controller State Machine



7 x 17 BGA Dimensions



Note: All dimensions in Millimeters.

Revision Log

Rev	Contents of Modification
6/94	Initial Release of the 32K x 36 & 64K x 18 (5/6/7) BGA FLOW THRU Application Spec.
1/95	Addition of SRAM Features section. Changed parameter/signal names for JEDEC compatibility.
2/95	Add package dimensions and identify SA and DQ pins.
4/95	Correct ZQ in X36 pinout.
5/95	Release to Fax Server.
7/95	WWW Release.
9/95	Change tCHQV specs.
4/96	Parameter updates.
5/96	Output Impedance and Power updates.
7/96	t_{KHQX4} changed from 3.5ns to 3.0ns at 7ns cycle time.
5/97	Add 4H sorts to datasheet.

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