Spread Spectrum Clock Generator for Pentium® & Pentium® II, 3 DIMM Designs

Preliminary

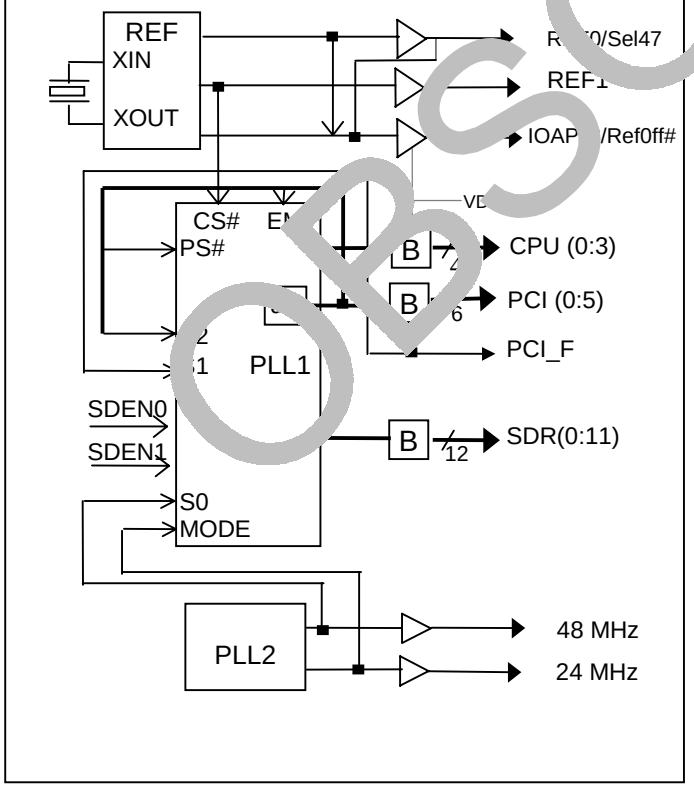
PRODUCT FEATURES

- Supports Pentium®, Pentium®II, M2 and K6.
- Supports 430TX and 440LX chipset requirements.
- 4 CPU clocks
- Up to 12 SDRAM clocks for 3 DIMMs.
- 7 PCI synchronous clocks.
- Optional common or mixed supply mode:
- (Vdd = Vddq3 = Vddq2 = 3.3V) or
- (Vdd = Vddq3 = 3.3V, Vddq2 = 2.5V)
- < 250ps skew among CPU or SDRAM clocks.
- < 250ps skew among PCI clocks.
- Power Management Capability.
- IOAPIC clocks for multiprocessor support.
- 48 MHz for USB support
- 48-pin SSOP package
- **Integrates EMI reduction SSCG technology for upto 15dB attenuation.**

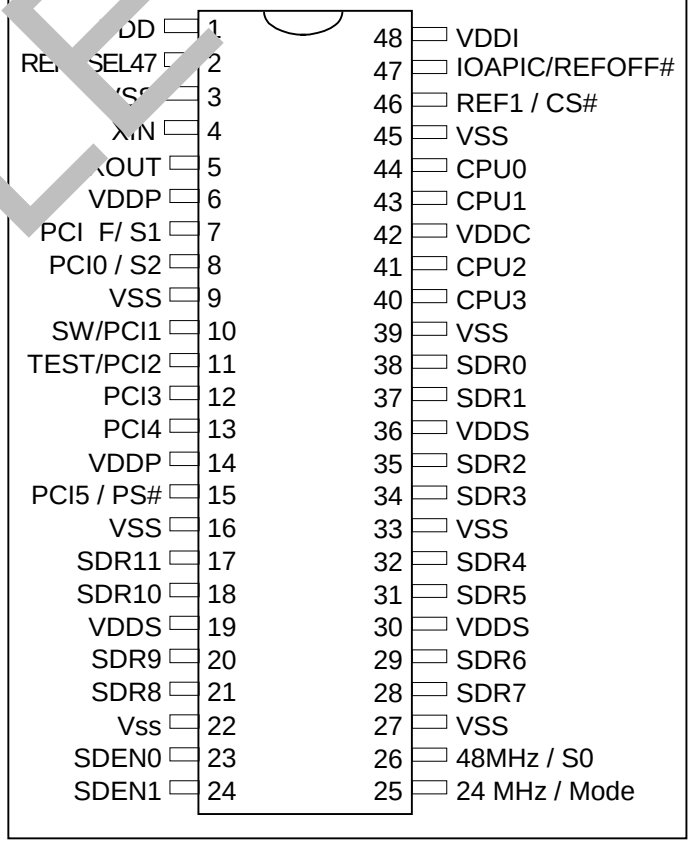
FREQUENCY TABLE (MHz)

S2	S1	S0	CPU	PCI
0	0	0	50	25
0	0	1	75	30
0	1	0	83.3	33.3
0	1	1	100	33.3
1	0	0	55	27.5
1	0	1	75	37.5
1	1	0	60	30
1	1	1	66.8	33.4

BLOCK DIAGRAM



CONNECTION DIAGRAM



NOTE : Purchase of I^2C components of International Microcircuits, Inc. or one of its sublicensed Associated Companies conveys a license under the Phillips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Phillips.

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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
4	**Xin**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	VDD	O	OSC1	O-chip reference oscillator output pin. Drives an external crystal When an externally generated reference signal is used, is left unconnected
46	**REF1**	VDD	O	BUF	This pin is bidirectional. If pin 25, MODE = 1 (default), then this pin is a REF1 buffered output of the crystal. If pin 25, MODE = 0 then this pin is CS# and is used in power management mode for synchronously stopping all CPU clocks (see page 4).
	CS#	-	I	PADI4 PU	
2	**REF0**				This pin is bidirectional. If it is pulled low with a programming resistor at power up then pin 47 is configured as an input pin which will act as a reference enable pin for pin 2 (this pin). If this pin is high (no programming resistor) at power up, then this pin is a REF1 buffered output of the crystal.
	SEL47				
44, 43, 41, 40	**CPU(0:3)**	VDDC	O	BUF1	Clock outputs CPU frequency table specified on page 1.
47	**IOAPIC**	VDDI	O	BUF2	IOAPIC clock for multiprocessor support. Fixed frequency at 14.31818 Mhz. This is a bidirectional pin. If Sel47 = 1, becomes IOAPIC output powered by VDDq2. If Sel47 = 0, becomes input pin with internal pull-up. When Refoff# = 1 (default), then REF0 is enabled, if Refoff# is 0, then REF0 is disabled.
	REFOFF#	-	I	PAD	
12, 13	**PCICLK(3:4)**	VDDP	O	BUF4	PCI bus clocks. See frequency select table on page 1.
11	**PCI2**	VDDP	O	BUF4	Low skew (<250pS) PCI clock outputs. This pin is bidirectional. During power-up, It is an input (TEST) and is used for configure the output frequency of CPU, SDRAM and PCI clocks into the TEST mode. When the power reaches the VDD rail (See Fig.1), the selected data is latched internally to the IC
	TEST	-	AD		and this pins become PCI_F clock output.
7	**PCI_F**	VDDP	O	BUF4	Low skew (<250pS) PCI clock outputs. This pin is bidirectional. During power-up, It is an input (S1) and is used for HARD selecting the output frequency of CPU, SDRAM and PCI clocks, see Frequency table page1. When the power reaches the VDD rail (See Fig.1), the selected data is latched internally to the IC and this pins become PCI_F clock output.
	S1	-	I		
10	**PCI1**	VDDP	O	BUF4	Low skew (<250pS) PCI clock outputs. This pin is bidirectional. During power-up, It is an input (SW) and is used for HARD selecting the spreading width of the EMI reducing modulation. When the power reaches the VDD rail (See Fig.1), the data bit is latched internally in the IC and this pin becomes PCI1 clock output.
	Sw	-	I	PAD	
23,24	**sden [0:1]**	-	1	PAD	SDRAM clock enable pins. When these pins are brought to a Loigc 0 (low) level, they tri-state the SDRAM buffers they control. SDEN0 Controls SDRAM 4:7, SDEN1 controls SDRAM 8:11.

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PIN DESCRIPTION (Cont.)

PIN No.	Pin Name	PWR	I/O	TYPE	Description
8	**PCI0**	VDDP	O	BUF4	Low skew (<250pS) PCI clock outputs. This pin is bidirectional. During power-up, it is an input (S2) and is used for HARD selecting the output frequency of CPU, SDRAM and PCI clocks, see Frequency table page 1. When the power reaches the VDD rail (See Fig.1), the selected data is latched internally to the IC
	S2	-	I	PAD	and this pin become PCI0 clock output.
15	**PCI5**	VDD	0	BUF4	Low skew (<250pS) PCICLK output. If mode is set to a 1 logic (high state). If mode is set to a logic 0 (low state), this pin acts as
	PS#		I	PAD	a PCI_STOP control for power management. As such, it will disable all PCI clocks when brought low (logic 0 low state) level.
17, 18, 20, 21, 28,29,31,32, 34,35,37,38	**SDR[0:11]**	VDDS	I	PAD	Synchronous DRAM clocks, SDRAM clock frequency = CPU clock frequency.
3, 9, 16, 22, 27, 33, 39, 45	**VSS**	-	P	-	Ground pins for the device.
6, 14	**VDDP**	-	P	-	3.3 Volt power supply pin for PCI and PCI_F clock output buffers.
42, 48	**VDDC**	-	P	-	3.3 or 2.5 V power supply for CPU and IOAPIC clock buffers.
1	**VDD**	-	P		Power supply pin for analog circuits and core logic
25	**24 Mhz**				This is a bidirectional pin. During power-up, this pin is an input and is used for enabling (0) or disabling (1, default) the power
	MODE				management pins 15 and 46. When power reaches the VDD rail (See Fig. page3), the selected data is latched internally to the device this pin becomes a 24 Mhz output clock.
26	**48 Mhz**				Low skew (<250pS) PCI clock outputs. This pin is bidirectional. During power-up, It is an input (S0) and is used for HARD selecting the output frequency of CPU, SDRAM and PCI clocks, see Frequency table page1. When the power reaches the VDD rail (See Fig.1), the selected data is latched internally to the IC
	S0				and this pins become 48 MHz clock output.
19, 36, 30	**VDDS**		P		Power for SDRAM buffers.

SDen1	Sden0	SDRAM	SDRAM(8:11)
0	0		
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	ON

A bypass capacitor (0.1µF) should be placed as close as possible to each Vdd, Vddq2, and Vddq3 pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductances of the traces.

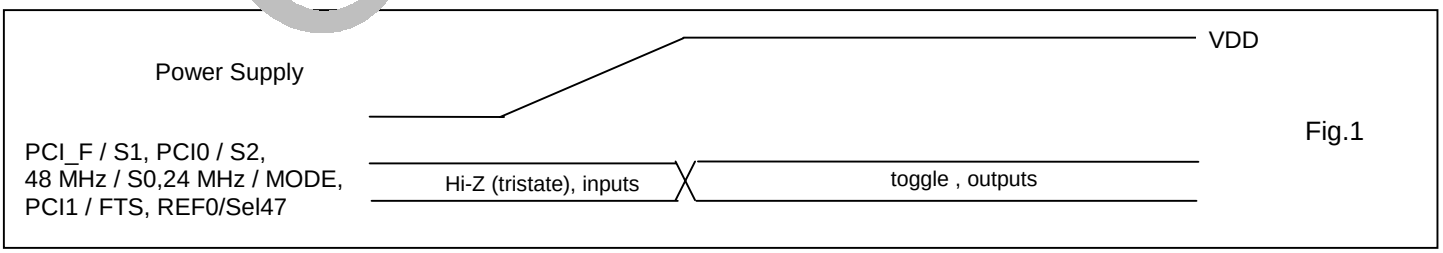

Fig.1

Spread Spectrum Clock Generator for Pentium® & Pentium® II, 3 DIMM Designs

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POWER MANAGEMENT FUNCTIONS

When MODE=0, pins 15 and 46 are inputs PS# (PCI_STOP#), and CS# (CPU_STOP#), respectively (when MODE=1, these functions are not available). The IMISG742 clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. The CPU/AGP and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	CPU	PCI	OTHER CLK	XTAL & VCOs
0	0	LOW	LOW	RUNNING	RUNNING
0	1	LOW	See Frequency Table	RUNNING	RUNNING
1	0	See Frequency Table	LOW	RUNNING	RUNNING
1	1	See Frequency Table	See Frequency Table	RUNNING	RUNNING

All clocks are stopped in the low state.

POWER MANAGEMENT TIMING

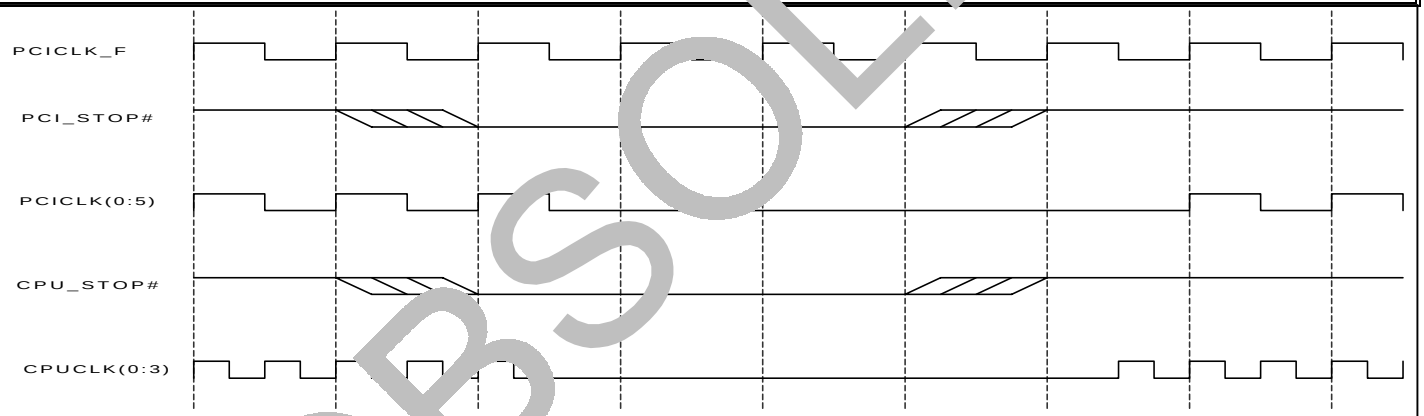

Fig. 2

Spread Spectrum Clock Generator for Pentium® & Pentium® II, 3 DIMM Designs

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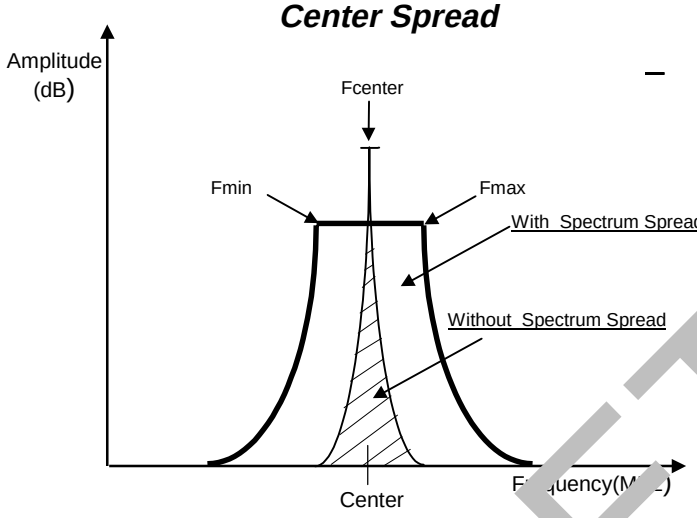
SPECTRUM SPREAD CLOCKING

Center Spread



Spectrum Analysis

SPECTRUM SPREADING SELECTION TABLE (CONT)

Unspread CPU frequency in MHz	Center Spreading									
	SWI=0					SW=1 (default)				
desired	Unspread (MHz)	F Min (MHz)	F Center (MHz)	F Max (MHz)	Spread (total %)	Unspread (MHz)	F Min (MHz)	F Center (MHz)	F Max (MHz)	Spread (total %)
50	50.11		49.97		1.8	50.11		49.97		1
75	74.99		75.1		1.8	74.99		75.13		1
83.3	83.18		83.[illegible]1		1.8	83.18		83.51		1
100	100.22		99.94		1.8	100.22		99.94		1
55	55.23		55.21		1.8	55.23		55.21		1
75	74.99		75.12		1.8	74.99		75.12		1
60	59.99		60.10		1.8	59.99		60.10		1
66.8	66.82		66.74		1.8	66.82		66.74		1

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0ºC to + 125ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-		10	µA	
Dynamic Supply Current	Idd	-		116	mA	CPU = 66.6 MHz, PCI = 33.3 Mhz Unloaded
Static Supply Current	Isdd	-		13	µA	-
Short Circuit Current	ISC		-	-	mA	1 output at a time - 30 seconds
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC						

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Skew (CPU-CPU), (SDRAM-SDRAM)	tSKEW1	-	-	250	ps	15 pf Load Measured at 1.5V
Skew (CPU-SDRAM), (PCI-PCI)	tSKEW2	-	-	500	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Overshoot/Undershoot Beyond Power Rails	V_{over}	-	-	1.5	V	22 ohms @ source of 8 inch PCB run to 15 pf load
VDD = VDDQ3 =3.3V ±5%, VDDQ2 =2.5 ± 5%, TA = 0ºC to +70ºC						

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TYPE 1 BUFFER CHARACTERISTICS FOR CPU (0:3)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-27	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-27	mA	Vout = 2.6 V
Pull-Down Current Min	IOL_{min}	-27	-	-	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.6	nS	20 pF Load
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC						

TYPE 2 BUFFER CHARACTERISTICS FOR IOAPIC, REF1						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-28	-	-	mA	Vout = 1.4 V
Pull-Up Current Max	IOH_{max}	-	-	-28	mA	Vout = 2.7 V
Pull-Down Current Min	IOL_{min}	-28	-	-	mA	Vout = 1.0 V
Pull-Down Current Max	IOL_{max}	-	-	28	mA	Vout = 0.2 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.6	nS	20 pF Load
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC						

TYPE 3 BUFFER CHARACTERISTICS FOR REF0 and SDRAM(0:11)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-46	-	-	mA	Vout = 1.65 V
Pull-Up Current Max	IOH_{max}	-	-	-46	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	-46	-	-	mA	Vout = 1.65 V
Pull-Down Current Max	IOL_{max}	-	-	53	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	1.3	nS	30 pF Load
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC						

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TYPE 5 BUFFER CHARACTERISTICS FOR PCI_F AND PCI(0:5)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Condition**
Pull-Up Current Min	IOH_{min}	-33	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-33	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	30	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	38	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	15 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2	nS	30 pF Load
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC						

TYPE 6 BUFFER CHARACTERISTICS FOR 24 MHZ AND 48 MHZ						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}				mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-46	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}		-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IO_{max}	-		53	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	15 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TR_{max}	-	-	2	nS	50 pF Load
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5 ± 5%, TA = 0ºC to +70ºC						

Application Note for Selection on Bidirectional Pins

Pins 2, 7, 8, 10, 25, and 26 are bidirectional pins and are used for selecting different functions in this device (see Pin description, Pages 2&3). During power-up of the SG742, these pins are in input mode (see Fig1, page3), therefore, they are considered input select pins. Internal to the IC, these pins have a large value pull-up each (100KΩ), therefore, a selection "1" is the default. If a selection "0" is desired, then a direct connection to ground through a 10KΩ resistor should be implemented as shown in Fig.3. Please note the selection resistor (10KΩ) is placed before the Damping resistor (Rd) close to the pin.

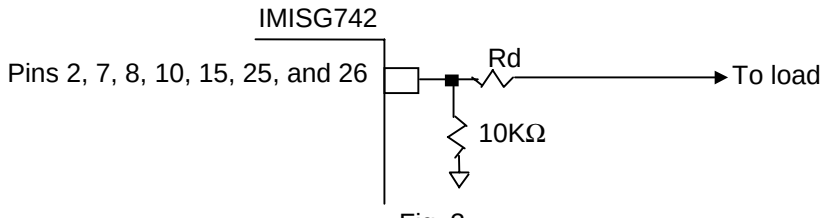

Fig. 3

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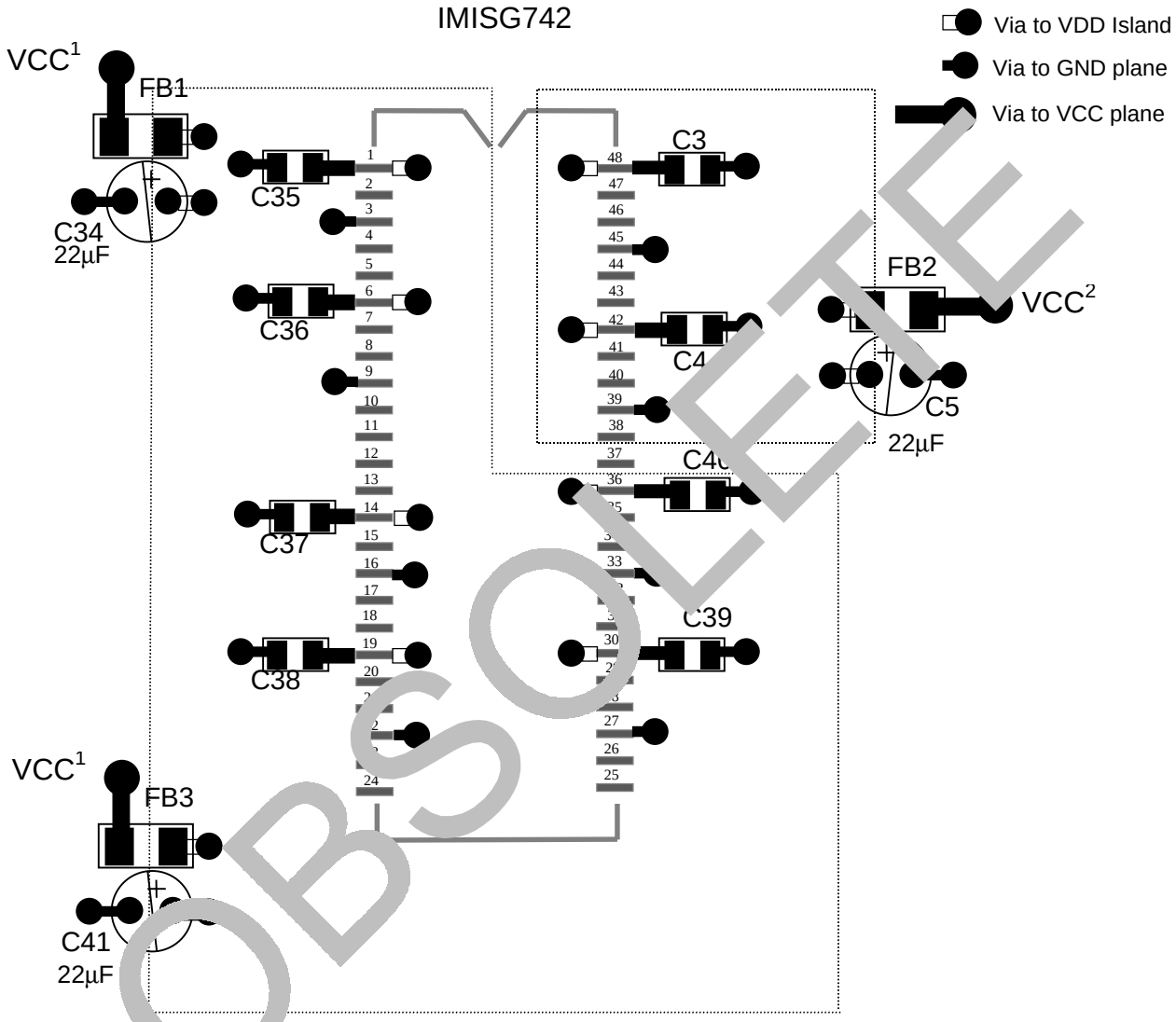
PCB LAYOUT SUGGESTION



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C3, C4, C35, C36, C37, C38, C39and C40 (all are 0.1µf) should always be used and placed as close as possible to their VDD pins.

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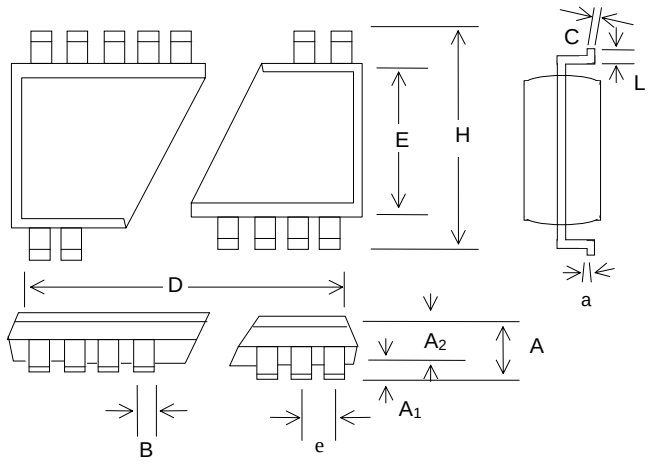
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.01	0.20	0.30	0.41
A2	0.085	.090	95	2.1	2.29	2.41
b	0.008	0.010	0.01	.20	0.25	0.33
C	0.0 6	0 08	0.010	0.15	0.20	0.25
D		0.62	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
	0.025 BSC			0.64 BSC		
H	.395	0 08	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0	5º	8º	0º	5º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG742AYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG742AY
Date Code, #
IMISG742AY

Flow
= Commercial, 0ºC to + 70ºC

Package
Y = SSOP

Revision

IMI Device Number