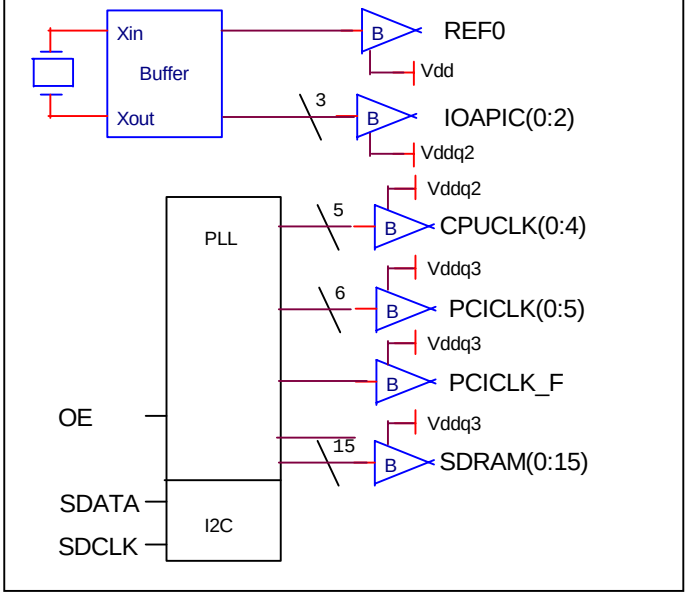
Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

PRODUCT FEATURES

- Supports Pentium™ and Pentium™ II CPU's
- Supports 440LX chipset
- Designed to Intel chipset specification
- Spread Spectrum EMI reduction mode
- 5 CPU / AGP clocks
- Up to 16 SDRAM clocks for 4 DIMMs.
- 7 PCI synchronous clocks.
- Optional common or mixed supply mode:
- (Vdd = Vddq3 = Vddq2= 3.3V) or
- (Vdd = Vddq3 = 3.3V, Vddq2 = 2.5V)
- Supports Power Management Function
- < 250ps skew CPU and SDRAM clocks.
- < 250ps skew among PCI clocks.
- I²C 2-Wire serial interface
- Programmable registers featuring:
  - enable/disable each output pin
  - mode as tri-state, test, or normal
- 3 IOAPIC clocks for multiprocessor support.
- 56-pin SSOP package

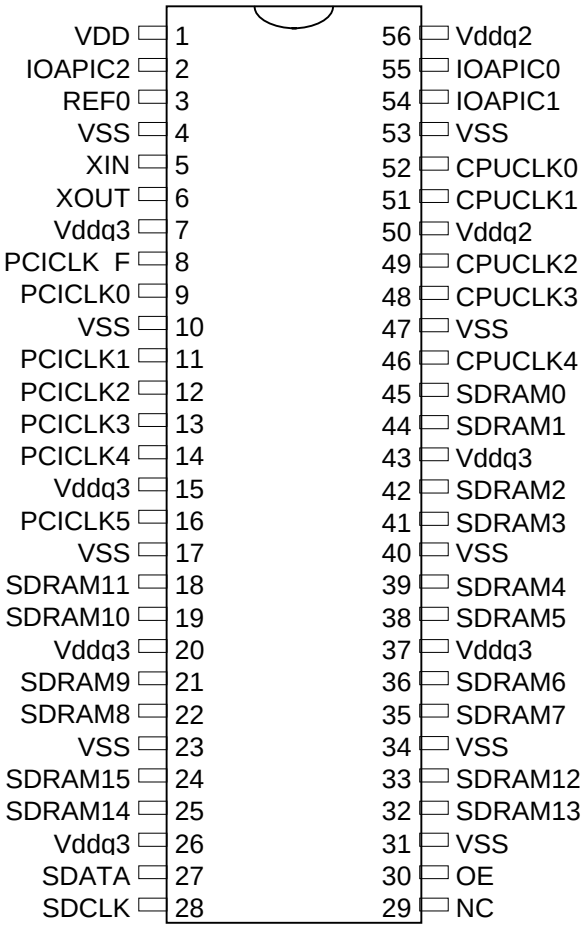
BLOCK DIAGRAM



FREQUENCY TABLE

OE	CPU	PCI
0	All output clocks tristated	
1	66.58	33.29

CONNECTION DIAGRAM



Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

PIN DESCRIPTION

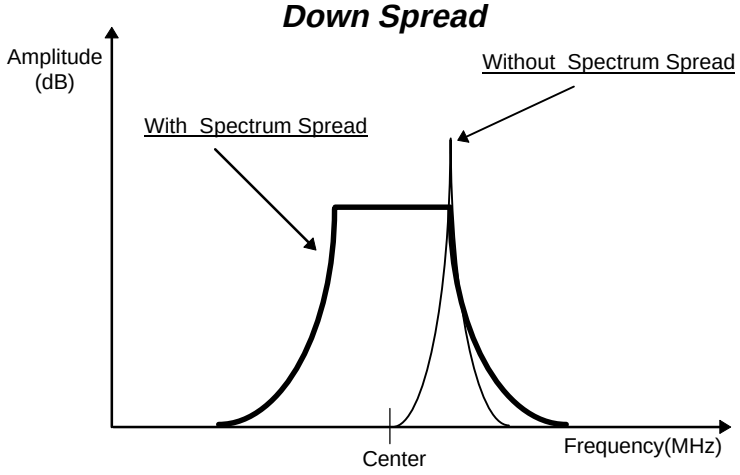
PIN No.	Pin Name	PWR	I/O	TYPE	Description
5	**Xin**	Vdd	I	OSC1	On-chip reference oscillator input pin. Requires either an external crystal (nominally 14.318 MHz) or externally generated reference signal
6	**Xout**	Vdd	O	OSC1	O-chip reference oscillator output pin. Drives an external crystal When an externally generated reference signal is used, is left unconnected
29	**NC**	-	-	-	No Connection should be made to this pin.
52, 51, 49, 48, 46	**CPU(1:5)**	Vddq2	O	1	Clock outputs. CPU frequency table specified on page 1.
55, 54, 2	**IOAPIC(1:2)**	Vddq2	O	2	IOAPIC clock for multi proscssor support. Fixed frequency at 14.31818 Mhz. (2.5 or 3.3 supply = VDDI)
8, 9, 11, 12, 13, 14, 16	**PCI(1:7)**	Vddq3	O	5	PCI bus clocks. See frequency select table on page 1.
30	**OE**	-	I	PAD PU	Output Enable Tristates all clock outputs when at a logic 0 (LOW) level. This pin has an internal pull-up
27	**SDATA**	-	I/O	PAD	Serial I2C control interface data pin.
28	**SCLK**	-	I	PAD	Serial I2C control interface clock pin.
4, 10, 17, 23, 31, 34, 40, 47, 53	**VSS**	-	P	-	Ground pins for the device.
3	**REF**	Vdd	O	4	Buffered copy of the 14.31818 Mhz reference oscillator.
7, 15, 20, 26, 37, 43	**VDDQ3**	-	P	-	3.3 Volt power supply pin for SDRAM, PCI clock output buffers.
56, 50	**VDDQ2**	-	P	-	3.3 or 2.5 V power supply for CPU and IOAPIC clock buffers.
1	**VDD**	-	P		Power supply pins for analog circuits and core logic
45, 44, 42, 41, 39, 22, 21, 19, 18, 33, 32, 25, 24, 35, 36, 38	**SDRAM(1:16)**	Vddq3	O	4	High drive SDRAM output clocks.

Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

SPECTRUM SPREAD CLOCKING

Down Spread



Spectrum Analysis

SPECTRUM SPREADING SELECTION TABLE

Min (MHz)	Center (MHz)	Max (MHz)	Unspread CPU Frequency	% OF FREQUENCY SPREADING	MODE
66.16	66.37	66.58	66	.625% (-.625% + 0%)	Down Spread
65.91	66.25	66.58	66	1.0% (-1.0% + 0%)	Down Spread

2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The IMISG579 cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The IMISG579 will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The IMISG579 will not respond to any other control interface conditions. Previously set control registers are retained.

Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

Byte 0: Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved. Don't set
6	0	-	Reserved. Don't set
5	0	-	Reserved. Don't set
4	0	-	Reserved. Don't set
3	1	-	Reserved
2	0	-	0 = 0.625% Down Spreading 1 = 1.0% Down Spreading
1 0	0 0		Bit1 Bit0 1 1 Tri-State 1 0 Spread Mode On 0 1 Test Mode 0 0 Normal

IMPORTANT NOTE

Reserved bits are intended for possible future functions. It is important that they be left at their Power Up logic levels at all times. Otherwise data sheet specifications cannot be guaranteed.

Note: The OE pin is logically or'ed with the Byte 0 bit 0=1 and bit 1=1 Tri-State function. It does not set, reset or cause these bits to change.

Function Table

Function Description	Outputs				
	CPU	PCI	SDRAM	Ref	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	Tclk/2	Tclk/4	Tclk/2	Tclk	Tclk
Normal	66	CPU/2	CPU	14.318	14.318

Notes:
1. Tclk is a test clock over driven on the Xin input during test mode.

Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

SERIAL CONTROL REGISTERS (Cont.)

Byte 1: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	Reserved for IMI test. Must be set to 1
6	x	-	Reserved
5	x	-	Reserved
4	1	46	CPUCLK4 enable/Stopped
3	1	48	CPUCLK3 enable/Stopped
2	1	49	CPUCLK2 enable/Stopped
1	1	51	CPUCLK1 enable/Stopped
0	1	52	CPUCLK0 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	8	PCICLK_F enable/Stopped
5	1	16	PCICLK5 enable/Stopped
4	1	14	PCICLK4 enable/Stopped
3	1	13	PCICLK3 enable/Stopped
2	1	12	PCICLK2 enable/Stopped
1	1	11	PCICLK1 enable/Stopped
0	1	9	PCICLK0 enable/Stopped

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	35	SDRAM7 enable/Stopped
6	1	36	SDRAM6 enable/Stopped
5	1	38	SDRAM5 enable/Stopped
4	1	39	SDRAM4 enable/Stopped
3	1	41	SDRAM3 enable/Stopped
2	1	42	SDRAM2 enable/Stopped
1	1	44	SDRAM1 enable/Stopped
0	1	45	SDRAM0 enable/Stopped

Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

SERIAL CONTROL REGISTERS (Cont.)

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	24	SDRAM15 enable/Stopped
6	1	25	SDRAM14 enable/Stopped
5	1	32	SDRAM13 enable/Stopped
4	1	33	SDRAM12 enable/Stopped
3	1	18	SDRAM11 enable/Stopped
2	1	19	SDRAM10 enable/Stopped
1	1	21	SDRAM9 enable/Stopped
0	1	22	SDRAM8 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	2	IOAPIC2 enable/Stopped
5	1	54	IOAPIC1 enable/Stopped
4	1	55	IOAPIC0 enable/Stopped
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	1	3	REF enable/Stopped

Byte 6: Reserved Register

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	88	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	130	µA	OE = 0
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

Vdd = Vddq3 =3.3V ±5%, Vddq2 = 2.5V ±5%,, TA = 0ºC to +70ºC

Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Skew (CPU-CPU,SDRAM-SDRAM,PCI-PCI)	tSKEW1	-	-	250	ps	15 pf Load Measured at 1.5V
Skew (CPU-SDRAM)	tSKEW2	-	-	500	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Vdd = Vddq3 =3.3V ±5%, Vddq2 = 2.5V ±5%,, TA = 0ºC to +70ºC						

TB40A_V TYPE BUFFER CHARACTERISTICS FOR IOAPIC(1:2)and CPUCLK (1:4)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	22	-	31	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	37	-	56	mA	Vout = 1.25V
Pull-Down Current Min	IOL_{min}	30	-	41	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	75	-	102	mA	Vout = 1.2V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.6	nS	20 pF Load
Vdd = Vddq3 =3.3V ±5%, Vddq2 = 2.5V ±5%, TA = 0ºC to +70ºC						

TB40A TYPE BUFFER CHARACTERISTICS FOR REF and SDRAM(1:16)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	30	-	39	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	75	-	109	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	30	-	40	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	75	-	103	mA	Vout = 1.2V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	1.3	nS	30 pF Load
Vdd = Vddq3 =3.3V ±5%, Vddq2 = 2.5V ±5%,, TA = 0ºC to +70ºC						

Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

TB4L1 TYPE BUFFER CHARACTERISTICS FOR PCICLK(1:6, F)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	68	-	23	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	44	-	64	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	18	-	25	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	50	-	70	mA	Vout = 1.5V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	15 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
Vdd = Vddq3 =3.3V ±5%, Vddq2 = 2.5V ±5%,, TA = 0ºC to +70ºC						

CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerence	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallell Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	the crystals rated load. note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	crystals internal package capacitance (total)

For maximum accuracy,the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 18.0 pF

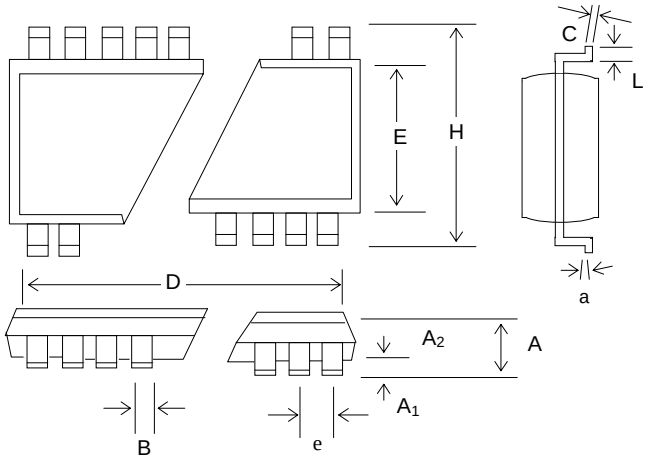
the total parasitic capacitance would therefore be = 20.0.0 pF.

Note 1: It is recommended but not manditory that a crystal meets these specifications.

Low EMI I²C Clock Generator for Pentium™ II, 440LX, 4DIMM Designs

Preliminary

PACKAGE DRAWING AND DIMENSIONS



56 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	.720	.725	.730	18.29	18.42	18.54
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG579BYB	56 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG579BYB
Date Code, Lot #

IMISG579BYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number

Purchase of I²C components of International Microcircuits, Inc. or one of its sublicensed Associated Companies conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.