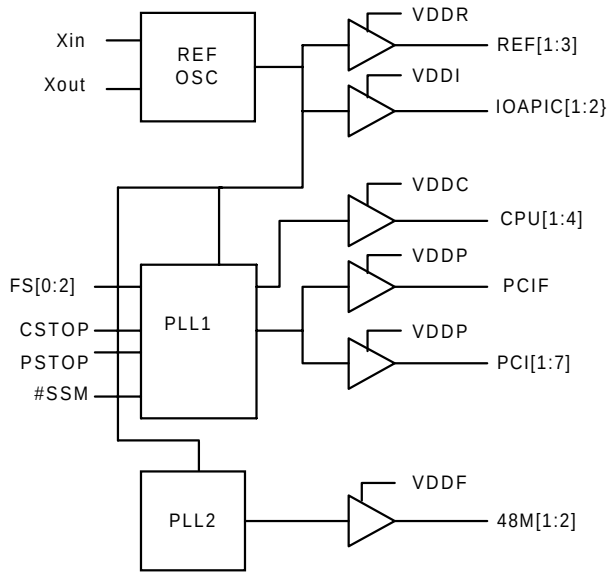
Low EMI Clock Generator for Pentium® II Systems with Power Management

Approved Product

PRODUCT FEATURES

- Supports Pentium®. Pentium® II & Pro CPUs.
- Designed to meet Intel chipset specification
- 4 CPU and 8 PCI clocks
- Two 48 MHz fixed clocks for USB and Super IO.
- Separate supply pins for mixed CPU, IOAPIC, and Fixed/PCI clocks
- < 175 ps Max. skew among CPU clocks.
- < 250 ps Max. skew among PCI clocks.
- Controlled current output buffers
- Power management feature
- 2 IOAPIC clocks for multiprocessor support.
- 48-pin SSOP package
- Spread Spectrum EMI reduction mode

BLOCK DIAGRAM

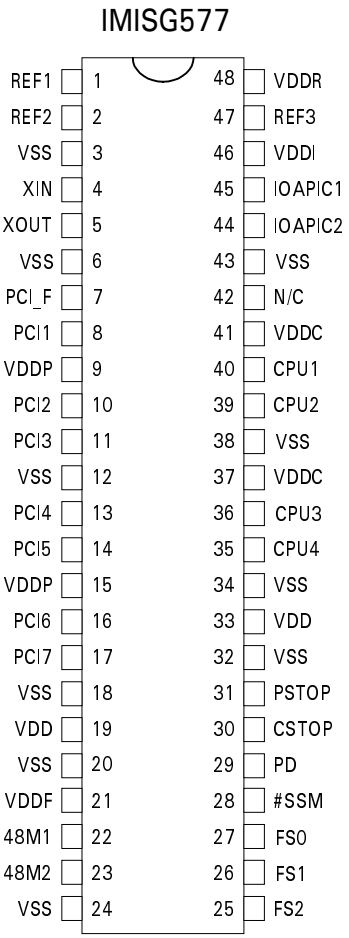


FREQUENCY TABLE

FS2	FS1	FS0	CPU	PCI
0	0	0	Tri-State	Tri-State
0	1	1	66 (66.58)*	33.3*
1	0	0	Ref/2	Ref/4
1	1	1	100 (99.7)**	33.2**

NOTE: *Down Spread 1.25% (total)
**Down Spread .5% (total)

CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
4	**Xin**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	VDD	O	OSC1	O-chip reference oscillator output pin. Drives an external parallel resonant crystal when an externally generated reference signal is used, is left unconnected
25, 26, 27	**FS(0:2)**	-	I	PAD PU	Frequency select input pins. See frequency select table on page 1. These pin has an internal pull-up
40, 39, 36, 35	**CPU(1:4)**	VDDC	O	BUF1	Clock outputs. CPU frequency table specified on page 1.
45, 44	**IOAPIC(1:2)**	VDDI	O	BUF2	IOAPIC clock for multi processor support. Fixed frequency at 14.31818 MHz. (2.5 or 3.3 supply = VDDI)
8, 10, 11, 13, 14, 16, 17	**PCI(1:7)**	VDDP	O	BUF4	PCI bus clocks. See frequency select table on page 1.
7	**PCI_F**	VDDP	O	BUF4	PCI clock that ceases only when PD (pin 29) is ascerted. See frequency select table on page 1.
3, 6, 12, 18, 20, 24, 32, 34, 38, 43	**VSS**	-	P	-	Ground pins for the device.
46	**VDDI**	-	P	-	3.3 or 2.5 Volt power supply pins for IOAPIC clock output buffers.
9, 15	**VDDP**	-	P	-	3.3 Volt power supply pins for PCI and PCI_F clock output buffers.
21	**VDDF**	-	P	-	3.3 Volt power supply pins for 48 MHz clock output buffers.
48	**VDDR**	-	P		3.3 Volt power supply pins for reference clock output buffers.
37, 41	**VDDC**	-	P	-	3.3 or 2.5 Volt power supply pins for CPU clock output buffers.
19, 33	**VDD**				Power supply pins for analog circuits and core logic
1, 2, 47	**REF(1:3)**	VDDR	O	BUF3	Buffered outputs of on-chip reference oscillator.
22, 23	**48M(1:2)**	VDDF	O	BUF3	Fixed 48 MHz frequency clock outputs.
31	**PSTOP**	-	I	PAD PU	When driven to a logic low level, this pin will synchronously stop all PCI clocks (except PCI_F) at a logic low level.
30	**CSTOP**	-	I	PAD PU	When driven to a logic low level, this pin will synchronously stop all CPU clocks at a logic low level.
28	**#SSM**	-	I	PAD PU	When driven to a logic low level this pin enables EMI reducing Spread Spectrum mode (affects only CPU and PCI clocks).
29	**PD**	-	I	PAD PU	When this pin is driven to a logic low the IC will enter shutdown mode and **ALL** internal circuitry is turned off.

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Descriptions	Outputs				
	CPU	PCI, PCIF	48 MHz	REF1:3	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2	TCLK/4	TCLK/2	TCLK	TCLK

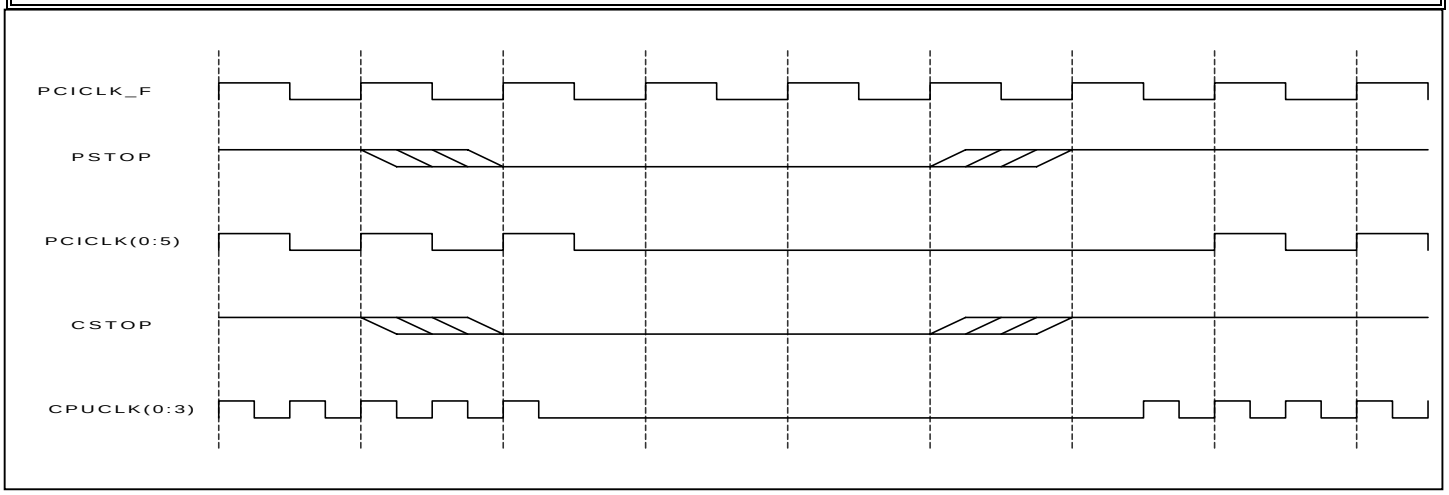
NOTE: TCLK is a test clock that is driven into the XTAL_IN input during test mode.

POWER MANAGEMENT FUNCTIONS

All PCI (excluding PCI_F) and CPU clocks can be enabled or stopped via the PSTOP and CSTOP input pins. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped and on transitions from stopped to running when the chip was not powered down. On power up, (after bring PD from a low to high state) the VCOs will stabilize to the correct pulse widths within about 0.2 mS. The CPU, and PCI clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CSTOP	PSTOP	PD	CPUCLK	PCICLK	OTHER CLKs	XTAL & VCOs
X	X	0	LOW	LOW	LOW	OFF
0	0	1	LOW	LOW	RUNNING	RUNNING
0	1	1	LOW	RUNNING	RUNNING	RUNNING
1	0	1	RUNNING	LOW	RUNNING	RUNNING
1	1	1	RUNNING	RUNNING	RUNNING	RUNNING

POWER MANAGEMENT TIMING



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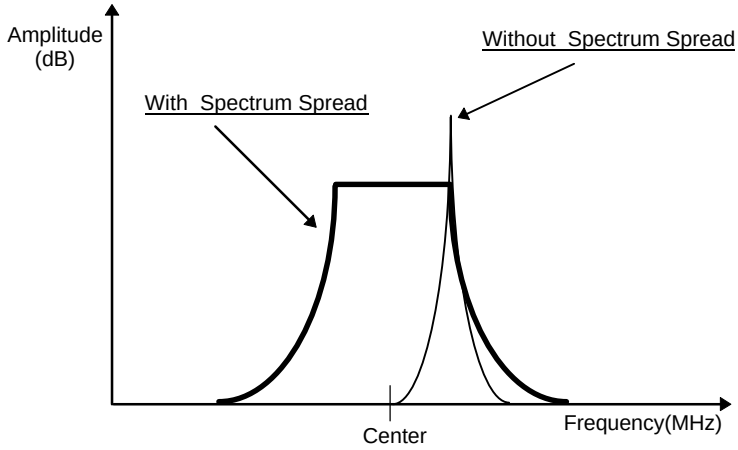
Power Management Timing		
Signal	**Signal State**	**Latency**
		No. of rising edges of free running PCICLK (PCIF)
CSTOP	0 (disabled)	1
	1 (enabled)	1
PSTOP	0 (disabled)	1
	1 (enabled)	1
PD	1 (normal operation)	3 mS
	0 (power down)	2 mS max.

NOTES:
1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high) to when the first valid clocks are driven from the device.

SPECTRUM SPREAD CLOCKING

Down Spread



Spectrum Analysis

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SPECTRUM SPREADING SELECTION TABLE					
Min (MHz)	Center (MHz)	Max (MHz)	CPU Frequency	% OF FREQUENCY SPREADING	MODE
99.50	99.75	99.7	100	.5% (-.5% + 0%)	Down Spread
65.4	66.4	67.39	66	1.25% (-1.25% + 0%)	Down Spread

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL	-66		-	µA	
Input High Current	IIH			5	µA	
Output Low Voltage IOL = 4mA	VOL	-	-	0.4	Vdc	All Outputs (see buffer spec)
Output High Voltage IOH = 4mA	VOH	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	275	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	75	mA	-
Crystal Oscillator Capacitance	Cx	-	18	-	pF	Xin and Xout crystal load capacitance values (each)
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%,, TA = 0ºC to +70ºC

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SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1.5	-	4	ns	CPU load = 20 pF, PCI load = 30 pF measured at 1.5V PCI and 1.25V CPU
Buffer out Skew All CPU Buffer Outputs	$tSKEW_1$	-	-	175	ps	20 pF Load Measured at 1.5V
Buffer out Skew All PCI Buffer Outputs	$tSKEW_2$	-	-	250	ps	30 pF Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI = 2.5V ±5%, TA = 0ºC to +70ºC						

TB40_V BUFFER CHARACTERISTICS FOR CPUCLK(1:4)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	22	-	31	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	37	-	56	mA	Vout = 1.25V
Pull-Down Current Min	IOL_{min}	30	-	41	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	75	-	102	mA	Vout = 1.20V
Dynamic Output Impedence	Z_o	10	-	15	Ohms	66 and 100 MHz
Rise/Fall Time Min/Max Between 0.4 V and 2.0 V	TRF	0.4	-	1.6	ns	20 pF Load
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%,, TA = 0ºC to +70ºC						

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TB40_V BUFFER CHARACTERISTICS FOR IOAPIC (1:2)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	22	-	31	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	37	-	56	mA	Vout = 1.25V
Pull-Down Current Min	IOL_{min}	30	-	41	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	75	-	102	mA	Vout = 1.2V
Rise/Fall Time Min/Max Between 0.4 V and 2.0 V	TRF_{max}	0.4	-	1.6	nS	20 pF Load
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%,, TA = 0ºC to +70ºC						

TB5 BUFFER CHARACTERISTICS FOR REF(1:3) and 48(1:2) MHz						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	13	-	17	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	30	-	44	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	13	-	19	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	32	-	44	mA	Vout = 1.5V
Dynamic Output Impedence	Z_o	18	-	25	Ohms	66 and 100 MHz
Rise/Fall Time Min/Max Between 0.4 V and 2.4 V	TRF	0.5	-	2.0	ns	20 pF Load
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%,, TA = 0ºC to +70ºC						

TB4 BUFFER CHARACTERISTICS FOR PCICLK(1:8,F)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	18	-	23	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	44	-	64	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	18	-	25	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	50	-	70	mA	Vout = 1.5V
Dynamic Output Impedence	Z_o	14	-	20	Ohms	66 and 100 MHz
Rise/Fall Time Min/Max Between 0.4 V and 2.4 V	TRF	0.5	-	2.0	ns	30 pF Load
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI =2.5V ±5%,, TA = 0ºC to +70ºC						

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CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerence	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallell Resonant
Pin Capacitance	CP		5		pF	Capacitance of XIN and Xout pins
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	7	pF	
X1 and X2 Load	CL		17		pF	internal crystal loading gapacitors on each pin (to ground)

For maximum accuracy,the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 18.0 pF

the total parasitic capacitance would therefore be = 20.0 pF.(matching CL)

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

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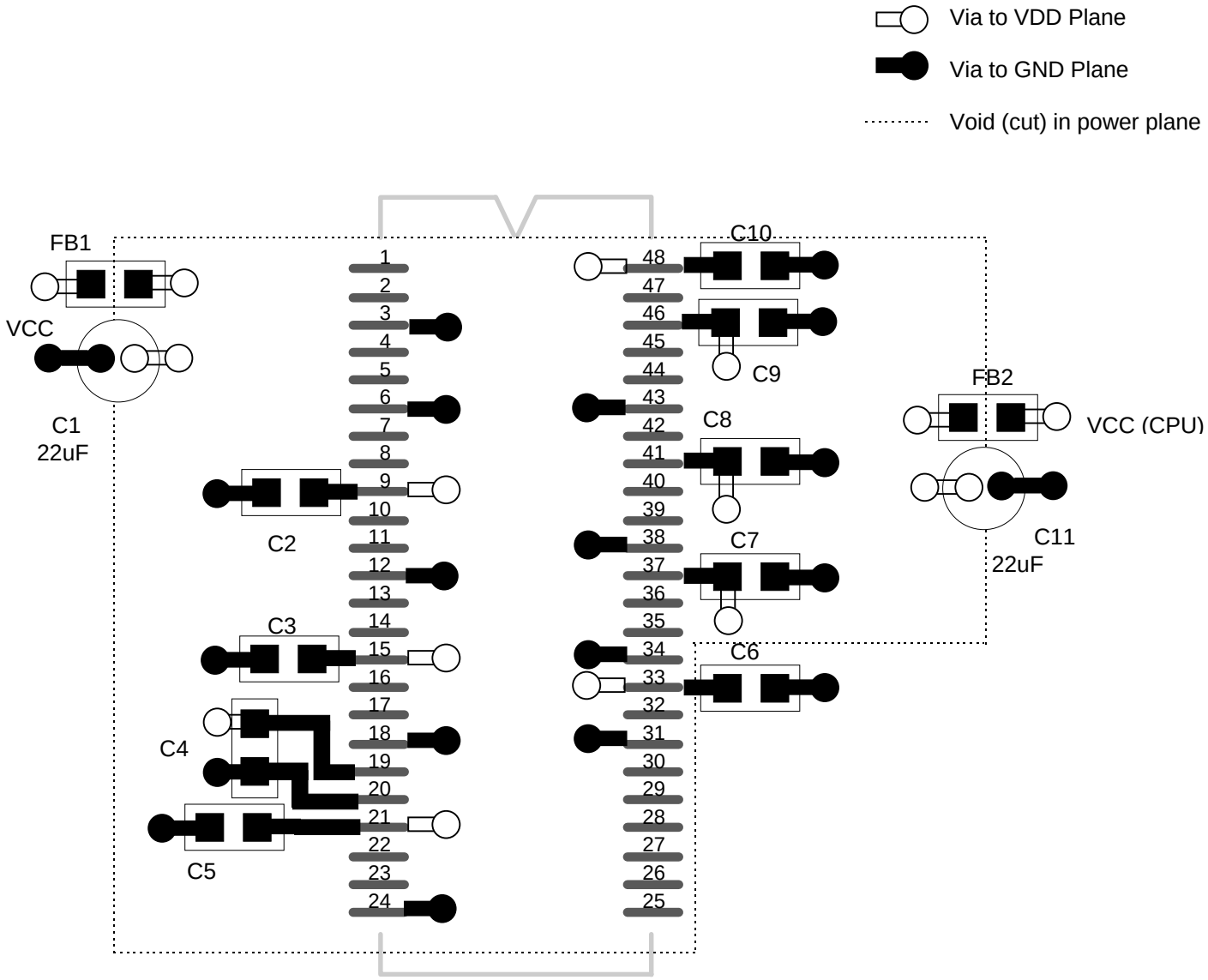
PCB LAYOUT SUGGESTION



This is only a layout recommendation for best performance and lower EMI. the designer may choose a different approach but C2, C3, C4, C5, C6, C7, C8, C9, and C10 (all are 0.1 uf) should always be used and placed as close to their VDD pins as is physically possible. The topological hookup of C4 with respect to its power and ground vias is especially important.

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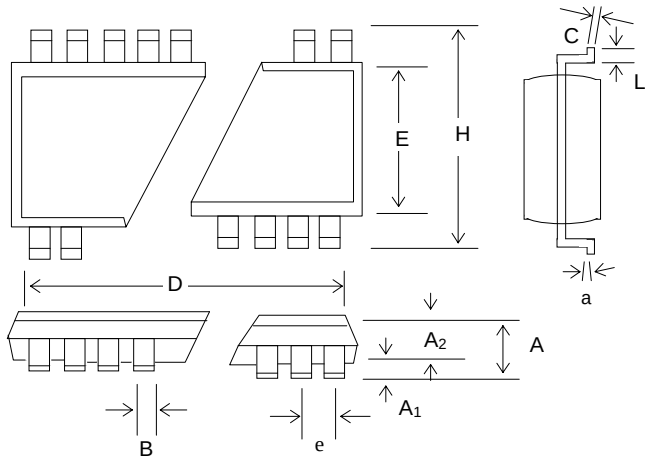
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
c	0.005	.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.637	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.0256 BSC			0.640 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.024	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG577CYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG577CYB
Date Code, Lot #

IMISG577CYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number