Low EMI Clock Generator for Multi-Function Products

Approved Product

PRODUCT FEATURES

- Supports clocking requirements for Multi-Function Products supporting Printers, Copiers, Scanners, Fax/modem integration.
- Programmable CPU clock output.
- Operates from 3.3V or 5V supply
- 60 mA buffer switching current
- 16 Pin SOIC for minimum board space
- **Integrates a Spectrum Spread technology for EMI attenuation of up to 15dB at harmonic frequencies.**

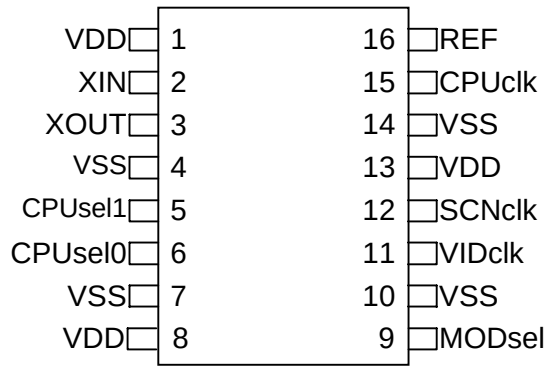
The IMISG536 is a clock generator that integrates clocking requirements for Multi-Function Products or stand alone products such as Printers, Copiers, and Scanners. In addition, it integrates a Spectrum Spread technology , a modulation technique designed specifically for reducing EMI at the fundamental frequency and at its harmonics. The EMI attenuation is proportional to the frequency, therefore achieving greater reduction at the harmonics where it is more difficult to pass federal regulations for radiated emissions (such as FCC, CSPIR, etc.).

The IMISG536 operates from a 20 MHz crystal oscillator across pins 2 and 3, or from an external clock source. The REF output is a buffered output of the input signal at XIN. CPUclk is the modulated output for EMI attenuation. This clock has optional frequency outputs which can be selected with CPUsel(0:1).

VIDclk (60 MHz) and SCNclk(40 MHz) are highly accurate fixed frequencies and therefore are not modulated.

This device is packaged in a 16 pin SOIC package for minimum occupation of board space.

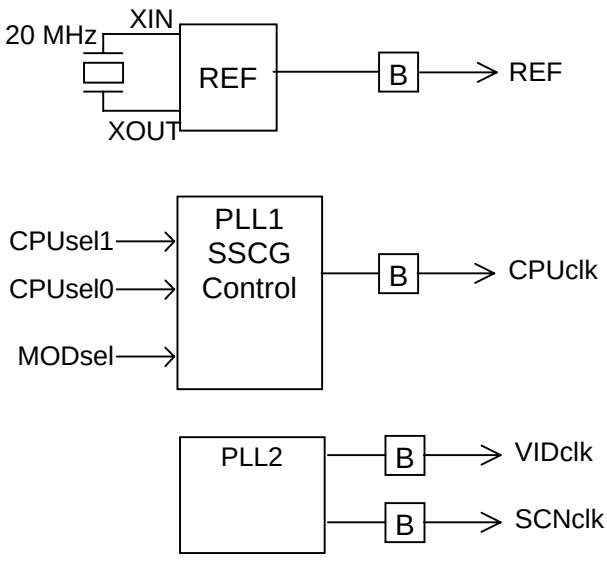
CONNECTION DIAGRAM



CPUclk SELECTION TABLE

CPUsel1	CPUsel0	CPUclk (MHz)
0	0	16
0	1	33
1	0	25
1	1	50

BLOCK DIAGRAM



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PIN DESCRIPTION

OSCin, OSCout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. OSCin may also serve as an input for an externally generated CMOS level or AC coupled reference signal.

CPUsel(0:1) - Input controls pins used to select the clock frequency of the CPUclk output. See table page 1. These pins have internal pull-ups.

MODsel - This pin is used to control the Spectrum Spread enable/disable. When Low, Spectrum Spread is not applied to the CPUclk output. When High (default), this pin enables the CPUclk to be modulated at +/-1.25 % of its center frequency as described in figure 2, Page 4 and reduces EMI as described in figure 1. It has an internal pull-up.

CPUclk - SSCG modulated clock output for system CPU. Frequency may be selected based on the table on page 1.

SCNclk - Non-modulated clock output for system scanner processing. It is centered exactly at 40.00000 MHz.

VIDclk - Non-modulated clock output for system engine logic. It is centered exactly at 60.00000 MHz.

VDD - Circuit positive power supply.

VSS - Circuit ground.

A bypass capacitor (0.1µF) should be placed as close as possible to each VDD pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be canceled by the lead inductances of the traces.

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	-55ºC to +125ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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ELECTRICAL CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL	-	-	0.8	Vdc	CPUsel (0:1), MODsel
Input High Voltage	VIH	2.0	-	-	Vdc	CPUsel (0:1), MODsel
Input Low, or High Current with Pull- up or Pull-down	IIL, IIH	-	-	66	µA	CPUsel (0:1), MODsel
Output Low Voltage IOL = 12mA	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH = 12mA	VOH	2.4	-	-	Vdc	All Outputs
Dynamic Supply Current	Icc	-	-	40	mA	CPUclk = 50 MHz
Static Supply Current	Icc (PD)	-	200	-	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
						VDD = 5 V, TA = 0ºC to +70ºC

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Rise (0.4V - 2.0V) and Fall (2.0V-0.4V) time	tTLH, tTHL	-	-	2	ns	15 pf Load
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
ΔPeriod Adjacent Cycles CPU	ΔP	-	-	±250	ps	-
Jitter Absolute CPU	tjab	-		500	ps	MODsel = 0
Switching Current Low*	IOL(AC)	-	60	-	mA	VOL = 1.5V
Switching Current High*	IOH(AC)	-	60	-	mA	VOL = 1.5V
						VDD = 5 V, TA = 0ºC to +70ºC

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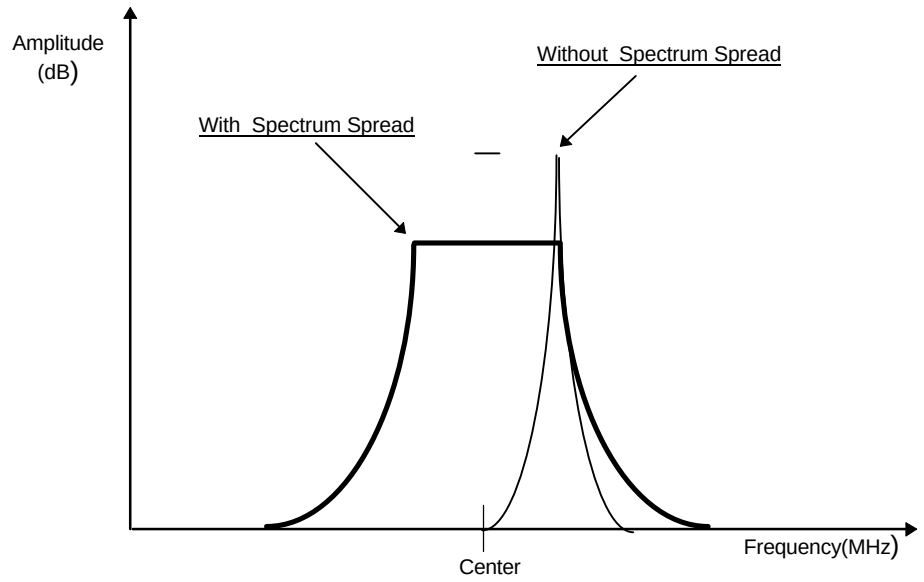
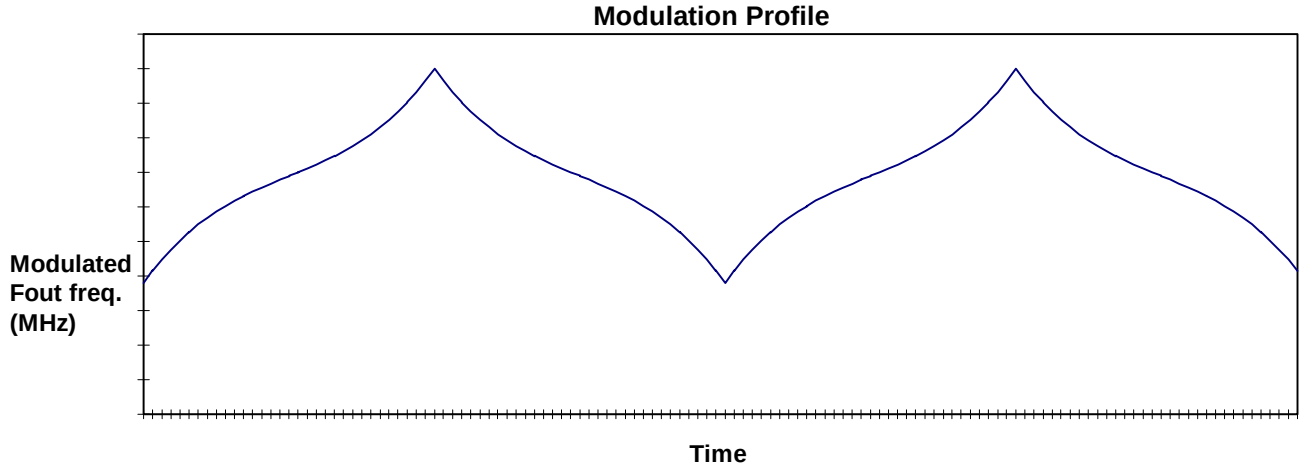
SPECTRUM SPREAD



Spectrum Analysis

Modulation Domain Analysis



Note : The modulation rate, *fr*, is dependent on the Input frequency (Xin).

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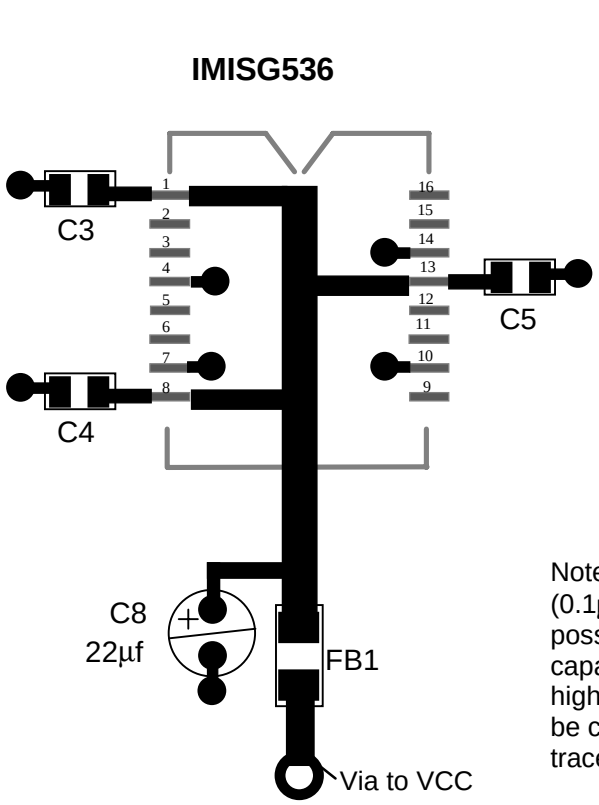
PCB LAYOUT SUGGESTION



Note: Bypass capacitors C3, C4, and C5, (0.1µf) should be placed as close as possible to each VDD pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be canceled by the lead inductances of the traces.

NOTES

1. POWER SUPPLY BYPASS CAPS (O.1UF) MUST BE POSITIONED CLOSE TO VDD PINS TO BE EFFECTIVE.

2. C3, C4, C5, C and C8 CAPS MUST BE LOW LEAKAGE SUCH AS MULTILAYER CERAMIC Z5U OR X7R MATERIAL.

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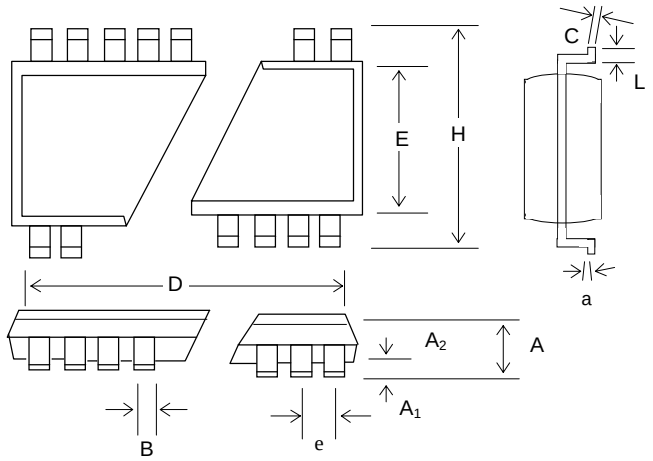
PACKAGE DRAWING AND DIMENSIONS



16 PIN SOIC OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A_1	0.0020	0.009	0.0015	0.060	0.22	0.38
A2	0.090	0.092	0.111	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.0091	0.010	0.0125	0.23	0.25	0.32
D	.399	.407	.412	10.13	10.34	10.46
E	0.285	0.296	0.299	7.24	7.52	7.59
e	0.050 BSC			1.27 BSC		
H	0.400	0.406	0.40	10.16	10.31	10.41
a	0°	5°	10°	0°	5°	10°
L	0.24	0.032	0.040	0.61	0.81	1.02

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG536AXB	16 PIN SOIC	Commercial, 0ºC to + 70ºC

Marking: Example: IMI
SM536AXB
Date Code, Lot#

IMISM536AXB

Flow
B = Commercial, 0°C to + 70°C

Package
X = SOIC

Revisions

IMI Device Number