I²C Clock Generator for Pentium™ II, 440LX, 3DIMM Designs

Preliminary

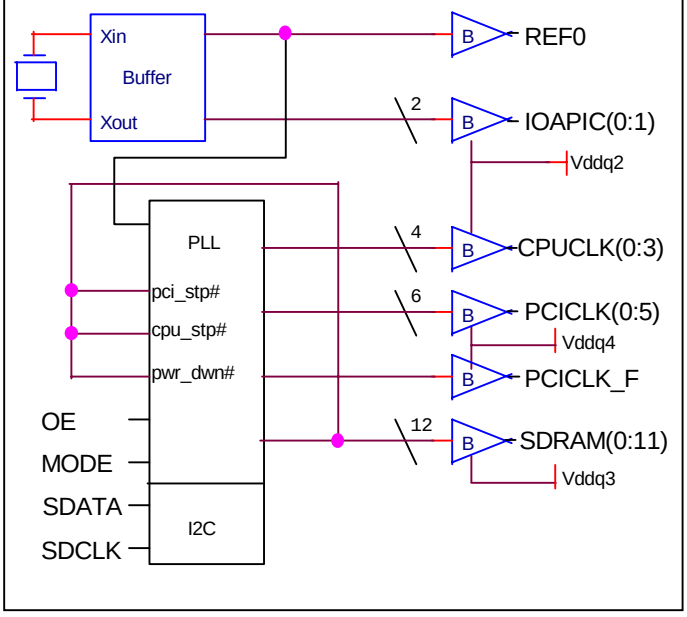
PRODUCT FEATURES

- Supports Pentium™ and Pentium™ II CPU's.
- Supports 440LX chipset.
- Designed to Intel chipset Specification
- 4 CPU / AGP clocks.
- 12 SDRAM clocks for 3 DIMMs.
- 7 PCI synchronous clocks.
- Optional common or mixed supply mode:
- (Vdd = Vddq3 = Vddq2= 3.3V) or
- (Vdd = Vddq3 = 3.3V, Vddq2 = 2.5V)
- Supports Power Management function
- < 250ps skew CPU and SDRAM clocks.
- < 250ps skew among PCI clocks.
- I²C 2-Wire serial interface
- Programmable registers featuring:
  - enable/disable each output pin
  - mode as tri-state, test, or normal
- 2 IOAPIC clocks for multiprocessor support.
- 48-pin SSOP package

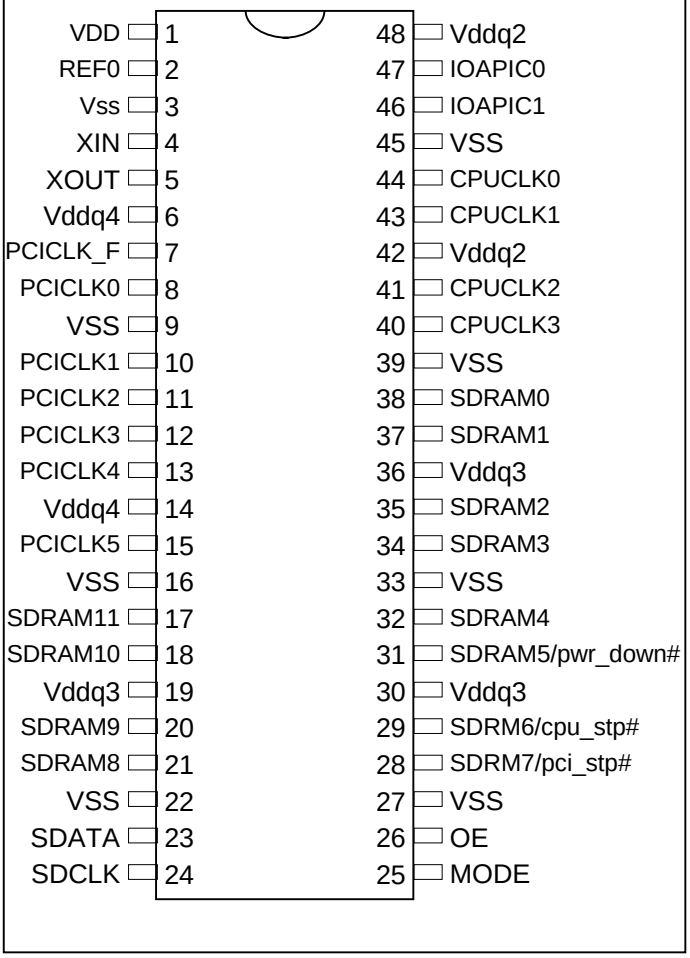
FREQUENCY TABLE

OE	CPU*/SDRAM*	PCI
0	All output clocks tristated	
1	66.44	33.22

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
4	**Xin**	Vdd	I	OSC1	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	Vdd	O	OSC1	On-chip reference oscillator output pin. Drives an external parallel resonant crystal when an externally generated reference signal is used, is left unconnected
26	**OE**	Vddq3	I	PADI4 PU	Output Enable. When at a logic 0 (LOW) all output are tristated (Hi-Z) and all internal circuitry running. It has an internal pull-up
2	**REF**	Vdd	O	BUF	Buffered output of on-chip reference oscillator.
44, 43, 41, 40	**CPUCLK(0:3)**	Vddq2	O	BUF	Clock outputs. CPU frequency table specified.
24	**SDCLK**	Vddq3	I/O	PADI4 PU	serial clock of I²C 2-wire control interface. Has internal pull-up resistor.
23	**SDATA**	Vddq3	I/O	PADI4 PU	serial data of I²C 2-wire control interface. Has internal pull-up resistor.
8, 10, 11, 12, 13, 15	**PCICLK(0:5), F**	Vddq3	O	BUF	A PCI clock outputs. See frequency select table on page 1.
7	**PCICLK_F**	Vddq3	O	BUF	PCI clock output that does not stop until in power down mode. It is synchronous with other PCI clocks.
47, 46	**IOAPIC(0:1)**	Vddq2	O	BUF	Two Buffered outputs of 14.3MHZ for multiprocessor support. They are powered by Vddq3
38, 37, 35. 34. 32, 21, 20, 18, 17	**SDRAM (0:4) (8:11)**	Vddq3	O	BUF	If MODE=1, this pin is a Synchronous DRAM DIMs clock output powered by Vddq3. If MODE=0, this pin is a PS# input signal, where a low level stops the PCI clocks. It has an internal pull-up.
31	**SDRAM5/ pwr_dwn#**	Vddq3	I/O	BUF PU	If MODE=1, this pin is a Synchronous DRAM DIMs clock output powered by Vddq3. If MODE=0 this pin is a PD# input signal. Where a low level (Logic 0) all outputs and internal logic has Power Removed
29	**SDRAM6/ cpu_stp#**	Vddq3	I/O	BUF PU	If MODE=1, this pin is a Synchronous DRAM DIMs clock output powered by Vddq3. If MODE=0, this pin is a CS# input signal, where a low level stops the CPU (the SDRAM clocks will stay active) . It has an internal pull-up
28	**SDRAM7/ pci_stp#**	Vddq3	I/O	BUF PU	If MODE=1, this pin is a Synchronous DRAM DIMs clock output powered by Vddq3. If MODE=0, this pin is a PS# input signal, where a low level stops the PCI clocks. It has an internal pull-up.
25	**MODE**	Vddq3	I	PAD PU	This pin controls the functionality of pins 28, 29 and 31 and enables Tristate mode. See Frequency Table on page 1 for functionality discription. It has an internal pull-up.
3, 9, 16, 22, 27, 33, 39, 45	**VSS**	-	P	-	Ground pins for all power supplies,
1	**VDD**	-	P	-	Power supply pins for fixed clocks and core logic
42, 48	**Vddq2**	-	P	-	Power supply pins for 2.5V/3.3V CPU and IOAPIC clock pins.
36, 30, 19	**Vddq3**		P	-	Power supply pins for 3.3V SDRAM clock clock pins.
6,14	**Vddq4**	-	P	-	Power supply pin for 3.3V PCI clock ouput pin.

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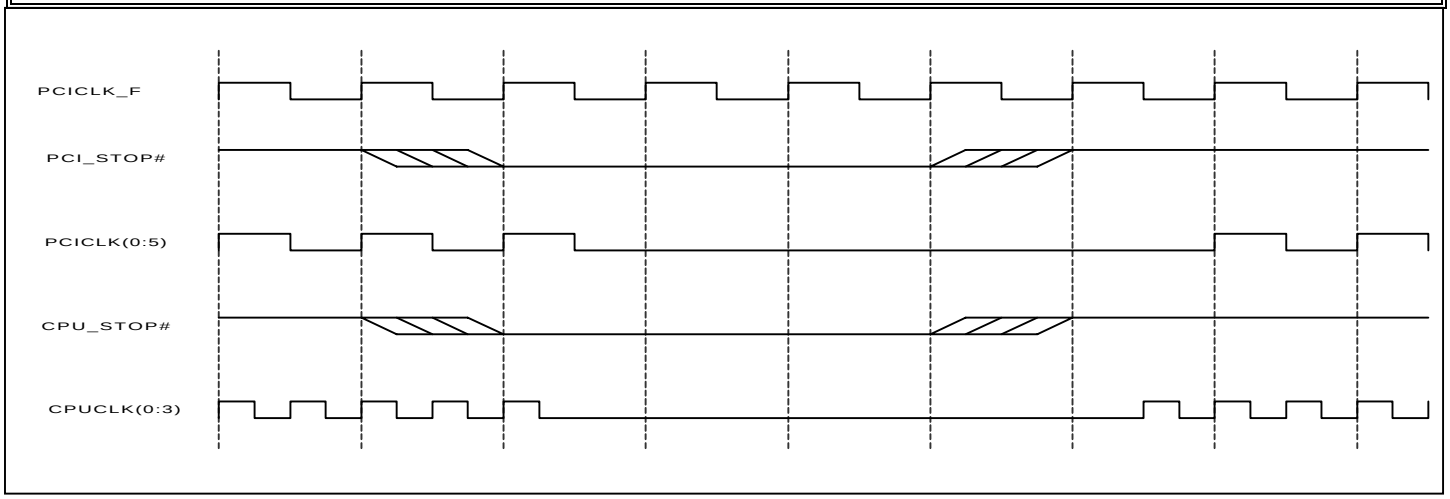
POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or stopped via the 2-wire control interface. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped and on transitions from stopped to running when the chip was not powered down. On power up, the VCOs will stabilize to the correct pulse widths within about 0.2 mS. The CPU, and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

When MODE=0 and SEL=1, pins 28, 29 and 31 are inputs pci_stp#; cpu_stp# and pwr_dwn# respectively (when MODE=1, these functions are not available). A particular output is enabled only when both the serial interface and these pins indicate that it should be enabled. The device clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. On low to high transitions of PWR_DWN#, external circuitry should allow 0.2 mS for the VCOs to stabilize prior to assuming the clock periods are correct. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	OTHER CLKs	XTAL & VCOs
X	X	0	LOW	LOW	LOW	OFF
0	0	1	LOW	LOW	RUNNING	RUNNING
0	1	1	LOW	33 MHZ	RUNNING	RUNNING
1	0	1	66 MHZ	LOW	RUNNING	RUNNING
1	1	1	66 MHZ	33 MHZ	RUNNING	RUNNING

POWER MANAGEMENT TIMING



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2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The IMISC676 cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.
During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The IMISC676 will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The IMISC676 will not respond to any other control interface conditions. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

Byte 0: Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	0	-	Reserved Do Not Set
5	0	-	Reserved Do Not Set
4	0	-	Reserved Do Not Set
3	1	-	Reserved
2	1	-	Reserved
1 0	0 0		Bit1 Bit0 1 1 Tri-State 1 0 Reserved for Test 0 1 Test Mode 0 0 Normal

IMPORTANT NOTE

Reserved bits are intended for possible future functions. It is important that they be left at their Power Up logic levels at all times. Otherwise data sheet specifications cannot be guaranteed.

Note: the OE pin26 is logically or'ed with the Byte 0 bit 0=1 and bit 1=1 Tri-State function. It does not set, reset or cause these bits to change.

SERIAL CONTROL REGISTERS (Cont.)

Function Table

Function Description	Outputs				
	CPU	PCI	SDRAM	Ref	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	Tclk/2	Tclk/4	Tclk/2	Tclk	Tclk
Normal Mode	66	CPU/2	CPU	14.318	14.318

Notes:
1. Tclk is a test clock over driven on the Xin input during test mode.

Byte 1: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	1	40	CPUCLK3 enable/Stopped
2	1	41	CPUCLK2 enable/Stopped
1	1	43	CPUCLK1 enable/Stopped
0	1	44	CPUCLK0 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	7	PCICLK_F enable/Stopped
5	1	15	PCICLK5 enable/Stopped
4	1	14	PCICLK4 enable/Stopped
3	1	12	PCICLK3 enable/Stopped
2	1	11	PCICLK2 enable/Stopped
1	1	10	PCICLK1 enable/Stopped
0	1	8	PCICLK0 enable/Stopped

SERIAL CONTROL REGISTERS(Cont.)

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1*	28	SDRAM7 enable/Stopped
6	1*	29	SDRAM6 enable/Stopped
5	1*	31	SDRAM5 enable/Stopped
4	1	32	SDRAM4 enable/Stopped
3	1	34	SDRAM3 enable/Stopped
2	1	35	SDRAM2 enable/Stopped
1	1	37	SDRAM1 enable/Stopped
0	1	38	SDRAM0 enable/Stopped

***This bit acts as a don't care bit when the MODE pin is 0 (logic low) (input mode)**

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	1	17	SDRAM11 enable/Stopped
2	1	18	SDRAM10 enable/Stopped
1	1	20	SDRAM9 enable/Stopped
0	1	21	SDRAM8 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	1	46	IOAPIC1 enable/Stopped
4	1	47	IOAPIC0 enable/Stopped
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	1	2	REF0 enable/Stopped

SERIAL CONTROL REGISTERS(Cont.)

Byte 6: Reserved Register

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to + 70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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ELECTRICAL CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	90	mA	CPU = 66.6 MHz, PCI = 33.3 Mhz fully loaded
Static Supply Current	Isdd	-	-	150	µA	Power down mode
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%, TA = 0ºC to +70ºC						

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	20 pf Load on CPU, 30 pF load on PCI, Measured at 1.25 V CPU to 1.5 V PCI, *note 1*
Skew (CPU-CPU,SDRAM-SDRAM,PCI-PCI)	tSKEW1	-	-	250	ps	20 pf Load on CPU, 30 pF load on PCI, Measured at 1.25 V CPU to 1.5 V PCI
Skew (CPU-SDRAM)	tSKEW2	-	-	500	ps	20 pf CPU, 30 pF SDRAM load, *note1*
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5% (unless noted), TA = 0ºC to +70ºC						

note 1: CPU clocks are measured at 1.25 Volts. SDRAM and PCI clocks are measured at 1.5Volts.

TYPE 1 BUFFER CHARACTERISTICS FOR CPUCLK(1:4)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-27	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	27	mA	Vout = 2.6 V
Pull-Down Current Min	IOL_{min}	-27	-	-	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.6	nS	20 pF Load
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%, TA = 0ºC to +70ºC						

TYPE 2 BUFFER CHARACTERISTICS FOR IOAPIC(1:2)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-28	-	-	mA	Vout = 1.4 V
Pull-Up Current Max	IOH_{max}	-	-	28	mA	Vout = 2.7 V
Pull-Down Current Min	IOL_{min}	-28	-	-	mA	Vout = 1.0 V
Pull-Down Current Max	IOL_{max}	-	-	28	mA	Vout = 0.2 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.6	nS	20 pF Load
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%, TA = 0ºC to +70ºC						

TYPE 4 BUFFER CHARACTERISTICS FOR REF and SDRAM(1:12)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-46	-	-	mA	Vout = 1.65 V
Pull-Up Current Max	IOH_{max}	-	-	46	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	-53	-	-	mA	Vout = 1.65 V
Pull-Down Current Max	IOL_{max}	-	-	53	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	30 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	1.3	nS	30 pF Load
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%, TA = 0ºC to +70ºC						

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TYPE 5 BUFFER CHARACTERISTICS FOR PCICLK(1:6,F)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-33	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-33	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	30	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	38	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	30 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%, TA = 0ºC to +70ºC						

CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerence	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallell Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	the crystals rated load. note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	crystals internal package capacitance (total)

For maximum accuracy,the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 18.0 pF

the total parasitic capacitance would therefore be = 20.0.0 pF.

Note 1: It is recommended but not manditory that a crystal meets these specifications.

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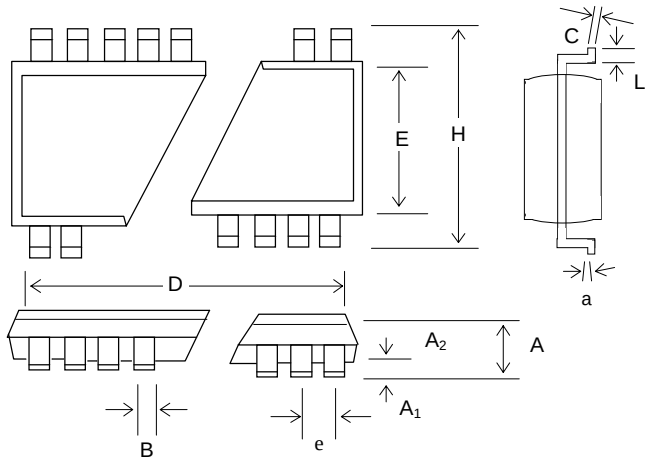
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0º	5º	8º	0º	5º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC676EYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC676EYB
Date Code, Lot #

IMISC676EYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number

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