Audio and Peripheral Clock Generator

Approved Product

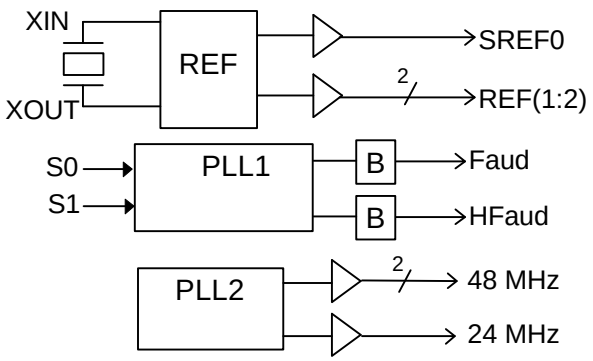
PRODUCT FEATURES

- Supports Intel architecture based desktop for complimenting the IMI SC673 and SC674 in the 430 TX, and the next generation chipsets from Intel.
- 2 USB clocks and 1 SIO clock.
- Selectable audio clocks.
- Supports 5V or 3.3V.
- 20 Pin SSOP for minimum board space.

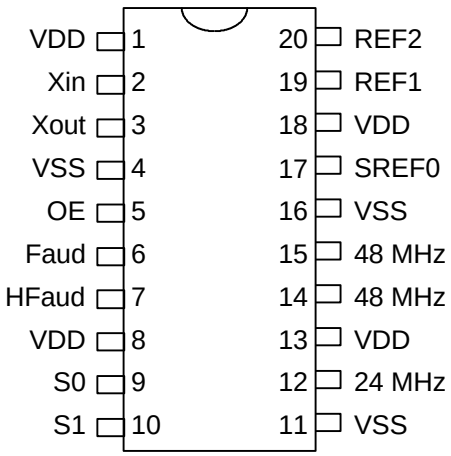
FREQUENCY TABLE

Select		Audio Frequency Outputs(MHz)		Fixed Frequency Outputs(MHz)		
S1	S0	Faud	HFaud	SREF0 REF1,2	48	24
0	0	Xin/2	Xin/4	Xin	Xin/ 2	Xin/ 4
0	1	24.576	12.288	14.318	48	24
1	0	33.868	16.934	14.318	48	24
1	1	LOW	LOW	14.318	48	24

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

Xin, Xout - On-chip reference oscillator buffer. These pins are connected to the terminals of a parallel (or anti-) resonant crystal. Xin may also be used as input for an externally generated signal; in this case Xout must be left unconnected (floating.)

OE - Output Enable input. When OE is low (0), all outputs are tristated. When OE is high (1, default) all outputs are toggling. This pin has an internal pull-up.
Faud - Audio frequency output. Selectable with S0 and S1, see table page 1.

HFaud - Audio frequency output. This output is a divide by 2 of the frequency selected at Faud.

S1, S0 - Input select lines for programming the audio (Faud and HFaud) output frequency. See table, page 1 for frequency selection. These pins have internal pull-ups.

48 MHz - USB clock output. The center frequency of this clock is within the USB spec. of +/- 0.167 % accuracy.

24 MHz - SIO clock output. The center frequency of this clock is within +/- 0.167 % accuracy.

REF(1:2) - These are buffered outputs of the Xin reference input signal.
SREF0 - This is a buffered output of the Xin reference input signal.

VSS - Circuit ground.

VDD - Power supply.

A 0.1µF capacitor must be placed as close as possible to each VDD pin. Otherwise the filtering intent of the cap will be neutralized by the trace lead inductance.

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD	0.3V
Storage Temperature:	-65ºC to 150ºC
Ambient Temperature:	-55ºC to +125ºC
Maximum Operating Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to its circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS <(Vin, Vout)< VDD

Unused inputs must always be tied to an appropriate logic voltage level (either Vss or VDD).

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL}	-	-	0.8	Vdc	S1, S0, OE
Input High Voltage	V_{IH}	2.0	-	-	Vdc	
Current on Pull-Up	I_{IL}, I_{IH}			5	µA	
Output Low Voltage	V_{OL}	-	-	0.4	Vdc	IOL = 12mA
Output High Voltage	V_{OH}	2.4	-	-	Vdc	IOH = 12mA
Tri-State leakage Current	I_{OZ}	-	-	10	µA	
Dynamic Supply Current	I_{DD}	-	-	28	mA	Faud = 33.868 MHz
Static Supply Current	I_{DD}	-	-	15	mA	
Short Circuit Current	I_{OS}	25	-	-	mA	1 output at a time - max 30 sec.

VDD = 3.3V ± 10%. TA = 0ºC to 70ºC

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.4V - 2.0V)	tTLH,	-	-	1.5	nS	20 pF load. ALL OUTPUTS
and Fall (2.0V-0.4V) time	tTHL	-	-	1.5	nS	20 pF load. ALL OUTPUTS
Output duty cycle		45	50	55	%	Measured at 1.5V
Cycle to cycle ΔPeriod	ΔP	-	-	± 250	pS	Measured at 1.5V on CPU*
Jitter Absolute	tjab	-	-	500	pS	Measured at 1.5V on CPU*
Switching current (AC)	I_{ol}, I_{oh}	-	90	-	mA	48 MHZ, 24 MHZ, REF(1:2), Faud, HFaud
Switching current (AC)	I_{ol}, I_{oh}	-	120	-	mA	SREF0

VDD = 3.3V ± 10%. TA = 0ºC to 70ºC

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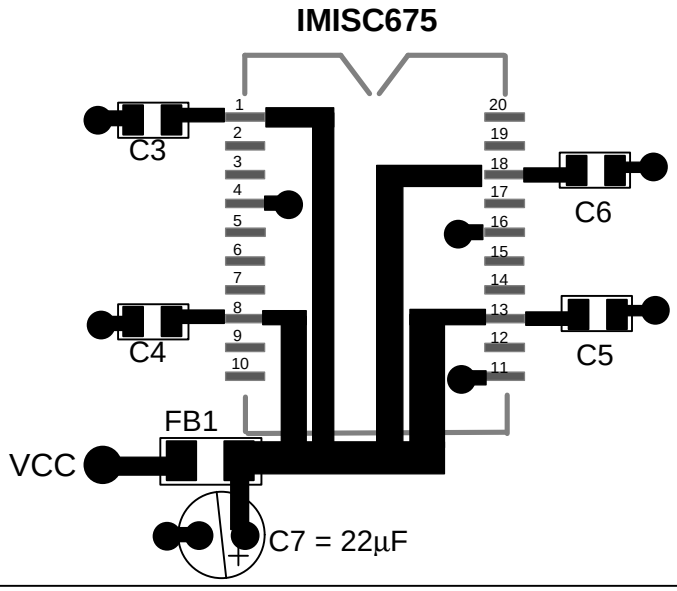
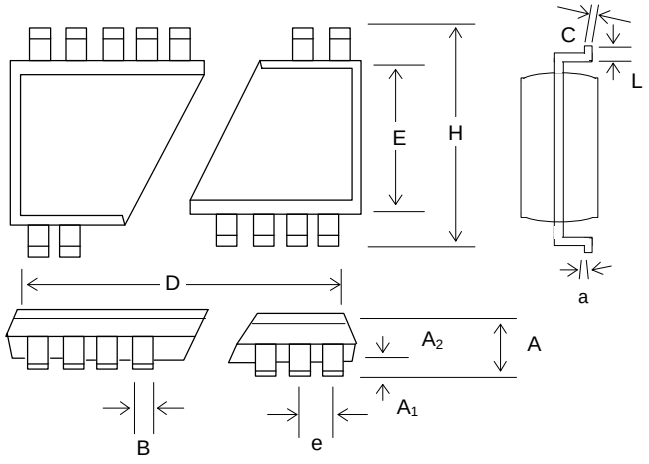
PCB LAYOUT RECOMMENDATION



Via to GND plane

This is only a layout recommendation. The designer may choose a different approach such as using VDD islands instead of traces. Regardless of the layout implementation, Bypass caps : C3, C4, C5, and C6 (all 0.1µF) should always be used and placed as close to their VDD pins as possible. Caps should be multilayer low impedance at high frequencies such as Z5U material.

PACKAGE DRAWINGS AND DIMENSIONS



20 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A_2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.278	0.284	0.289	7.07	7.20	7.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC675AYB	20 Pin SSOP	Commercial, 0° C to + 70° C