I²C Clock Generator for Pentium™ and Pentium™ II with 440LX Chipset and 4 DIMMs

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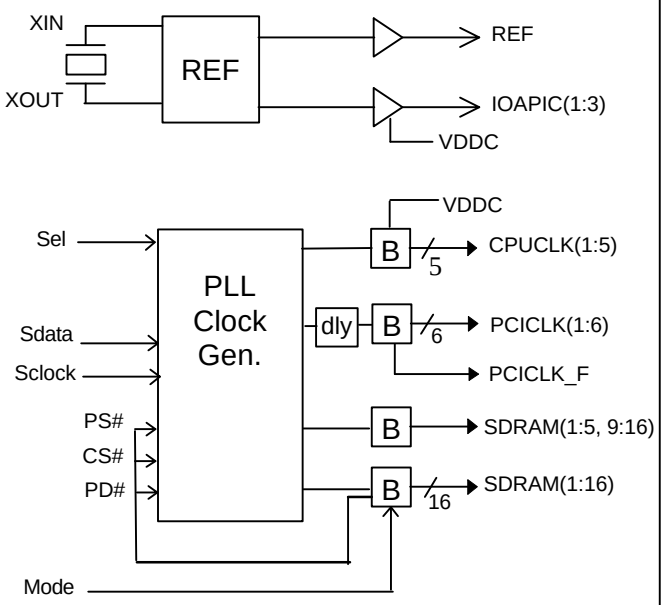
PRODUCT FEATURES

- Supports Pentium™ & Pentium™ II using the 440LX chipset..
- 5 CPU / AGP clocks
- Up to 16 SDRAM clocks for 4 DIMMs.
- 7 PCI synchronous clocks.
- Optional common or mixed supply mode:
- (VDD = VDDP = VDDC = 3.3V) or
- (VDD = VDDP = 3.3V, VDDC = 2.5V)
- Supports Power Management
- < 250ps skew CPU and SDRAM clocks.
- < 250ps skew among PCI clocks.
- I²C 2-Wire serial interface
- Programmable registers featuring:
  - enable/disable each output pin
  - mode as tri-state, test, or normal
- 3 IOAPIC clocks for multiprocessor support.
- 56-pin SSOP package

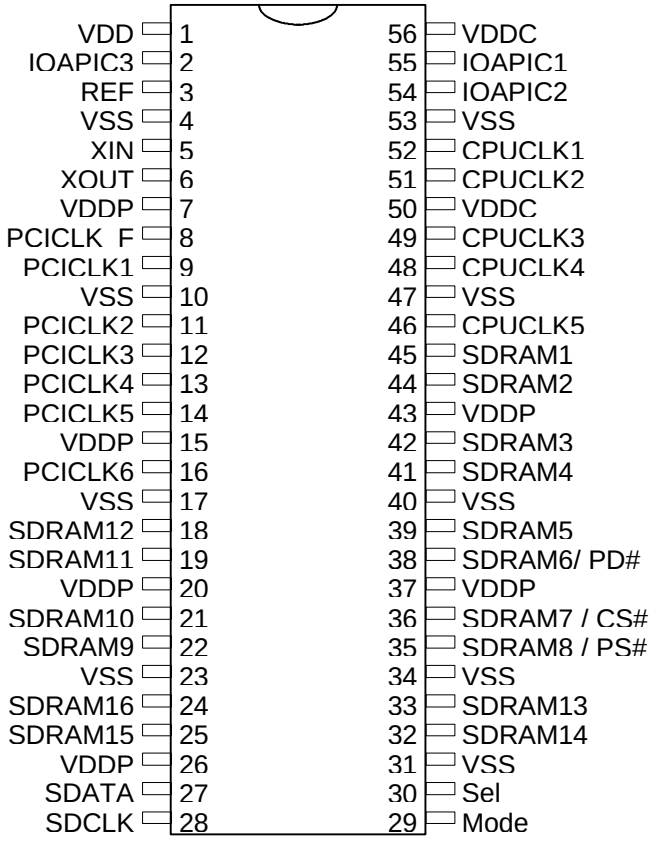
BLOCK DIAGRAM



FREQUENCY TABLE

SEL	CPU	PCI
0	60.0	30.0
1	66.6	33.3

CONNECTION DIAGRAM



PS# : PCI_STOP#
CS# : CPU_STOP#
PD# : PWR_DWN#

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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
5	**Xin**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external crystal (nominally 14.318 MHz) or externally generated reference signal
6	**Xout**	VDD	O	OSC1	O-chip reference oscillator output pin. Drives an external crystal When an externally generated reference signal is used, is left unconnected
30	**SEL**	-	I	PADI4 PU	Frequency select input pin. See frequency select table on page 1.
52, 51, 49, 48, 46	**CPUCLK(1:5)**	VDDC	O	BUF1	Clock outputs. CPU frequency table specified on page 1.
55, 54, 2	**IOAPIC(1:2)**	VDDC	O	BUF2	IOAPIC clock for multi processor support. Fixed frequency at 14.31818 Mhz. (2.5 or 3.3 supply = VDDI)
9, 11, 12, 13, 14, 16	**PCICLK(1:6)**	VDDP	O	BUF4	PCI bus clocks. See frequency select table on page 1.
8	**PCI_F**	VDDP	O	BUF4	PCI clock that ceases only when PD (pin 29) is ascerted. See frequency select table on page 1.
29	**MODE**	-	I	PAD	Input Output mode control pin for pins 35, 36 and 38
27	**SDATA**	-	I/O	PAD	Serial I2C control interface data pin.
28	**SCLK**	-	I	PAD	Serial I2C control interface clock pin.
4, 10, 17, 23, 31, 34, 40, 47, 53	**VSS**	-	P	-	Ground pins for the device.
3	**REF**	VDDP	O	BUF 4	Buffered copy of the 14.31818 Mhz reference oscillator.
7, 15, 20, 26, 37, 43	**VDDP**	-	P	-	3.3 Volt power supply pin for SDRAM, PCI and PCI_F clock output buffers.
56, 50	**VDDC**	-	P	-	3.3 or 2.5 V power supply for CPU and IOAPIC clock buffers.
1	**VDD**	-	P		Power supply pins for analog circuits and core logic
45, 44, 42, 41, 39, 22, 21, 19, 18, 33, 32, 25, 24	**SDRAM(1:5), (8:16)**	VDDP	O	BUF 4	High drive SDRAM output clocks.
35	**SDRAM7**	VDDP	O	BUF 4	Bidirectional pin. When MODE is HIGH, acts as a SDRAM clock. When MODE is low and SEL is HIGH, acts as an input and when driven low, will synchronously stop all PCI clocks (except PCI_F) at a logic low level.
	PS#	-	I	PAD PU	
36	**SDRAM6**	VDDP	O	BUF 4	Bidirectional pin. When MODE is HIGH (logic 1) this pin acts as a SDRAM clock. When MODE is low (logic 0) and SEL is HIGH this pin acts as an input and when driven to a logic low level, will synchronously stop all CPU clocks at a logic low level.
	CS#	-	I	PAD PU	
38	**SDRAM5**	VDDP	O	BUF 4	Bi-directional pin. When MODE is HIGH (logic 1) this pin acts as a SDRAM clock. When MODE is low (logic 0) and SEL is high this pin acts as an input and when driven to a logic low level the IC will enter shutdown mode and **ALL** internal circuitry is turned off.
	PD#	-	I	PAD PU	

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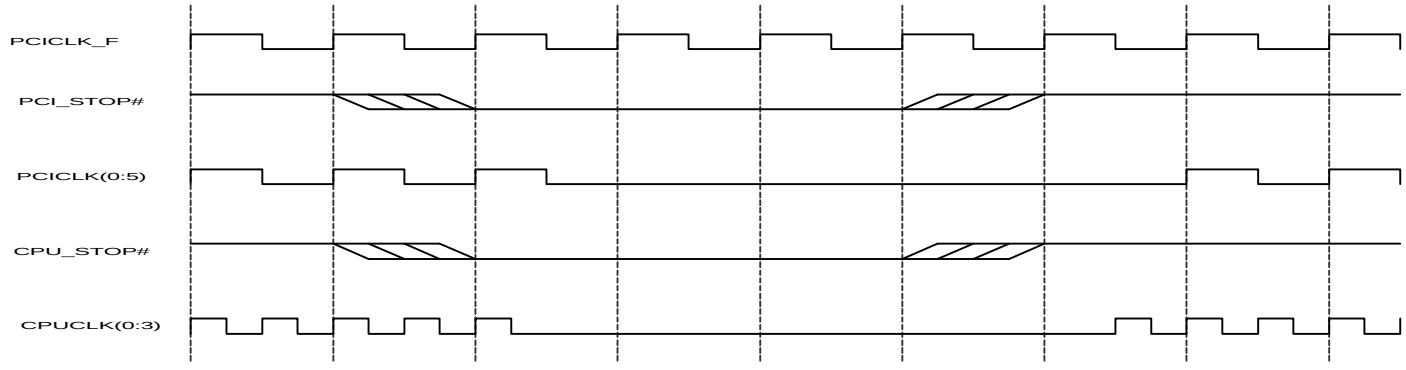
POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or stopped via the 2-wire control interface. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped and on transitions from stopped to running when the chip was not powered down. On power up, the VCOs will stabilize to the correct pulse widths within about 0.2 mS. The CPU, and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

When MODE=0, pins 26 and 27 are inputs PCI_STOP# and CPU_STOP# respectively (when MODE=1, these functions are not available). A particular output is enabled only when both the serial interface and these pins indicate that it should be enabled. The devices clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. On low to high transitions of PWR_DWN#, external circuitry should allow 0.2 mS for the VCOs to stabilize prior to assuming the clock periods are correct. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	OTHER CLKs	XTAL & VCOs
X	X	0	LOW	LOW	LOW	OFF
0	0	1	LOW	LOW	RUNNING	RUNNING
0	1	1	LOW	RUNNING	RUNNING	RUNNING
1	0	1	RUNNING	LOW	RUNNING	RUNNING
1	1	1	RUNNING	RUNNING	RUNNING	RUNNING

POWER MANAGEMENT TIMING



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2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The IMISC674 cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The IMISC674 will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The IMISC674 will not respond to any other control interface conditions. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

Byte 0: Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	*	Reserved, Don't set
6	0	*	Reserved, Don't set
5	0	*	Reserved, Don't set
4	0	*	Reserved, Don't set
3	1	23	48/24 Mhz
2	1	22	48/24 Mhz
1 0	0 0		Bit1 Bit0 1 1 Tri-State 1 0 Reserved 0 1 Test Mode 0 0 Normal

IMPORTANT NOTE

Reserved bits are intended for possible future functions. It is important that they be left at their Power Up logic at all times. Otherwise data sheet specifications cannot be guaranteed.

SERIAL CONTROL REGISTERS (Continued)

Function Table

Function Description	Outputs				
	CPU	PCI	SDRAM	Ref	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	Tclk/2	Tclk/4	Tclk/2	Tclk	Tclk
Normal SEL=1	66	CPU/2	CPU	14.318	14.318
Normal SEL=0	60	CPU/2	CPU	14.318	14.318

Notes:
1. Tclk is a test clock over driven on the Xin input during test mode.

Byte 1: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	1	46	CPUCLK5 enable/Stopped
3	1	48	CPUCLK4 enable/Stopped
2	1	49	CPUCLK3 enable/Stopped
1	1	51	CPUCLK2 enable/Stopped
0	1	52	CPUCLK1 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	8	PCICLK_F enable/Stopped
5	1	16	PCICLK6 enable/Stopped
4	1	14	PCICLK5 enable/Stopped
3	1	13	PCICLK4 enable/Stopped
2	1	12	PCICLK3 enable/Stopped
1	1	11	PCICLK2 enable/Stopped
0	1	9	PCICLK1 enable/Stopped

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Approved Product

SERIAL CONTROL REGISTERS(Continued)

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	35	SDRAM8 enable/Stopped
6	1	36	SDRAM7 enable/Stopped
5	1	38	SDRAM6 enable/Stopped
4	1	39	SDRAM5 enable/Stopped
3	1	41	SDRAM4 enable/Stopped
2	1	42	SDRAM3 enable/Stopped
1	1	44	SDRAM2 enable/Stopped
0	1	45	SDRAM1 enable/Stopped

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	24	SDRAM16 enable/Stopped
6	1	25	SDRAM15 enable/Stopped
5	1	32	SDRAM14 enable/Stopped
4	1	33	SDRAM13 enable/Stopped
3	1	18	SDRAM12 enable/Stopped
2	1	19	SDRAM11 enable/Stopped
1	1	21	SDRAM10 enable/Stopped
0	1	22	SDRAM9 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	2	IOAPIC3 enable/Stopped
5	1	54	IOAPIC2 enable/Stopped
4	1	55	IOAPIC1 enable/Stopped
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	1	3	REF enable/Stopped

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Approved Product

SERIAL CONTROL REGISTERS(Continued)

Byte 6: Reserved Register

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	-55ºC to +125ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	88	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	150	µA	PD# = 0, MODE = 0
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC

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SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Skew (CPU-CPU,SDRAM-SDRAM,PCI-PCI)	tSKEW1	-	-	350	ps	15 pf Load Measured at 1.5V
Skew (CPU-SDRAM)	tSKEW2	-	200* 300**	500* 600**	ps	20 pf CPU, 30 pF SDRAM load * @ VDDC = 3.3V ±5% ** @ = VDDC = 2.5V ±5%,
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

note 1: Ring Back must not enter this range.

TYPE 1 BUFFER CHARACTERISTICS FOR CPUCLK(1:4)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-27	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-27	mA	Vout = 2.6 V
Pull-Down Current Min	IOL_{min}	-27	-	-	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	2.0	nS	20 pF Load
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

TYPE 2 BUFFER CHARACTERISTICS FOR IOAPIC(1:2)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-28	-	-	mA	Vout = 1.4 V
Pull-Up Current Max	IOH_{max}	-	-	-28	mA	Vout = 2.7 V
Pull-Down Current Min	IOL_{min}	-28	-	-	mA	Vout = 1.0 V
Pull-Down Current Max	IOL_{max}	-	-	28	mA	Vout = 0.2 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	2.0	nS	20 pF Load
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

TYPE 4 BUFFER CHARACTERISTICS FOR REF and SDRAM(1:16)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-46	-	-	mA	Vout = 1.65 V
Pull-Up Current Max	IOH_{max}	-	-	46	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	-53	-	-	mA	Vout = 1.65 V
Pull-Down Current Max	IOL_{max}	-	-	53	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

TYPE 5 BUFFER CHARACTERISTICS FOR PCICLK(1:6, F)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-33	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-33	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	30	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	38	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	15 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
VDD = VDDP =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

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CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		6		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	the crystals rated load. note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	crystals internal package capacitance (total)

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore	2.0 pF
Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore	3.0 pF
External crystal loading capacitors (connected to ground) (3o pF each)	15.0 pF
the total parasitic capacitance would therefore be	= 20.0.0 pF.

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

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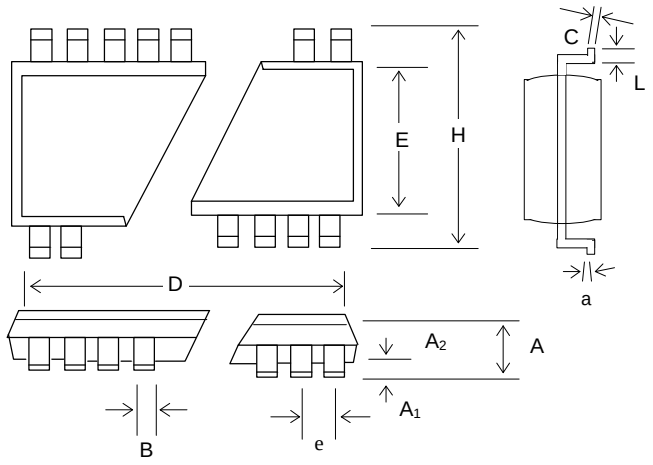
PACKAGE DRAWING AND DIMENSIONS



56 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	.720	.725	.730	18.29	18.42	18.54
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC674BYB	56 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC674BYB
Date Code, Lot #

IMISC674BYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number

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