Clock Generator for 3 DIMM, USB and 2.5V Pentium® Design

Approved Product

PRODUCT FEATURES

- Supports Pentium®, Pentium® II, Pentium® Pro, and Cyrix CPU's.
- 12 host clocks for additional SDRAM support.
- Optional common or mixed supply mode :

  VDD = VDDRM = VDDCPU = VDDIO = 3.3V

  VDD = VDDRM = VDDCPU = 3.3V, VDDIO = 2.5V

  VDD = VDDRM = 3.3V, VDDCPU = VDDIO = 2.5V

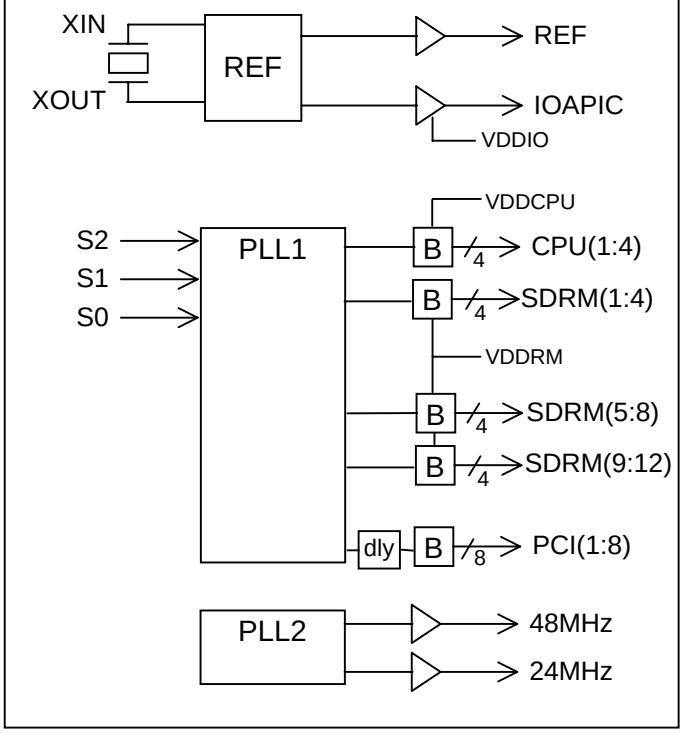
  VDD = 3.3V, VDDRM = VDDCPU = VDDIO = 2.5V
- < 250 pS skew on CPU and SDRM* buffers
- < 250 pS skew on PCI buffers
- Buffer output impedance of ≤ 22 ohms
- 52 Pin QFP package for minimum board space and easy layout

FREQUENCY TABLE (MHz)

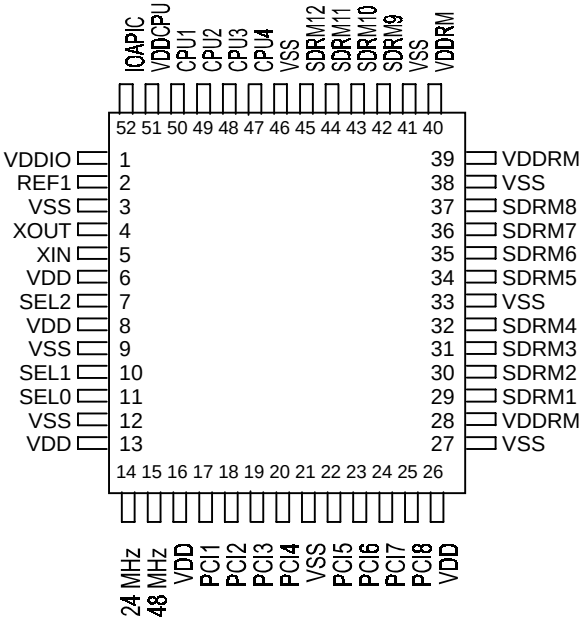
S2	S1	S0	CPU	PCI
0	0	0	tristate	tristate
0	0	1	75	a.32
0	1	0	55	27.5
0	1	1	75	37.5
1	0	0	50	25
1	0	1	60	30
1	1	0	66.6	33.3
1	1	1	test	test

a.32 = Asynchronous PCI.

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

Xin, Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal in which case Xout must be kept unconnected.

S0, S1, and S2 - Standard frequency select inputs. These inputs have internal pull-ups($\geq$ 100KΩ).

CPU(1:4) - Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset, Cache, etc... CPU1-CPU4 voltage level is controlled by VDDCPU.

SDRM(1:12) - Low skew (<250 pS) clock outputs for SDRAM. Voltage level is controlled by VDDRM.

IOAPIC - Buffered output clock of the crystal. Voltage level is controlled by VDDIO.

PCI(1:8) - Low skew (<250pS) clock outputs for PCI frequencies. These buffers voltage level is controlled by VDD.

REF - Buffered output of on-chip reference.

48MHz - Frequency output for USB.
24MHz - Frequency output for Floppy Drive.

VSS - Circuit ground.

VDD - Positive power supply.

VDDCPU - 3.3V/2.5V logic level control for CPU(1:4) outputs. Voltage cannot be greater than VDD.

VDDRM - 3.3V logic level control for SDRM(1:12) outputs. Voltage cannot be greater than VDD.

VDDIO - 3.3V/2.5V logic level control for IOAPIC output. Voltage cannot be greater than VDD.

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0ºC to + 125ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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ELECTRICAL CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low, or High Current with Pull- up or Pull-down	IIL, IIH	7	-	70	µA	S0-S2 Inputs
Output Low Voltage	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage	VOH	2.4	-	-	Vdc	All Outputs
Tri-State leakage Current	Ioz	-	-	10	µA	All Outputs
Dynamic Supply Current	Icc	-	250	300	mA	CPU = 66.6 MHz, PCI = 33.3 Mhz All Clocks Unloaded.
Static Supply Current	Icc (PD)	-	50	100	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
VDD = VDDCPU = VDDRM = 3.3V±5%, TA = 0ºC to +70ºC						

TB4-M BUFFER SWITCHING CHARACTERISTICS (ALL OUTPUTS)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Rise (0.4V - 2.0V) and Fall (2.0V-0.4V) time	tTLH, tTHL	-	-	1.6	ns	15 pf Load CPU, SDRAM and PCI outputs
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Buffer out Skew All CPU, SDRAM and PCI Buffer Outputs	tSKEW	-	-	250	ps	15 pf Load Measured at 1.5V
ΔPeriod Cycles, CPU	ΔP	-	-	±250	ps	-
Jitter Absolute, CPU	tjab	-	-	500	ps	(Long term jitter measured over a 3 minute period)
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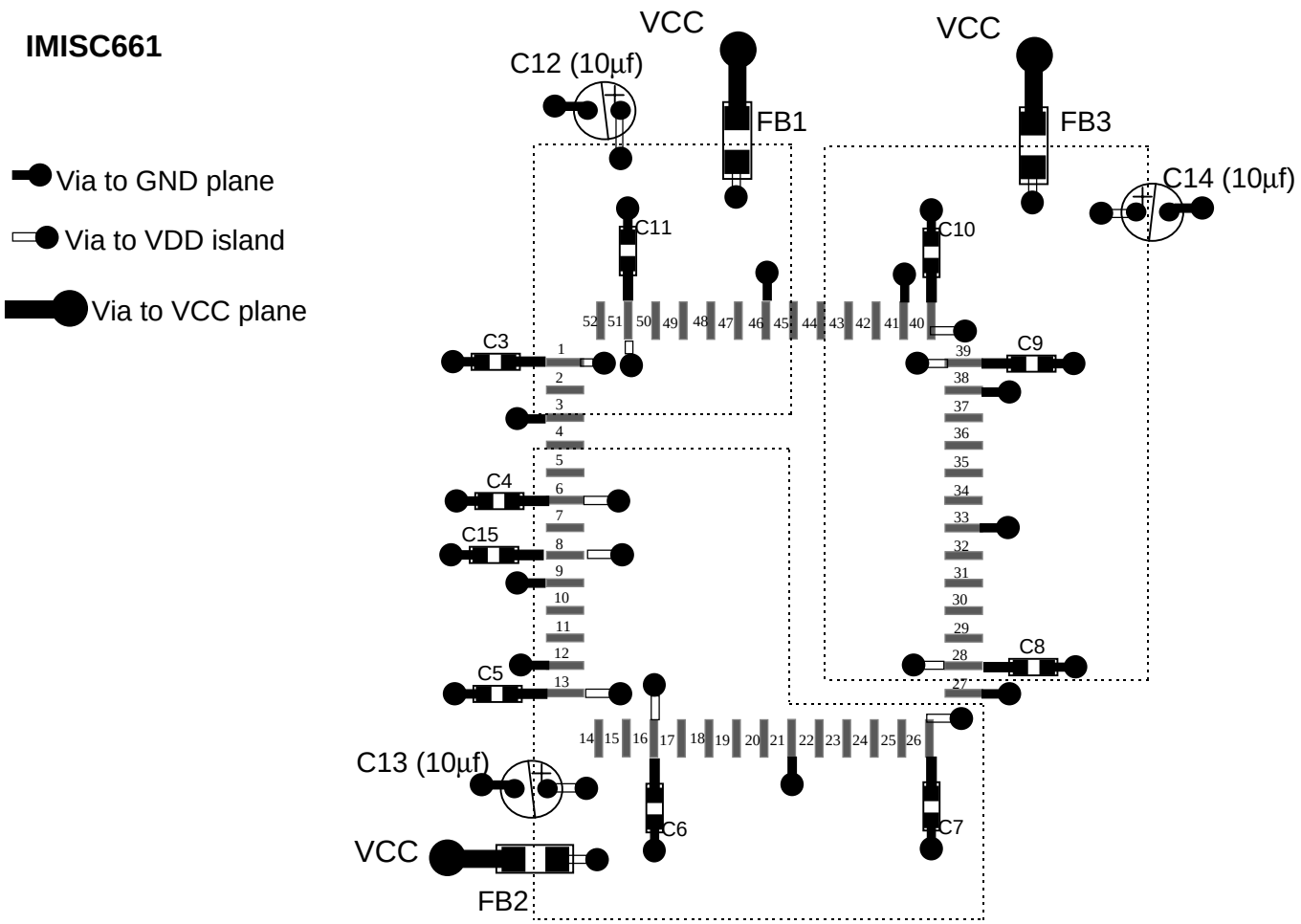
PCB LAYOUT SUGGESTION



This is only a layout suggestion for best performance and lower EMI. The designer may choose a differnent approach such as using VDD traces instead of islands (dashed areas). Also, the designer may choose to use less than three beads. Regardless of which way the layout is implemented, Bypass caps : C3, C4, C5, C6, C7, C8, C9, C10, C11 and C15 (all 0.1 µF) should always be used and placed as close to their VDD pins as possible.

NOTES

1. POWER SUPPLY BYPASS CAPS (O.1UF) MUST BE POSITIONED AS CLOSE AS POSSIBLE TO VDD PINS TO BE EFFECTIVE.
2. BYPASS CAPS MUST BE LOW LEAKAGE SUCH AS MULTILAYER CERAMIC Z5U OR X7R MATERIAL WHICH ALSO RESULTS IN LOWER IMPEDANCE AT HIGH FREQUENCY.
3. FB: FERRITE BEAD

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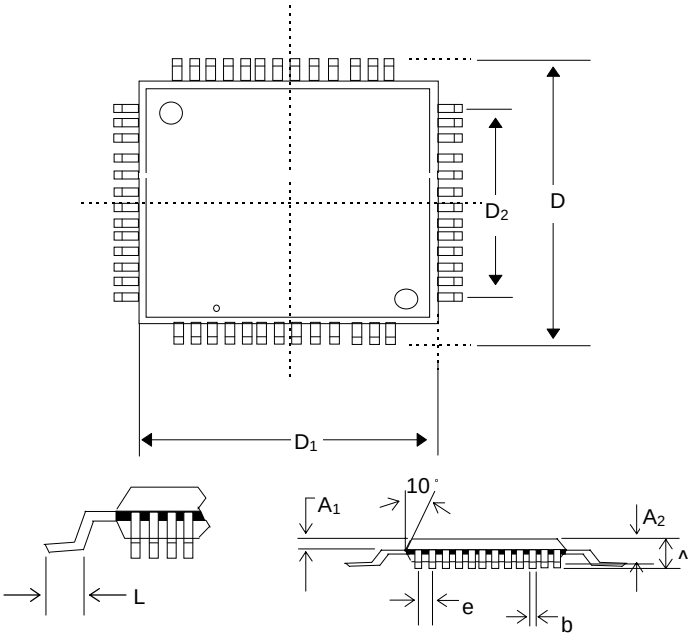
PACKAGE DRAWING AND DIMENSIONS



52 PIN QFP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	0.084	0.093	-	2.13	2.35
A_1	0.00	.006	.010	0.00	0.15	0.25
A_2	0.077	0.079	0.083	1.95	2.00	2.10
D	0.537	0.547	0.557	13.65	13.90	14.15
D_1	0.390	0.394	0.398	9.90	10.00	10.10
D_2	0.307 REF			7.80 REF		
b	0.009	-	0.015	0.22	-	0.38
e	.0256 BSC			0.65 BSC		
L	0.026	0.031	0.037	0.65	0.80	0.95

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC661BAB	52 PIN QFP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC661BAB
Date Code, Lot #

IMISC661BAB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: A= QFP
- Revision
- IMI Device Number