Clock Generator for Pentium Based Designs W/2 DIMM Support

Approved Product

PRODUCT FEATURES

- Supports Pentium® series, 6X86 and K6 CPUs.
- Supports Intel VIA, SiS and Opti chipset requirements.
- Supports Sychronous DRAM designs
- 4 host (CPU/AGP) clocks & 8 SDRAM clocks.
- Optional common or mixed supply mode :

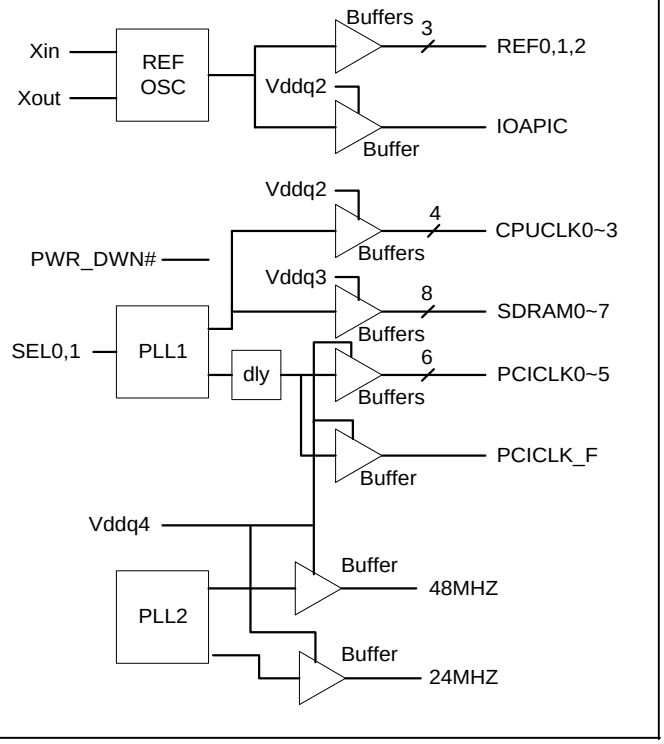
  (Vdd = Vddq3 = Vddq4 = Vddq2 = 3.3V)

  (Vdd = Vddq3 = Vddq4 = 3.3V, Vddq2 = 2.5V)
- < 250 pS skew on CPU buffers
- < 250 pS skew on PCI buffers
- Supports Single Pin Power Management.
- 48 Pin SSOP package for minimum board space

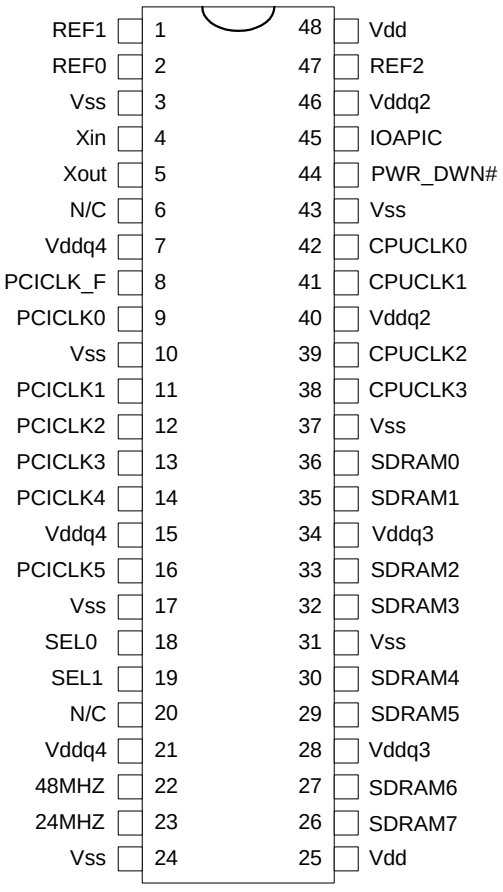
FREQUENCY TABLE

SEL1	SEL0	CPU	PCI
0	0	55.0	27.5
0	1	75.0	37.5
1	0	60.0	30.0
1	1	66.6	33.3

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

Xin, Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.

SEL(0:1) - Standard frequency select inputs. They have internal pull-ups.

CPUCLK(0:3) - Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset, Cache. Vddq2 is the supply voltage for these outputs.

SDRAM(0:7) - Synchronous DRAM DIMs clocks. They are powered by Vddq3.

PCICLK(0:5) - Low skew (<250pS) clock outputs for PCI frequencies. These buffers voltage level is controlled by Vddq3.

PCICLK_F - A PCI clock output that does not stop until in power down mode. It is synchronous with other PCI clocks.

REF(0:2) - Buffered outputs of reference 14.3MHZ.

IOAPIC - Buffered output of 14.3MHZ for multiprocessor support. It is powered by Vddq2.

48MHz - Frequency output for USB.
24MHz - Frequency output for super I/O.

PWR_DWN# - Power down pin to turn the power of the whole chip down including the VCOs and the PCICLK_F output pin. It has an internal pull-up

Vss - Ground pins for the chip.

Vdd - Power supply pins for analog circuit and core logic.

Vddq3 - Power supply pins for 3.3V IO pins.

Vddq2 - Power supply pins for 2.5V/3.3V IO pins.

N/C - No connection pins.

POWER MANAGEMENT FUNCTIONS

The IMISC652 clocks may be disabled using the PWR_DWN# pin in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. When powered down, the reference oscillator and VCOs are stopped. On low to high transitions of PWR_DWN#, external circuitry should allow 3 mS for the VCOs to stabilize prior to assuming the pulse widths are correct.

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	-55ºC to +125ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Output Low Current	IOL1	61	-	-	mA	VOL1 = 1.6V (@ CPU, SDRAM, PCI, IOAPIC and REF0 clocks)
Output High Current	IOH1	61	-	-	mA	VOH1 = 1.0V (@ CPU, SDRAM, PCI, IOAPIC and REF0 clocks)
Output Low Current	IOL2	42	-	-	mA	VOL2 = 1.9V (@ 48Mhz, 24 Mhz, REF2 and REF1 clocks)
Output High Current	IOH2	40	-	-	mA	VOH2 = 1.0V (@ 48Mhz, 24 Mhz, REF2 and REF1 clocks)
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	40	-	mA	CPU = 66.6 Mhz, No Load
Static Supply Current	Idd	-	200	-	µA	PWR_DWN# = Low
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDq2 = VDDq3 = 3.3V±5%, TA = 0ºC to +70ºC

Contact IMI for IBIS models.

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SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Rise (0.4V - 2.0V) and Fall (2.0V-0.4V) time	tTLH, tTHL	-	-	1.6	ns	22 pf Load CPU and PCI outputs
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	tSKEW1	-	-	250	ps	15 pf Load Measured at 1.5V
Skew (CPU-SDRAM)	tSKEW2	-	-	500	ps	15 pf Load Measured at 1.5V
ΔPeriod Cycles, CPU	ΔP	-	-	±250	ps	-
Jitter Absolute, CPU	tjab	-		500	ps	-
Overshoot/Undershoot Beyond Power Rails	V_{over}	-	-	1.5	V	22 ohms @ source of 8 inch PCB run to 15 pf load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	note1
						VDD = VDDq2 = VDDq3 = 3.3V±5%, TA = 0ºC to +70ºC

note 1: Ring Back must not enter this range.

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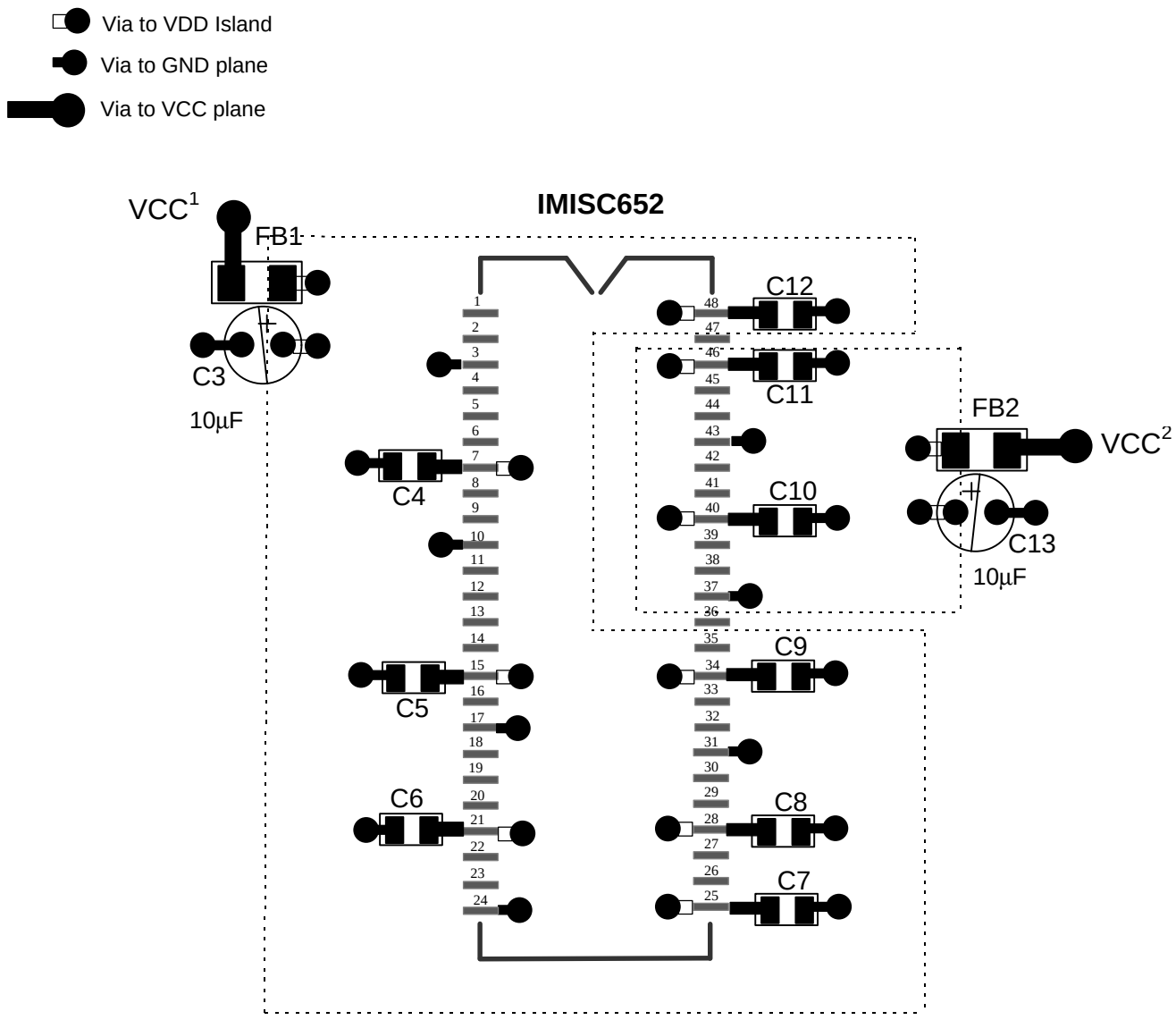
PCB LAYOUT RECOMMENDATION



This is only a layout recommendation for best performance and lower EMI. The designer may choose a differnent approach but C4, C5, C6, C7, C8, C9, C10, C11and C12 (all are 0.1µf) should always be used and placed close to their VDD pins.

PACKAGE DRAWING AND DIMENSIONS

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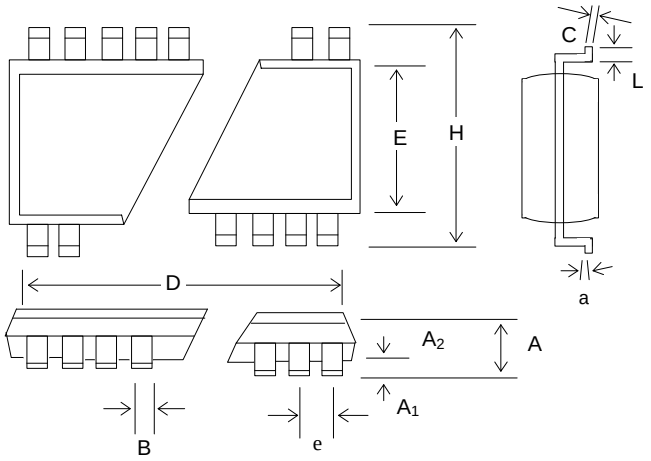

48 PIN SSOP OUTLINE DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
IMISC652EYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC652EYB
Date Code, Lot #

IMISC652EYB

- Flow
  B = Commercial, 0ºC to + 70ºC
- Package
  Y = SSOP
- Revision
- IMI Device Number