IMISC621 SYSTEM CLOCK CHIP

Preliminary January, 1996 **CMOS PLL**

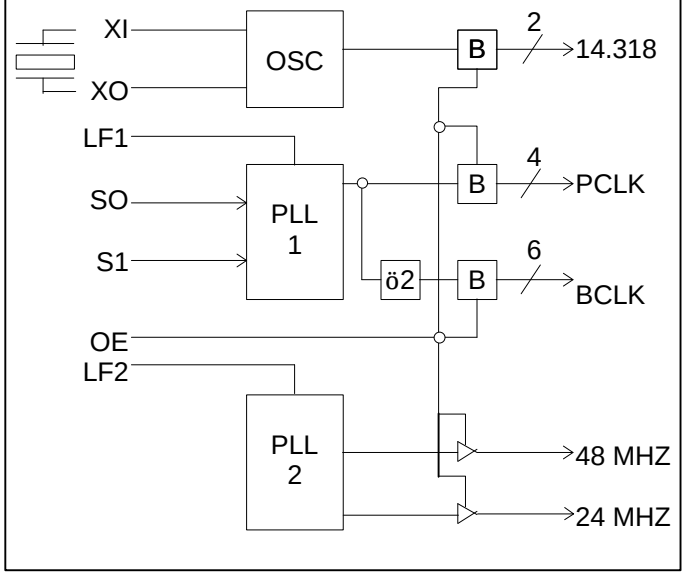
PRODUCT FEATURES

- Integrates clock generator and distribution buffers
- Supports Pentium™ and Cyrix based designs
- < 250 ps typical buffer skew on PCLK and on BLCK
- Supports USB (Universal Serial Bus)
- Designed to Intel's clock specification.
- 60 mA switching current
- 28 Pin SOIC

FREQUENCY TABLE

S0	S1	PCLK
0	0	50 MHz
0	1	60 MHz
1	0	66.6 MHz
1	1	55 MHz

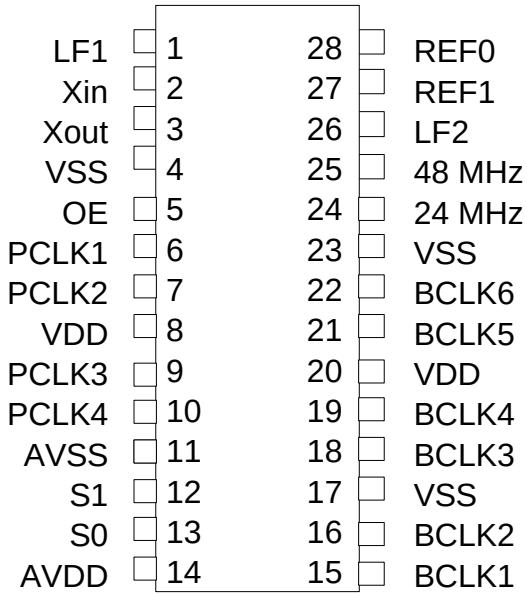
BLOCK DIAGRAM



PRODUCT DESCRIPTION

The IMISC621 provides the clock frequencies and clock distribution buffers required on a Pentium™ synchronous PCI system board. The SC621 contains PLL's for fixed and programmable clocks, fan-out buffers for the CPU and PCI busses, and operates from a 3.3V or 5V power source. The frequency selection of the PCLK outputs is determined by the S0-S1 pins. The on-chip buffers provide the low skew performance required by the CPU and PCI busses.

CONNECTION DIAGRAM



APPLICATIONS

The IMISC621 supports synchronous Pentium™ designs by providing clock distribution for the CPU and PCI bus and system fixed frequencies. The performance, functionality, and pin out conform to the Intel Mars and Triton II core logic requirements.

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PIN DESCRIPTIONS

Xin and Xout- These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal of 14.31818 at 22 PF load. Xin may also serve as an input for an externally generated CMOS reference signal.

OE- Output enable. When OE is high, all clock outputs are enabled. When OE is low, all clock outputs are tristated. This input has internal pull-up resistor to VDD.

PCLK(1:4) - Low skew (<200pS) buffered outputs for host clocks. These outputs have 60mA switchng currents at 3.3v.

BCLK(1:6) - Low skew (<250pS) buffered outputs for PCI clocks. These outputs have 60mA switchng currents at 3.3v. They are synchronous and 2 nS (Typ) offset to PCLK.

48 MHz - 48 MHz USB clock output
24 MHz - 24 MHz Floppy drive clock output

REF0, REF1 - 14.31818 MHz clock outputs.

S1 and S0- Frequency select inputs. These inputs select the frequency of the PCLK and BCLK outputs. Both have internal pull-down resistors to VSS.

VSS - Circuit grounds.

VDD- Positive power supplies.

AVSS- Analog circuit ground.

AVDD- Analog positive power supply. (3.3V)

SC 621 FREQUENCY SELECT TABLE

S0	S1	XIN	PCLK	BCLK	REF	48 MHz	24 MHz
0	0	14.318	50	25	14.318	48	24
0	1	14.318	60	30	14.318	48	24
1	0	14.318	66.6	33.3	14.318	48	24
1	1	14.318	55	27.6	14.318	48	24

MAXIMUM RATINGS

Voltage Relative to VSS	-0.3V
Voltage Relative to VDD	0.3V
Storage Temperature:	-65°C to +150°C
Ambient Temperature:	-0°C to + 70°C
Maximum Supply Voltage	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)< VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

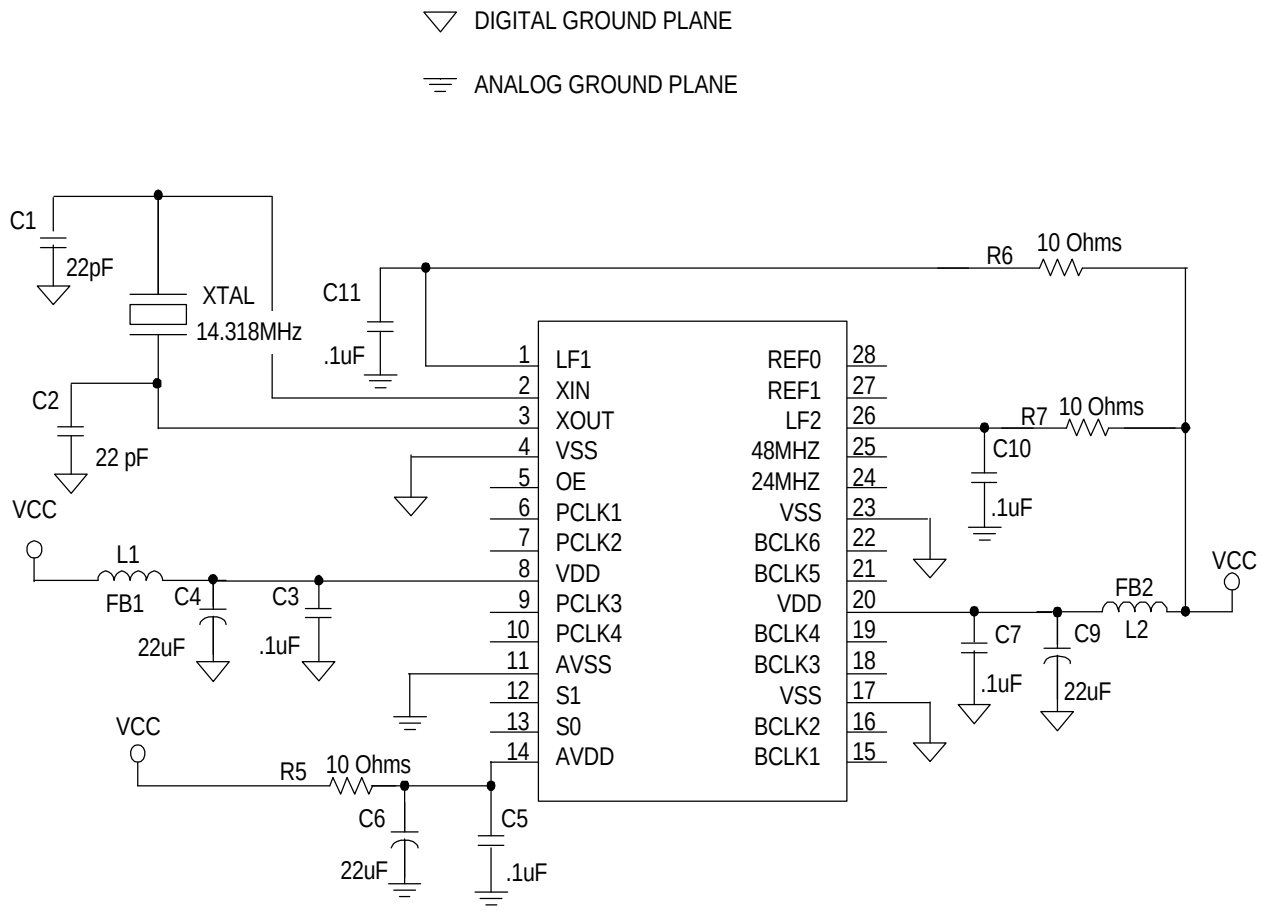
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	OE, S0-S1 Inputs
Input High Voltage	VIH	2.0	-	-	Vdc	OE, SO-S1 Inputs
Input Low, or high Current with Pull up or Pull-down	IIL, IIH	-	-	5 ±50	uA	OE, S0-S1 Inputs
Output Low Voltage IOL = 12 mA*	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH=12 mA*	VOH	2.4	-	-	Vdc	All Outputs
Tri-State Leakage Current	IOZ	-	-	10	uA	LF1 and LF2 and All Outputs
Dynamic Supply Current	ICC	-	-	60	mA	PCLK = 66.6 MHz
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 sec. max
AVDD = 3.3V						VDD = 3.3V +/- 10% , TA = 0°C to +70°C

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.4V - 2.0V) and Fall (2.0V-0.4V) time All Outputs	**t**TLH, **t**THL	-	-	1.5	ns	15 pf Load
Output Duty Cycle		45	50/50	55	%	Measured at 1.5V
Skew PCLK to BCLK	**t**SKEWPB	1.0	-	4	ns	15 pf Load Measured at 1.5V
Buffer out Skew PCLK or BCLK	**t**SKEW	-	-	250	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles PCLK	ΔP	-	-	±200	ps	-
Jitter Absolute PCLK and REF	**t**jab	-	±200	-	ps	-
Input Rise/Fall Time S0-S1		-	-	2	us	-
Switching Current Low: PCLK, BCLK Outputs Other Outputs	IOL (AC) IOL (AC)	-	60 30	-	mA mA	VOL = 1.5V VOL = 1.5V
Switching Current High:, PCLK, BCLK Outputs Other Outputs	IOH (AC) IOH (AC)	-	60 30	-	mA mA	VOL = 1.5V VOL = 1.5V
AVDD = 3.3V						VDD = 3.3V +/- 10% , TA = 0°C to +70°C

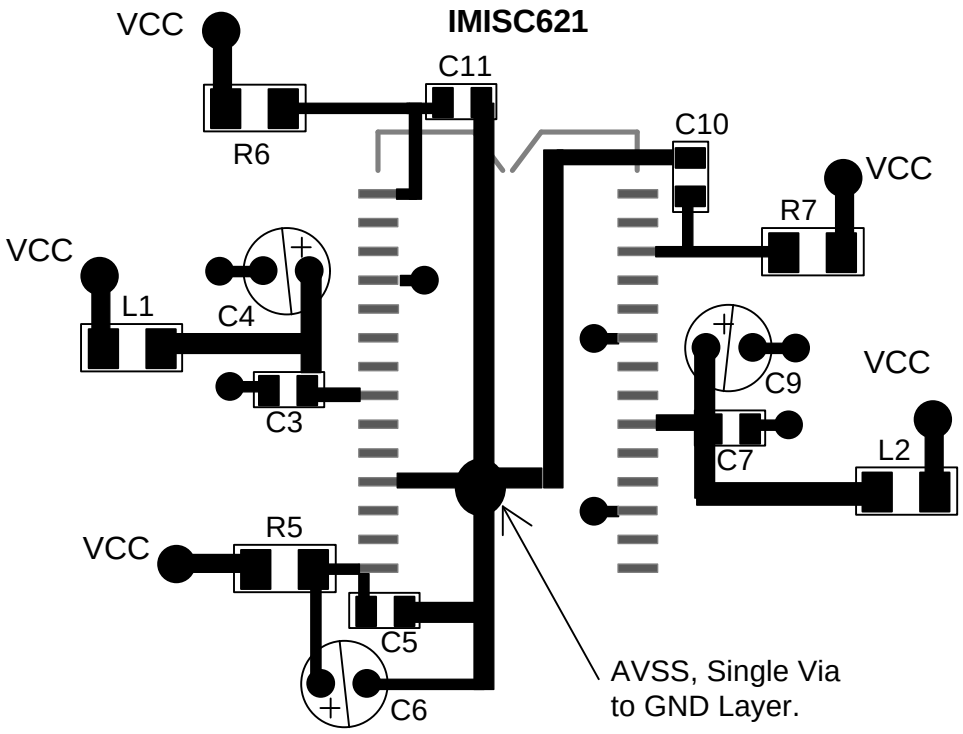
APPLICATION DIAGRAM

NOTE: IF VCC AT CLOCK GENERATOR CONTAINS POSITIVE VOLTAGE STEPS > OR -100 MV WITHIN 5 US (FROM TURNING DISK DRIVE OFF, ETC.), THE VALUES OF L1, C1, AND C2 SHOULD BE INCREASED APPROXIMATELY 100% TO AVOID OUT-OF-SPEC SHORT CLOCK CYCLES.



NOTE 1: C3, C5, C7, C8 MUST BE CLOSE TO THEIR VDD PINS.
NOTE 2: R6 AND R7 SHOULD BE PLACED WHEN USING OTHER THAN IMI CLOCK GENERATOR.

PCB LAYOUT SUGGESTION



NOTES

1) This layout accommodates IMI technology while maintaining pin compatibility with other vendors' products designed to the Intel clock generator spec. R 6 = R7 = ì (open) for IMI; R5 = R6 = 0 (closed) for other vendors. Note that jumpers may also be used instead of the resistor R6 and R7.

2) Separate top layer traces and filtering to AVDD and AVSS produce the best performance for IMI clock generators.

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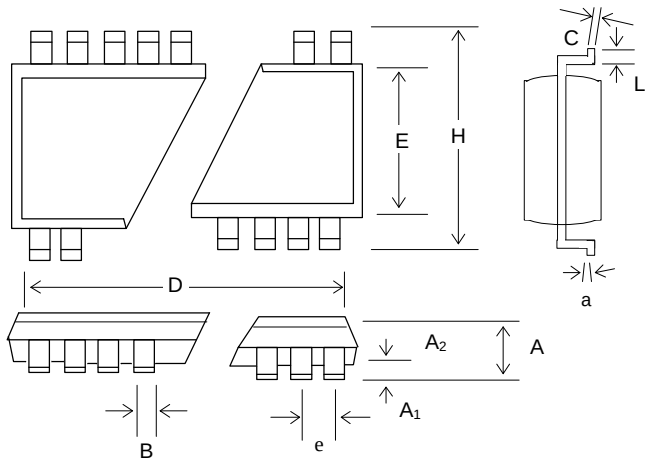
PACKAGE DRAWING AND DIMENSIONS



28 PIN SOIC OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A_1	0.005	0.009	0.0115	0.127	0.22	0.29
A2	0.090	0.092	0.094	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.009	0.010	0.0125	0.23	0.25	032
D	0.701	0.706	0.711	17.81	17.93	18.06
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.050 BSC			1.27 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0°	5°	8°	0°	5°	8°
L	0.024	0.032	0.040	0.61	0.81	1.02

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC621xXB	28 PIN SOIC	Commercial, 0°C to + 70°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC621xXB
Date Code, Lot #

IMISC621xXB

Flow
B = Commercial, 0°C to + 70°C

Package
X = SOIC

Revision

IMI Device Number

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