IMISC611 SYSTEM CLOCK CHIP

Preliminary, May, 1996 CMOS PLL

PRODUCT FEATURES

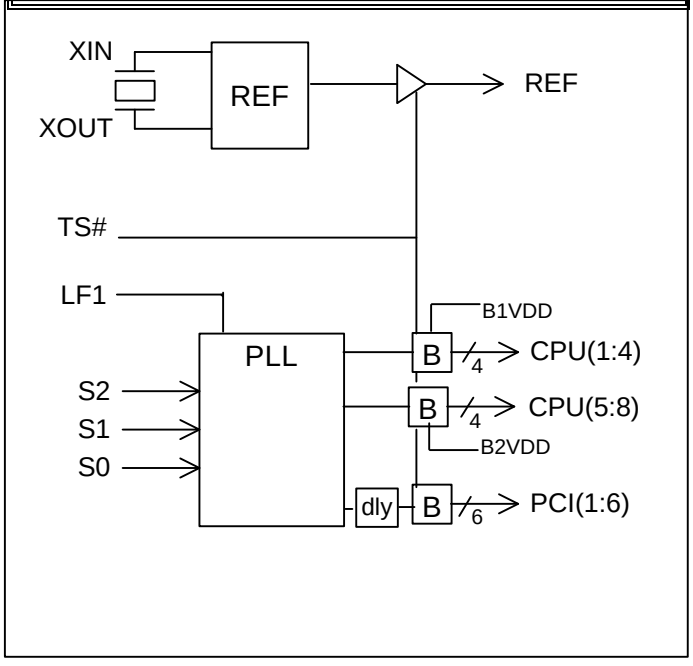
- Supports Pentium and Cyrix CPU's.
- 8 host (CPU) clocks for additional SDRAM support.
- Optional common or mixed supply mode :

  (VDD = B1VDD = B2VDD = 2.5V)
  (VDD = B1VDD = B2VDD = 3.3V)
  (VDD = 3.3V, B1VDD = B2VDD = 2.5V)
  (VDD = 3.3V, B1VDD = 3.3V, B2VDD = 2.5V)
  (VDD = 3.3V, B1VDD = 2.5V, B2VDD = 3.3V)
- < 250 pS skew on CPU buffers
- < 250 pS skew on PCI buffers
- 60 mA buffer switching current
- 34 Pin SSOP package for minimum board space

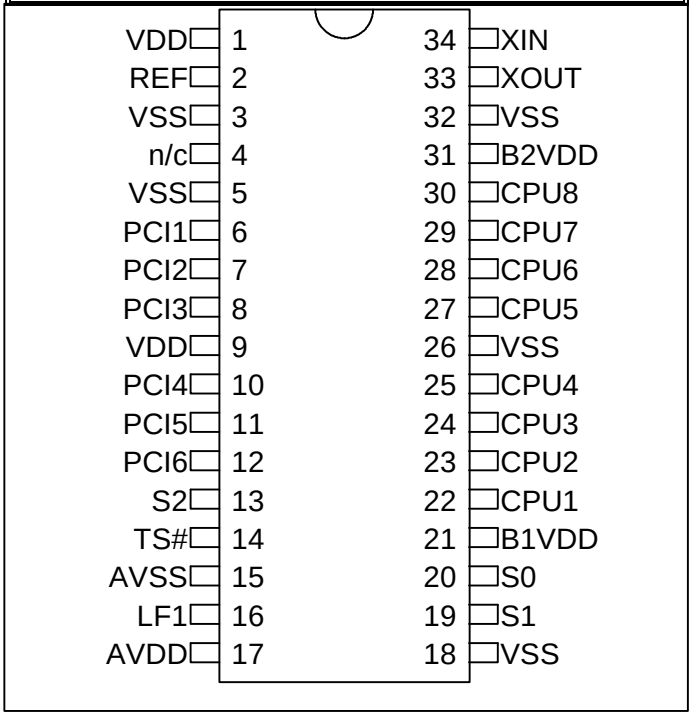
FREQUENCY TABLE

S2	S1	S0	CPU	PCI
0	0	0	50	33.3
0	0	1	55	36.67
0	1	0	TEST	TEST
0	1	1	75	37.5
1	0	0	50	25
1	0	1	55	27.6
1	1	0	60	30
1	1	1	66.6	33.3

BLOCK DIAGRAM



CONNECTION DIAGRAM



APPLICATIONS

Pentium™ or Cyrix CPU's with any available chipset support for PCI systems.

INTERNATIONAL MICROCIRCUITS, INC. 525 LOS COCHES ST.
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PIN DESCRIPTION

Xin, Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.

S0, S1, and S2 - Standard frequency select inputs. These inputs have internal pull-ups.

TS# - This input pin is used for tristate.. If TS# = 0, then all outputs are tristated and the device is in shutdown mode (VCO's off, crystal oscillator is off, and all logic is reset.).
When TS # = 1 the device is in normal operating mode. This pin has an internal pull-up.

CPU(1:8) - Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset, Cache, SDRAM, etc.. CPU1-CPU4 voltage level is controlled by B1VDD and CPU5-CPU8 voltage level is controlled by B2VDD. All these buffers have 60 mA switching current at 3.3V.

PCI(1:6) - Low skew (<250pS) clock outputs for PCI frequencies. These buffers voltage level is controlled by VDD. All these outputs have 60 mA switching current at 3.3V.

REF - Buffered output of on-chip reference. This output has 30mA switching current at 3.3V.

LF1, LF2 - These are the loop filter low current outputs for the clock generators. A 0.1 uF capacitor should be connected from each pin to the AVSS trace or plane.

VSS - Circuit Digital ground.

VDD - circuit digital positive power supply.

AVSS - analog circuit Ground.

AVDD - Analog circuit positive power supply.
This pin must always be connect to 3.3V supply only.

B1VDD - 3.3V/2.5V logic level control for CPU(1:4) outputs. Voltage cannot be greater than VDD.

B2VDD - 3.3V/2.5V logic level control for CPU(5:8) outputs. Voltage cannot be greater than VDD.

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	-55ºC to +125ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low, or High Current with Pull- up or Pull-down	IIL, IIH	-	-	5 ±50	µA	S0-S2, TS# Inputs
Output Low Voltage IOL = 12mA	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH = 12mA	VOH	2.4	-	-	Vdc	All Outputs
Tri-State leakage Current	Ioz	-	-	10	µA	LF1, and LF2
Dynamic Supply Current	Icc	-	-	65	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Icc (PD)	-	200	-	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

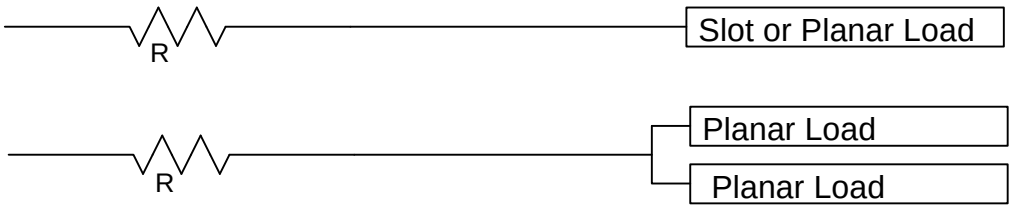
AVDD = 3.3V ***VDD = B2VDD = B1VDD = 3.3V, TA = 0ºC to +70ºC***

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.4V - 2.0V) and Fall (2.0V-0.4V) time	tTLH, tTHL	-	-	1.2	ns	15 pf Load CPU and PCI outputs
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Buffer out Skew All CPU and PCI Buffer Outputs	tSKEW	-	-	250	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles CPU	ΔP	-	-	±200	ps	-
Jitter Absolute CPU	tjab	-	±200	-	ps	-
Switching Current Low	IOL(AC)	-	60	-	mA	VOL = 1.5V
Switching Current High	IOH(AC)	-	60	-	mA	VOL = 1.5V

AVDD = 3.3V ***VDD = B2VDD = B1VDD = 3.3V, TA = 0ºC to +70ºC***

Output Loading Suggestion.



SUGGESTED MAXIMUM TRACE LENGTH, 10 INCHES.
(The above suggestions are based on VDD = B1VDD = B2VDD = 3.3 v)

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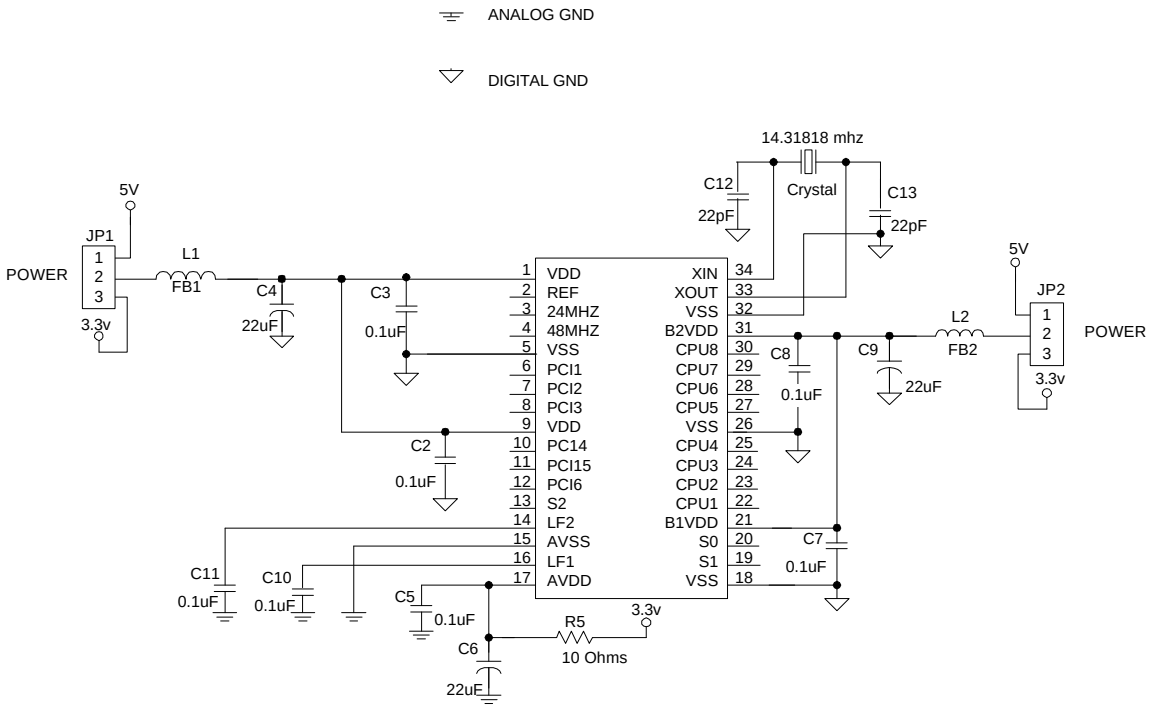
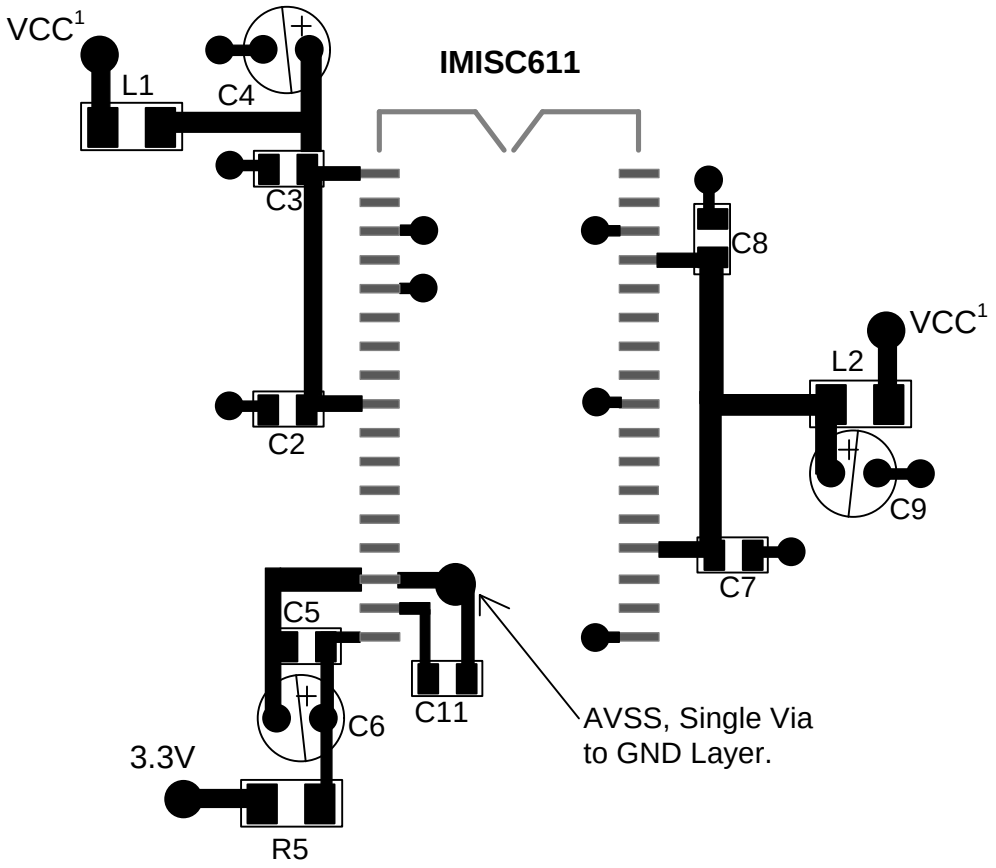
APPLICATION DIAGRAM



NOTE 1: PIN21, B1VDD MAY HAVE ITS OWN POWER (INDEPENDENT OF B2VDD, PIN 31)
NOTE 2: C2, C3, C5, C6, AND C8 MUST BE CLOSE TO THEIR VDD PINS (SEE PAGE 6)

PCB LAYOUT SUGGESTION



This is only a layout suggestion for best performance and lower EMI. The user may choose a differnent approach but C2, C3, C5, C7, and C8 should be always be used and placed close to their VDD pins.

NOTES

1. VCC MAY BE 3.3 V OR 5V .
2. POWER SUPPLY BYPASS CAPS (O.1UF) MUST BE POSITIONED CLOSE TO VDD PINS TO BE EFFECTIVE.
3. TOP LAYER TRACES AND FILTERING TO AVDD / AVSS SEPARATED FROM TRACES TO VDD /VSS PRODUCE BEST PERFORMANCE.
4. C10 and C11 CAPS MUST BE LOW LEAKAGE SUCH AS MULTILAYER CERAMIC Z5U OR X7R MATERIAL.

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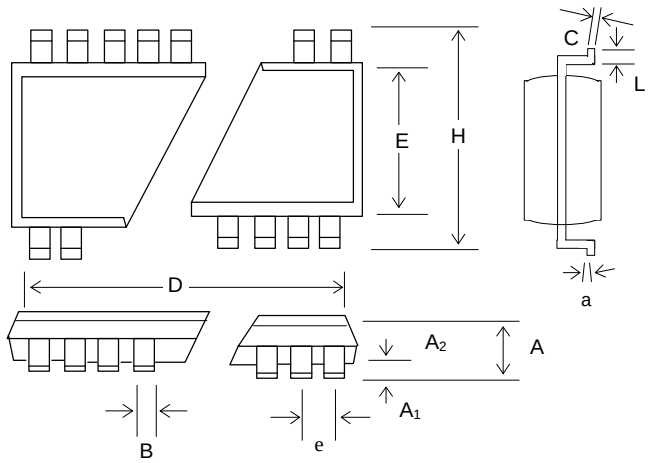
PACKAGE DRAWING AND DIMENSIONS



34 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A_1	0.0050	0.009	0.0115	0.127	0.22	0.29
A2	0.090	0.092	0.094	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.0091	0.010	0.0125	0.23	0.25	0.32
D	0.701	0.706	0.711	17.81	17.93	18.06
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.040 BSC			1.016 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	4º	8º	0º	4º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC611xYB	34 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The “x” following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC611xYB
Date Code, Lot #

IMISC611xYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number