C9806I

I^{2}C Frequency Clock Generator for Mobile Pentium® II Applications.

Preliminary

Product Features

- Supports Pentium® & Pentium® II CPUs.
- 2 CPU clocks.
- 7 independent SDRAM clocks for 3 SO DIMMs.
- Power Management hardware support.
- 7 PCI synchronous clocks.
- < 175 pS skew CPU and SDRAM clocks.
- < 175 pS skew among PCI clocks.
- I^{2}C 2-Wire serial interface
- Programmable registers featuring:
- Individual clock enable/disable
- Mode as Tri-state, test, or normal
- 24/48 MHz selections
- Enable/Disable SST
- Available in 48-pin SSOP and TSSOP packages
- **Spread Spectrum** Technology (SST)
- **Dial-a-Frequency**™ Feature

Frequency Table (MHz)

S1	S0	CPU(0:1)	PCI(_F,0:5)
0	0	60	30
0	1	66.6	33.3
1	0	133.3	33.3
1	1	100	33.3

Table 1

Block Diagram

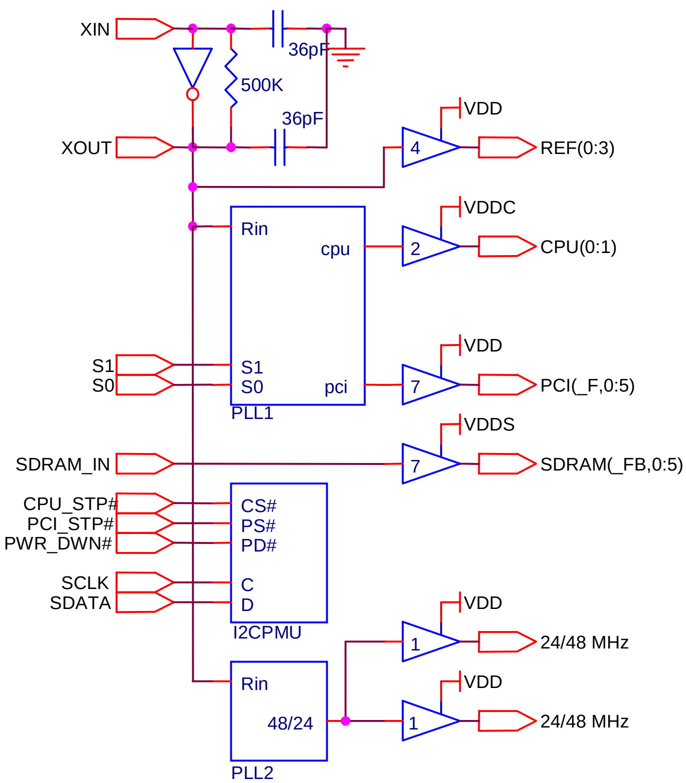
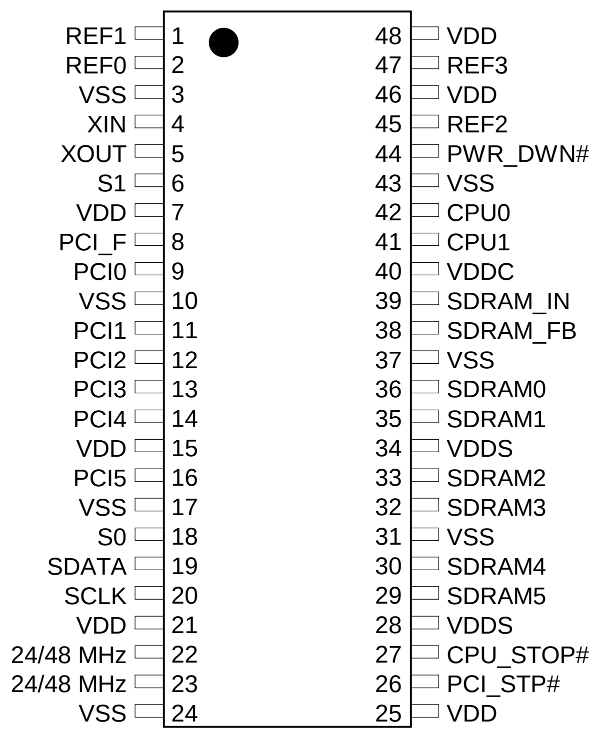


Fig.1

Pin Configuration



Pin Description

Pin No.	Pin Name	PWR	I/O	TYPE	Description
1,2,45, 47	**REF(0:3)**	VDD	O		Buffer output clocks of the reference signal at Xin.
4	**Xin**	VDD	I	OSC	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	VDD	O	OSC	On-chip reference oscillator output pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used at Xin, this pin remains unconnected.
6	**S1**		I	PD	Input for selecting CPU//PCI frequencies (see table 1,p.1).
18	**S0**		I	PU	Input for selecting CPU//PCI frequencies (see table 1,p.1).
8,9,11,12, 13,14,16	**PCI_F, PCI(0:5)**	VDD	O		PCI clock outputs, synchronous to the CPU clocks. If PCI_STP# is asserted low, PCI (0:5) stop in a low state, PCI_F does NOT.
19	**SDATA**	VDD	I/O	PU	Serial data input pin. Conforms to the Philips I2C specification of a Slave Receiver device. This pin is an input when receiving data. It is an open drain output when acknowledging. See I2C function description, p.5.
20	**SCLK**	VDD	I	PU	Serial clock input pin. Conforms to the Philips I2C 100KHz Specification.
22,23	**24/48M**	VDD	O		Programmable Peripheral clock outputs. Default to 48mhz for USB, but can be programmed to 24MHz through I2C bus.
26	**PCI_STP#**	VDD	I	PU	Input pin for stopping PCI (0:5) when active low. Default high. (see power management description p.3)
27	**CPU_STP#**	VDD	I	PU	Input pin for stopping CPU (0:1) when active low. Default high. (see power management description p.3). If Byte1, Bit2 and I^{2}C is low (0), then CPU0 DOES NOT STOP.
29,30,32, 33, 35, 36, 38	**SDRAM (FB,0:5)**	VDDS	O		SDRAM clock outputs. They are buffered outputs of the signal applied at SDRAM_IN, pin39.
41,42	**CPU(0:1)**	VDDC	O		Host (CPU) Clock outputs. See Table 1,p.1 for frequency selection.
44	**PWR_DWN#**	VDD	I	PU	Input pin for shutting down the device when asserted low. All outputs with the exception of SDRAM (FB,0:5), PLL's and crystal are stopped for minimum power consumption.
7,15,21,25 46, 48	**VDD**	-	P	-	3.3 Volt common power supply pins.
28,34	**VDDS**	-	P	-	3.3 Volt power supply pins for SDRAM_IN, SDRAM (FB, 0:5) outputs.
40	**VDDC**	-	P	-	3.3 or 2.5 Volt power supply pins for the CPU (0:1), outputs.
3,10,17, 24, 31, 37, 43	**VSS**	-	P	-	Common Ground pins.
39	**SDRAM_IN**	VDD	I	-	Input to SDRAM buffers.

Table 2

A bypass capacitor (0.1 uF) should be placed as close as possible to each Vdd, Vddc, and Vdds pins. If these bypass capacitors are not close to the pins, their high frequency filtering characteristic will be canceled by the lead inductance of the traces.

Power Management Functions

All clocks can be individually enabled or stopped via the 2-wire control interface. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped and on transitions from stopped to running when the chip was not powered down. On power up, the VCOs will stabilize to the correct pulse widths within about 0.5 mS. The CPU, SDRAM, and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

Pins 26 and 27 are inputs PCI_STOP# and CPU_STOP# respectively. A particular output is enabled only when both the serial interface and these pins indicate that it should be enabled. The device clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. On low to high transitions of PWR_DWN#, external circuitry should allow 0.5 mS for the VCOs to stabilize prior to assuming the clock periods are correct. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPU*	PCI	OTHER CLKs	XTAL & VCOs
X	X	0	LOW	LOW	LOW	OFF
0	0	1	LOW	LOW	RUNNING	RUNNING
0	1	1	LOW	Running	RUNNING	RUNNING
1	0	1	Running	LOW	RUNNING	RUNNING
1	1	1	Running	Running	RUNNING	RUNNING

Table 3

*If Byte1, bit2 is programmed to a "0", then CPU0 is not affected by CPU_STP#, and keeps running when CPU-STP# is asserted low.

Power Management Timing

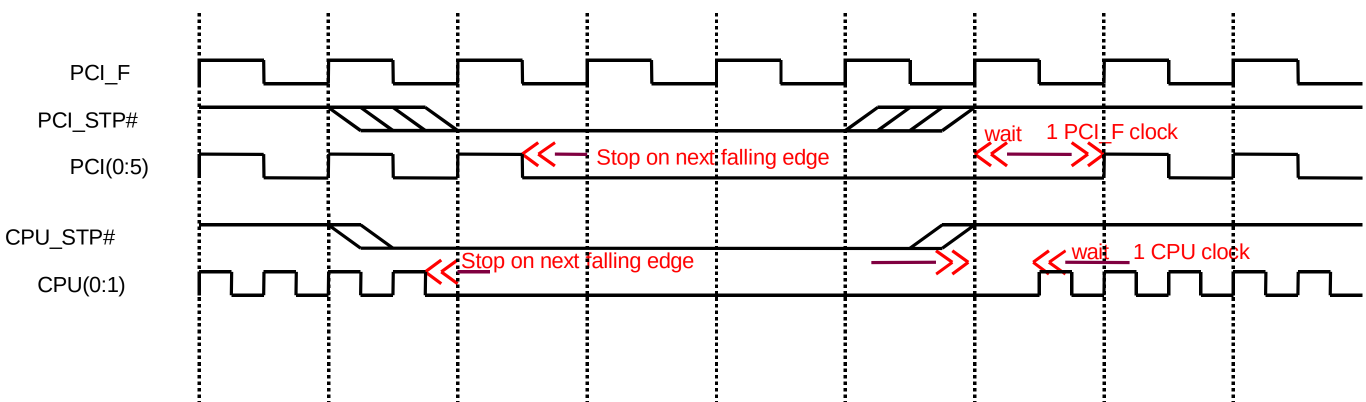


Fig.2

2-Wire I²C Control Interface

The 2-wire control interface implements a read/write slave only interface according to Philips I2C specification. (See fig3). The device can be read back by using standard I²C command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported. It also allows 24/48 MHz frequency selection and test mode enable as well as Spread Spectrum programmability.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit (R/W#) as the LSB. R/W# = 1 in read mode (see note1, below). R/W# = 0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. If the device should be read then an address **D3** must be sent. Data is transferred MSB first at a max rate of 100kbits/S. The device will not respond to any other control interface conditions, and previously set control registers are retained.

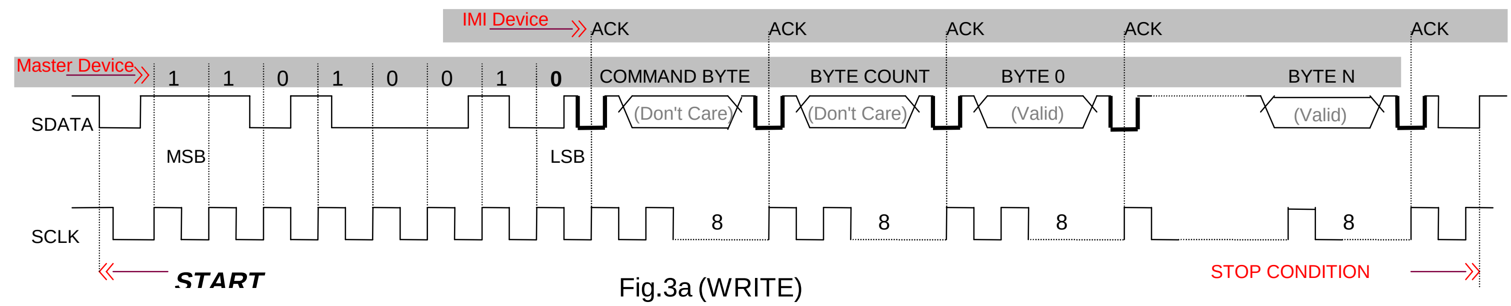


Fig.3a (WRITE)

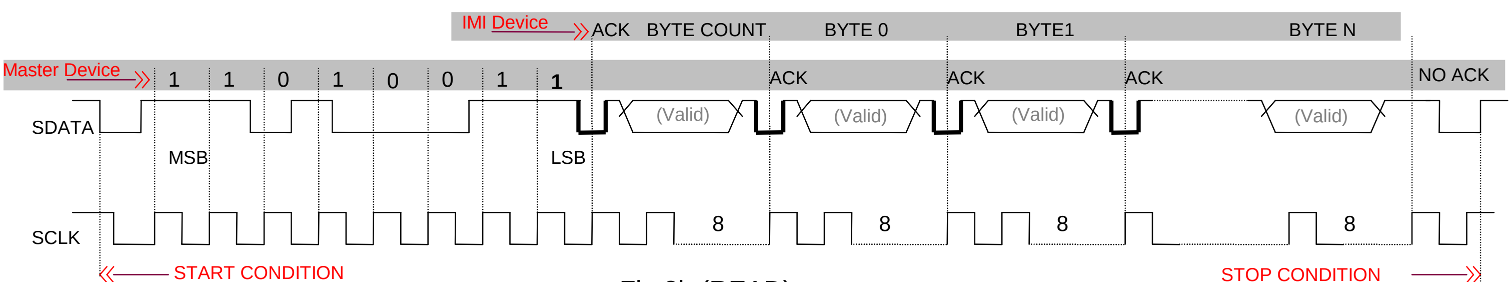


Fig.3b (READ)

Fig.3

Note1: Should the device be read, the address must be D3, therefore, the address' LSB is a 1 (for READ). After the device receives the address it will generate an acknowledge then immediately starts outputting data on the SDATA line. Data is transmitted following the Philips I2C standard. After each full byte is transmitted the device will wait for an acknowledge from the receiver before transmitting the next byte. The transmission will end when the device detects a Stop condition generated by the receiver.

Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.

Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

Byte 0: Function Select Register

Bit	@Pup	Pin#	Description
7	0	*	Reserved
6	1	*	SST2* (see table5, p.7)
5	1	*	SST1* (see table5, p.7)
4	1	*	SST0* (see table5, p.7)
3	1	22	24/48M, 1 selects 48mhz, 0 selects 24MHz.
2	1	23	24/48M, 1 selects 48mhz, 0 selects 24MHz.
1 0	0 0		Bit1 Bit0 1 1 Tri-State (all outputs) 1 0 ***Spread Spectrum enabled*** 0 1 Test Mode 0 0 NON spread spectrum operating mode

Byte 1: CPU, AGP, 48/24 MHz Register (1 = Enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	22	48/24 MHz Enable/Stopped
6	1	23	48/24 MHz Enable/Stopped
5	x	-	Reserved
4	x	-	Reserved
3	1	38	SDRAM_FB Enable/Stopped
2	1	39	If programmed to 0, CPU0 will be independent of CPU_STP# condition
1	1	41	CPU1 Enable/Stopped
0	1	42	CPU0 Enable/Stopped

Byte 2: PCI Register (1 = Enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	8	PCICLK_F Enable/Stopped
5	1	16	PCICLK5 Enable/Stopped
4	1	14	PCICLK4 Enable/Stopped
3	1	13	PCICLK3 Enable/Stopped
2	1	12	PCICLK2 Enable/Stopped
1	1	11	PCICLK1 Enable/Stopped
0	1	9	PCICLK0 Enable/Stopped

Serial Control Registers (Continued)

Byte 3: SDRAM Register (1 = Enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	26	Reserved
6	1	27	Reserved
5	1	29	SDRAM5 Enable/Stopped
4	1	30	SDRAM4 Enable/Stopped
3	1	32	SDRAM3 Enable/Stopped
2	1	33	SDRAM2 Enable/Stopped
1	1	35	SDRAM1 Enable/Stopped
0	1	36	SDRAM0 Enable/Stopped

Byte 4: SDRAM Register (1 = Enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

Byte 5: Peripheral Control (1 = Enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	1	47	REF3 Enable/Stopped
4	1	45	REF2 Enable/Stopped
3	x	-	Reserved
2	x	-	Reserved
1	1	1	REF1 Enable/Stopped
0	1	2	REF0 Enable/Stopped

*** SST (0:2) are soft select pins used for setting the Spread Spectrum width options. See Spread Spectrum description next section.**

Byte 6: Dial-a-Frequency™ Register

Bit	@Pup	Pin#	Description
7	0	-	N7, MSB
6	0	-	N6
5	0	-	N5
4	0	-	N4
3	0	-	N3
2	0	-	N2
1	0	-	N1
0	0	-	N0, LSB

Byte 7: Dial-a-Frequency™ Register

Bit	@Pup	Pin#	Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	R5
4	0	-	R4
3	0	-	R3
2	0	-	R2
1	0	-	R1
0	0	-	R0

Byte 8: Dial-a-Frequency™ Register

Bit	@Pup	Pin#	Description
7	0	-	Enable I2C N values
6	0	-	Enable I2C R values
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

Dial-a-Frequency™ Feature

I2C Dial-a-frequency feature is available in this device via bytes 6, 7 and 8.
These bytes allow the user to enter the N and R values that will enable them to program any CPU frequency desired following the formula:

$$Fcpu = \frac{P \times N}{R}$$ Equ.(1)

Where N and R values are programmed in binary into bytes 6 & 7 for N and byte 8 for R. See table below for min and max allowed values.

Dial-a-Frequency™ Feature (Cont.)

R	Min N	Max N
42	44	87
43	45	90
44	46	92
45	47	94
46	48	96
47	49	98
48	50	100
49	51	102
50	52	104
51	53	107

P is a large value PLL constant that depends on the last frequency selection achieved through the hardware selectors (S3, S2, S1, S0) or through the software selectors (byte0, bits7,6,5,4). P value may be determined from the following table:

S(3:0)	P
0000	32005333
0001, 1011	48008000
0010, 0011, 0101,1001, 1010	64010666
0110, 0111, 1000, 11xx	96016000

Therefore, if a 145MHz (use $145x10^6$)value is desired, then we should apply 145 into equation 1, and start by choosing R to be 47 (assume the last frequency selection has the value P = 96016000):

$$145X10^6 = \frac{96016000 \ X \ N}{47} \quad => \ N = 70.97775371$$

Since this N number must be entered in Binary, it can only be an integer, so it must be rounded up or down. Here we can rounded it up to 71, which will give us an exact CPU frequency of:

$$Fcpu = \frac{96016000 \ X \ N}{47} = 145.045 \text{ MHz (accuracy + 310 ppm)}$$

If the above frequency is not accurate enough, then you must choose another R value and start from the beginning. For example choose R = 49 and this will yield an N = 73.99808365, which is rounded to 74. If the 74 is applied in the formula 1, then Fcpu = 145.0038 MHz(accuracy + 26 ppm).

Other R values within the above limits may also be evaluated.

Reducing Clock Noise with Power Bypassing

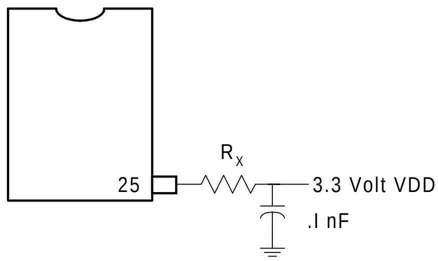


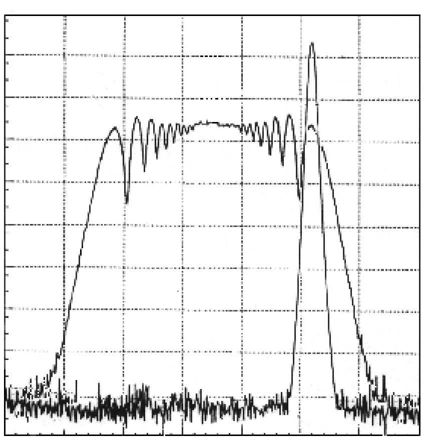
Figure 4

The C9806I produces many different frequency clocks simultaneously. If these clocks are allowed to couple back into the Internal Analog circuitry that may cause a destablizing noise injection condition. To eliminate this potential problem and produce the cleanest design and clock outputs, IMI recommends bypassing the 3.3V VDD supply to the Analog Power Pin (pin 25) with the circuitry shown in Figure 4. This will effectively isolate the device's Analog Power Supply from any noise that is present on it that will cause increased jitter and phase noise within it internal analog circuitry.

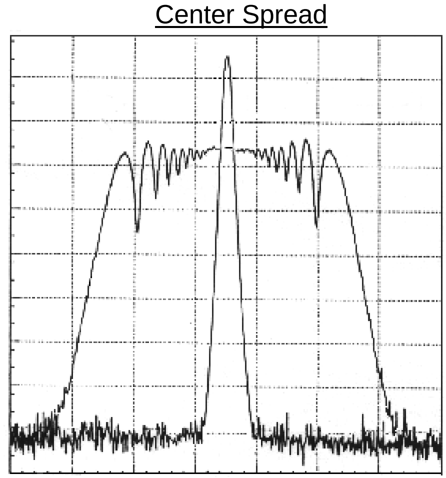
Spread Spectrum Clock Generation *(SSCG)*

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from or around the center of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting I2C byte0, bit1 = 1, and bit0 = 0. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have I2C accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SST (0:2) in I2C byte 0, bits 4, 5 & 6 following table 4 below.

Down Spread



Center Spread



Spread Spectrum Bandwidth Selection Table.

SST2	SST1	SST0	Bandwidth	Direction
0	0	0	+/- 0.75%	Center
0	0	1	+/- 0.5%	Center
0	1	0	+/-0.35%	Center
0	1	1	+/-0.25%	Center
1	0	0	-1.5%	Down
1	0	1	-1%	Down
1	1	0	- 0.7%	Down
1	1	1	- 0.5%	Down (default)

Table 4.

Maximum Ratings

Maximum Input Voltage Relative to VSS:	VSS - 0.3V
Maximum Input Voltage Relative to VDD:	VDD + 0.3V
Storage Temperature:	-65°C to + 150°C
Operating Temperature:	0°C to +85°C
Maximum ESD protection	2000V
Maximum Power Supply:	5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	S(0:1), PCI_STP#,
Input High Voltage	VIH	2.0	-	-	Vdc	CPU_STOP#, PWR_DWN#
Input Low Voltage	VIL	-	-	1	Vdc	SDATA
Input High Voltage	VIH	2.2	-	-	Vdc	SCLK
Input Low Current, Vin = VSS	IIL1			-66	µA	Pull-up at S1, PCI_STP#, CPU_STP#, PWR_DWN#
Input High Current, Vin = VDD	IIH1			5	µA	
Input Low Current, Vin = VSS	IIL2			5	µA	Pull-own at S0.
Input High Current, Vin = VDD	IIH2			66	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current, 3.3V	Idd3.3	-	-	185	mA	CPU = 100 MHz, Note 1
Dynamic Supply Current, 2.5V	Idd2.5	-	-	30	mA	CPU = 100 MHz, Note 1
Static Supply Current	Isdd	-	-	200	µA	PWR_DWN# = 0

Note 1: All outputs are loaded as per Table 5. CPU(0:1) outputs are measure at 1.25V. SDRAM (FB, 0:5), PCI(F,0:5), REF (0:2), 24/48M outputs are measured at 1.5V.

AC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Note 1,
CPU to PCI Offset	tOFF	1	-	4	nS	Note 1
Skew: (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	tSKEW1	-	-	175	pS	Note 1
∆Period Adjacent Cycles	∆P	-	-	250	pS	Note 1
VDD = VDDP = VDDF = VDDR = VDDA = 3.3V ± 5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

Note 1: All outputs are loaded as per Table 5. CPU (0:1) outputs are measured at 1.25V.
SDRAM (FB, 0:5), PCI (F, 0:5), REF (0:2), 24/48M outputs are measured at 1.5V.

Signal Name	Load, (max), pF
CPU(0:1), 24/48mhz, REF(0:2)	20
SDRAM(FB,0:5), PCI(_F,0:5)	30

Table 5

Buffer Characteristics for CPU (0:1),

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-15	-	-	mA	Vout =VDDC - 0.5V
Pull-Up Current	IOH_2	-30	-	-	mA	Vout = VDDC/2
Pull-Down Current	IOL_1	12	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	24	-	-	mA	Vout = VDDC/2
Rise/Fall Time, @ 0.4V-2.0V	Tr, Tf	0.4	-	1.3	nS	Note1

Buffer Characteristics for PCI(0:5, _F)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-14	-	-	mA	Vout =VDD - 0.5V
Pull-Up Current	IOH_2	-35	-	-	mA	Vout = VDD/2
Pull-Down Current	IOL_1	13	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	40	-	-	mA	Vout = VDD/2
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	2	nS	Note1

Buffer Characteristics for 24/48 MHz , REF(0:2)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-6	-	-	mA	Vout =VDD - 0.5V
Pull-Up Current	IOH_2	-15	-	-	mA	Vout = VDD/2
Pull-Down Current	IOL_1	6	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	22	-	-	mA	Vout = VDD/2
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	4	nS	Note1

Buffer Characteristics for SDRAM(0:5)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-20	-	-	mA	Vout =VDD - 0.5V
Pull-Up Current	IOH_2	-56	-	-	mA	Vout = VDD/2
Pull-Down Current	IOL_1	19	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	63	-	-	mA	Vout = VDD/2
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	1.3	nS	Note1
VDD = VDDS =3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

Note 1: All outputs are loaded as per Table 6. CPU(0:1) outputs are measure at 1.25V. SDRAM (FB, 0:5), PCI(F,0:5), REF (0:2), 24/48M outputs are measured at 1.5V.

Crystal and Reference Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	The crystal's rated load. Note 1
Effective Series resistance (ESR)	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	Note 1
Shunt Capacitance	CO	-	--	8	pF	Crystal's internal package capacitance (total)

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

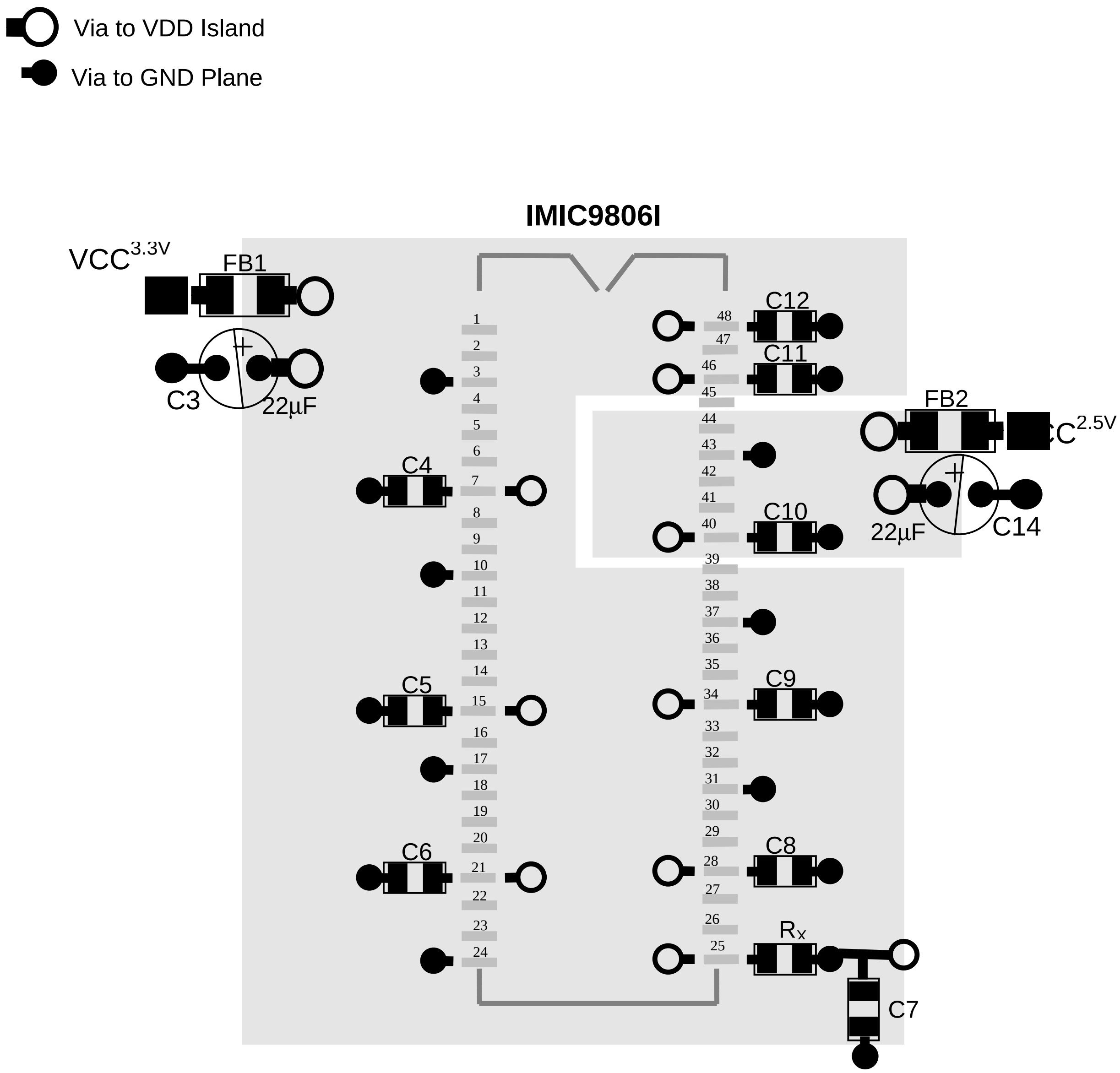
Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore = 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore = 18.0 pF

The total parasitic capacitance would therefore be = 20.0 pF.

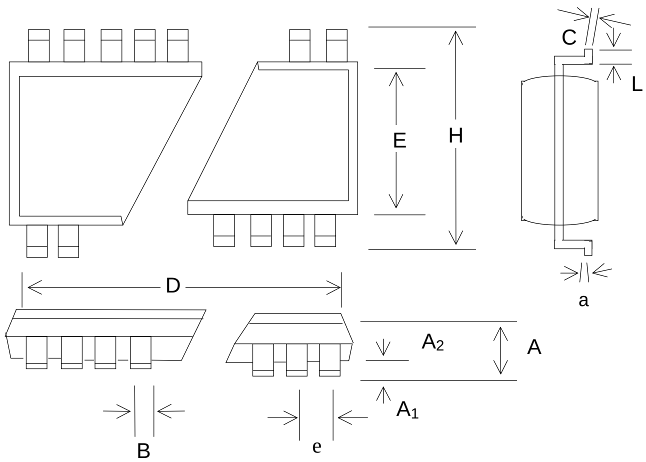
Note 1: It is recommended but not mandatory that a crystal meets these specifications.

PCB Layout Suggestion



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C4, C5, C6, C7, C8, C9, C10; C11and C12 (all are 0.1µf) should always be used and placed close to their VDD pins.

Package Drawing and Dimensions



48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

48 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.011	0.17	-	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.488	0.492	0.496	12.40	12.50	12.60
E	0.236	0.240	0.244	6.00	6.10	6.20
e	0.02 BSC			0.50 BSC		
H	0.315	0.319	0.323	8.00	8.10	8.20
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
IMIC9806IAY	48 PIN SSOP	Commercial, 0ºC to +70ºC
IMIC9806IAT	48 PIN TSSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
C9806IAY
Date Code, Lot #

IMIC9806IAY

Package
Y = SSOP
T = TSSOP

Revision

IMI Device Number

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