C9714-I

100 MHz Clock Generator with SSCG and Power Management for Mobile Application

Preliminary

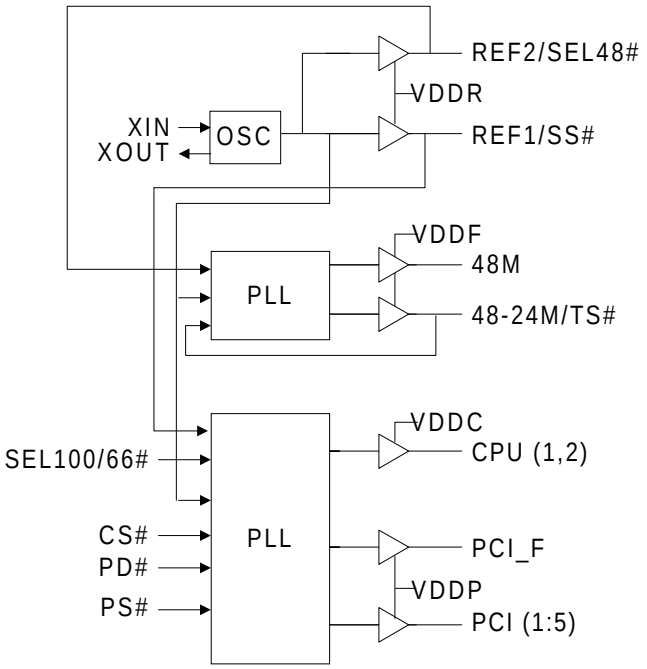
Product Features

- Supplies:
- 2 Ref clocks
  2 Host (CPU) clocks
- 1 free running and 5 PCI Clocks
- 1 48MHz fixed clock
- 1 48 or 24 MHz fixed clock
- Separate supply pins for mixed (3.3/2.5V) voltage application.
- 100 or 66 MHz CPU clock operation
- Spread Spectrum modulation for reducing EMI
- Rich Power Management Functions.
- 28-pin SSOP & TSSOP packages for minimum board space.

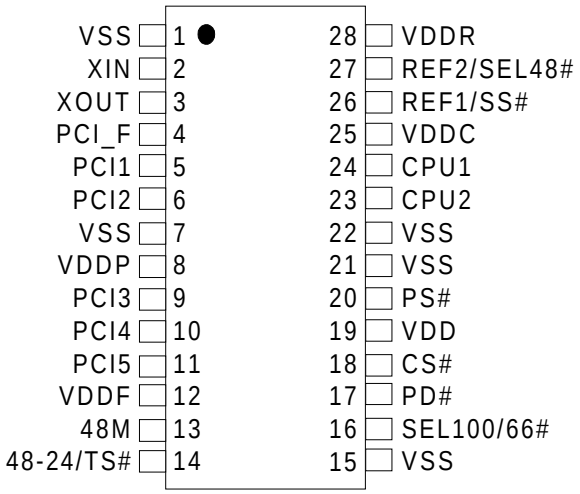
Frequency Table

SEL 100/66#	CPU Clock	PCI Clock
0	66.66 MHz	33 MHz
1	100.00 MHz	33 MHz

Block Diagram



Pin Configuration



Pin Description

PIN No.	Pin Name	PWR	I/O	Description
2	XIN	VDD	I	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
3	XOUT	VDD	O	O-chip reference oscillator output pin. Drives an external parallel resonant crystal (14.318 MHz) when an externally generated reference signal is used.
19	VDD	-	P	3.3 volt power supply for core logic.
23, 24	CPU (1,2)	VDDC	O	Clock outputs. CPU frequency table specified on page 1.
17	PD#	-	I	Powers down device when LOW
18	CS#	-	I	When signal is LOW, stops CPU clocks in low state.
16	SEL100/66#	-	I	Frequency select input pins. See frequency select table on page 1. NO INTERNAL PULLUP RESISTOR IS PROVIDED BY DEVICE
25	VDDC	-	P	2.5V power for CPU and Host clock outputs.
4	PCI_F	VDDP	O	Free running PCI clock 3.3V. Does not stop when PS# is at a logic LOW level
5,6,9, 10,11	PCI(1:5)	VDDP	O	PCI output clocks. See frequency table of page 1.
20	PS#	-	I	When signal is LOW, stops all PCI clocks (except PCI_F) in low state.
8	VDDP	-	P	3.3 Volt power supply pins for free running PCI clock output buffer.
13	48M	VDDF	O	Fixed 48 MHz clock.
14*	48-24M/TS#	VDDF	I/O	Power up selectable 48 or 24 MHz clock. See Pin 27 for description. If strapped LOW at powerup causes the all output clocks to be placed in a tri-state condition until the next power up sequence occurs.
26	REF1/SS#	VDDR	I/O	At power up this pin determines if the device's spread spectrum modulation feature is enabled or disabled. After power up this pin becomes a reference clock output. A 0 (logic low) enables SSCG and a 1 (logic high) disables SSCG.
27*	REF2/SEL48#	VDDR	I/O	At power up this pin determines the frequency of the clock at pin 14. If it is LOW, the clock will be 48 MHz, if HIGH the clock will be 24 MHz. After power up this pin will become a reference clock output.
12	VDDF	-	P	Power for fixed clock output buffer.
1, 7, 15, 21, 22	VSS	-	P	Ground pins for device.
28	VDDR	-	P	Power for Reference Oscillator output buffer.

Notes

1. All pin numbers followed by the * symbol have internal pullup resistors that will guarantee to a logic 1 (high) level if no connection is made to the device's pin. INP3 pins do not contain this function and must be electrically connected to VDD or VSS by external circuitry to ensure a valid logic 1or 0 is sensed.

Frequency Selection Table

	Outputs					
Descriptions	**48-24M/TS# at Power UP**	**SEL 66/100**	**CPU**	**PCI, PCI_F**	**48M**	**48/24M**
All Outputs Tri-State	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
66 MHz	1	0	66.66 MHz	33.33 MHz	48 MHz	24/48 MHz
100 MHz	1	1	100.00 MHz	33.33 MHz	48 MHz	24/48 MHz

Power Management Functions

PS#	CS#	PD#	CPU	48M	PCI	PCI_F	VCOs
X	X	0	LOW	LOW	LOW	LOW	OFF
1	0	1	LOW	ON	ON	ON	ON
0	1	1	ON	ON	LOW	ON	ON
0	0	1	LOW	ON	LOW	ON	ON
1	1	1	ON	ON	ON	ON	ON

CS# is used to turn off the CPU clocks for power management. CS# is an asynchronous external CPU clock control signal. It is internally synchronized to the device's PCI_F clock (see the Power Management Function Section of this data sheet for the specific timing). All other clocks are running while the CPU clocks are disabled. The CPU clocks are always stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. CPU clock on latency is **2 or 3 CPU clocks** periods in time and CPU clock off latency is **2 or 3 CPU clocks** periods in time.

Power Management Functions

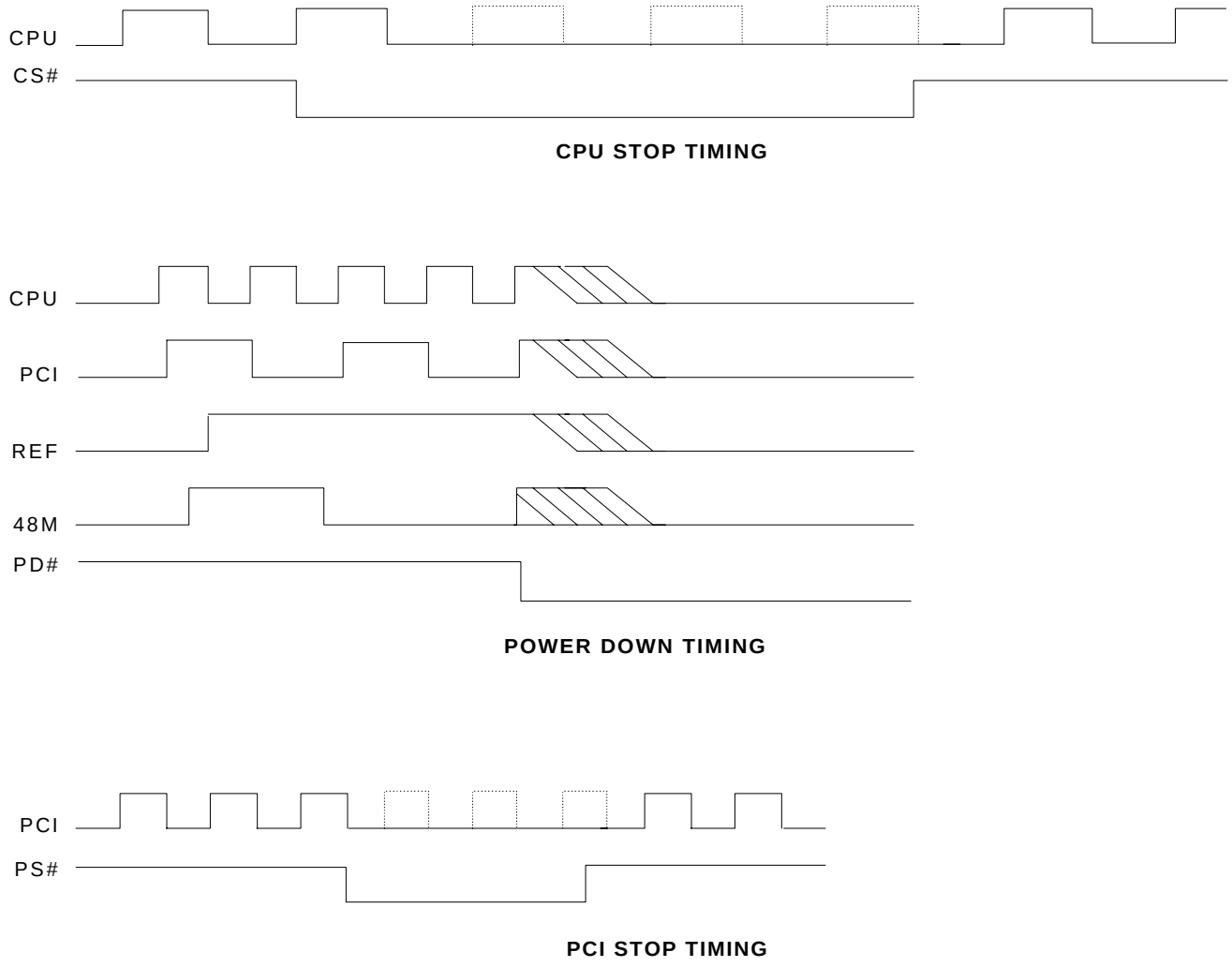


Fig. 1

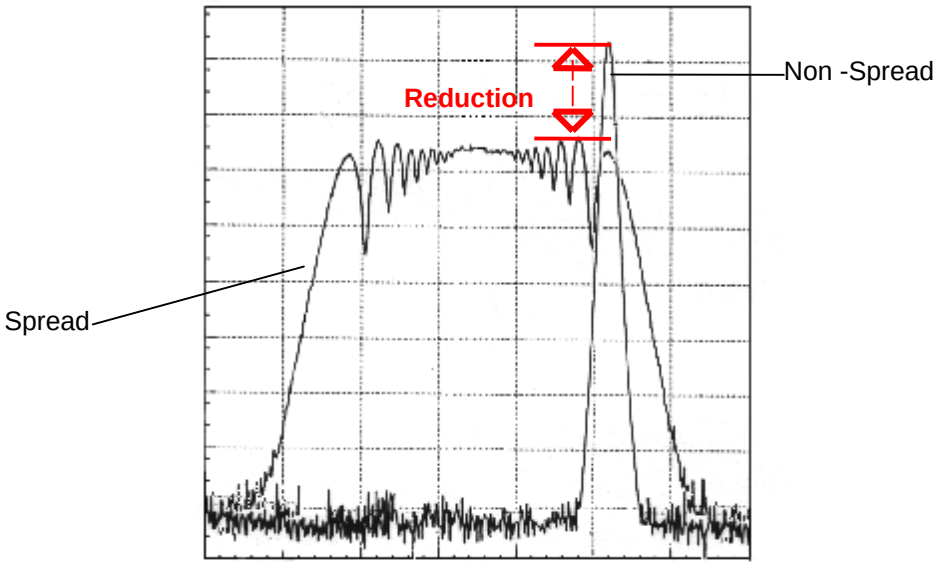
The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PD# is active low, all clocks need to be driven to a low value and held prior to turning off the VCO's and the Crystal. The power-up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. AS# and CS# are considered to be don't cares during the power down operations.

Power Management Timing

		Latency
Signal	**Signal State**	**No. of rising edges of free running PCI CLOCK (PCIF)**
CS#	0 (disabled)	1
	1 (enabled)	1
PD#	1 (cold start/normal operation)	3 mS
	0 (power down)	1

NOTES:
1. Clock on/off latency is defined in the number of rising edges of free running PCI CLOCK between the clock disable goes low/high to the first valid clock comes out of the device.

Spectrum Spread Clocking

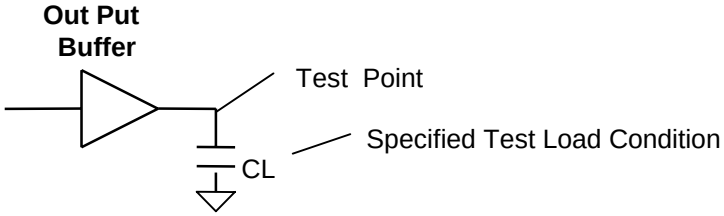


Spectrum Analysis

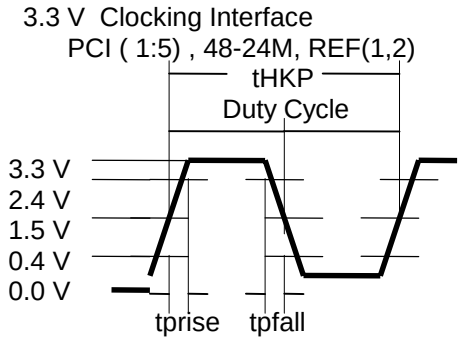
Spectrum Spreading Selection Table

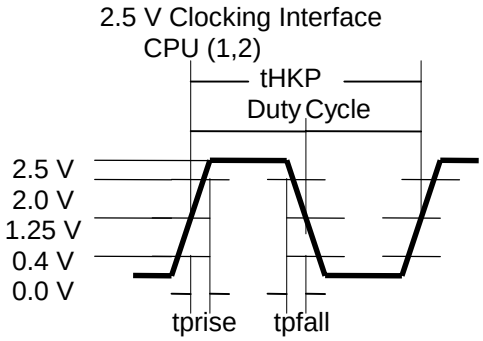
Min (MHz)	Center (MHz)	Max (MHz)	CPU Frequency	% OF FREQUENCY SPREADING	MODE
99.3	99.65	100	100.00	.7% (-.7% + 0%)	Down Spread
66.13	66.37	66.6	66.66	.7% (-.7% + 0%)	Down Spread

Test and Measurement Condition



Clock Output Wave form





Absolute Maximum Ratings

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0ºC to + 125ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin should be constrained to the range:

VSS<(Vin)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	
Input High Voltage	VIH	2.0	-	-	Vdc	
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Output Low Voltage IOL = 4mA	VOL	-	-	0.4	Vdc	All Outputs (see buffer spec)
Output High Voltage IOH = 4mA	VOH	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Tri-State leakage Current	Ioz	-	-	10	µA	TS# = 0
Dynamic Supply Current	$Idd2_{66}$	-	-	25	mA	TS# = 1, 100/66 = 0, CS# = 1, PD# = 1
(2.5 Volt Supply)	$Idd2_{100}$	-	-	25	mA	TS# = 1, 100/66 = 0, CS# = 1, PD# = 1
Dynamic Supply Current	$Idd3_{66}$	-	-	120	mA	TS# = 1, 100/66 = 1, CS# = 1, PD# = 1
(3.3 Volt Supply)	$Idd3_{100}$	-	-	120	mA	TS# = 1, 100/66 = 1, CS# = 1, PD# = 1
Power Down Mode	$I2.5_{PD}$	-	-	50	µA	PD# at logic low level
Power Down Mode	$I3.3_{PD}$	-	-	4.5	mA	PD# at logic low level
VDD = VDDF = VDDP=VDDR =3.3V ±5***%, VDDC = 2.5V*** ±5***%,, TA = 0ºC to +70ºC***						

AC Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	CPU and CPU/2 = Measured at 1.25V all others measured at 1.50V
CPU to PCI Offset	tOFF	1	-	4	ns	CPU = 20 pF load Measured at 1.25V PCI = 30 pF load Measure at 1.50V
Buffer out Skew All CPU and PCI Buffer Outputs	tSKEW	-	-	250	ps	CPU = 20 pF load Measured at 1.25V PCI = 30 pF Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	CPU
ΔPeriod Adjacent Cycles	ΔP	-	-	± 500	pS	PCI Only
VDD = VDDF = VDDP =VDDR =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

AC Skew Requirements

Characteristic	Bank Skew	Cycle to Cycle Jitters	VDD	Skew, Jitters Measure Point
CPU	175pS	250pS	2.5V	1.25V
48 MHz	n/a	500pS	3.3V	1.5V
PCI, PCI_F	500pS	500pS	3.3V	1.5V
Ref	n/a	500pS	3.3V	1.5V

Offset Requirements

Characteristic	Bank Offset	Measurement Loads (lumped)	Measure Points
CPU to PCI, PCI-5	1.5-4.0nS CPU leads	CPU @ 20pF, PCI @ 30 pF	CPU @ 1.25V, PCI @ 1.5V

DC Buffer Characteristics for CPU Outputs

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-82	-		mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}			-67	mA	Vout = 2.375 V
Pull-Down Current Min	IOL_{min}	81	-	-	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	60	mA	Vout = 0.3 V
Rise Time Between 0.4 V and 2.4 V	TR	0.4	-	1.6	nS	20 pF Load
Fall Time Between 0.4 V and 2.4 V	TF	0.5	-	1.6	nS	20 pF Load
VDD = VDDF = VDDP = VDDR =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

DC Buffer Characteristics for 48M, 48-24M and REF Outputs

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-29	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-23	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	29	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.4 V
Rise Time Between 0.4 V and 2.4 V	TR	0.5	-	2.0	nS	20 pF Load
Fall Time Between 0.4 V and 2.4 V	TF	0.5	-	2.0	nS	20 pF Load
VDD = VDDP= VDDR =3.3V ±5***%, VDDC = 2.5V*** ±5***%,, TA = 0ºC to +70ºC***						

DC Buffer Characteristics for PCI_F, PCI (1:5)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-33	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-33	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	30	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	38	mA	Vout = 0.4 V
Rise Time Between 0.4 V and 2.4 V	TR	0.5	-	2.0	nS	30 pF Load
Fall Time Between 0.4 V and 2.4 V	TF	0.5	-	2.0	nS	30 pF Load
VDDP= VDDR =3.3V ±5***%, VDDC = 2.5V*** ±5***%,, TA = 0ºC to +70ºC***						

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	14.17	14.31818	14.46	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
Frequency Stability	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exibit oscillator startup problems

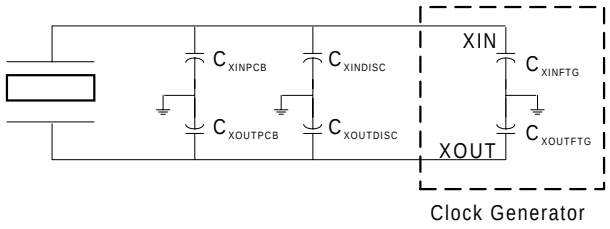
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit trace capacitance (C_{PCB}), and any onboard discrete load capacitance (C_{DISC}).

The following formula and schematic illustrates the application of the loading specification of a crystal (C_{XTAL})for a design.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

C_{XTAL} = the load rating of the crystal
$C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
$C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
$C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
$C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
$C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground

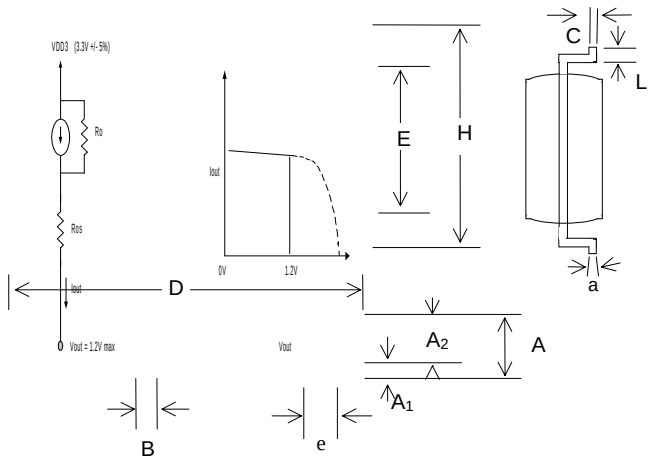


As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 4pF (typical value) would calculate as:

$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF

Package Drawings and Dimensions (28 Pin SSOP and TSSOP)



28 Pin SSOP Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.025 BSC			0.635 BSC		
H	0.301`	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

28 Pin TSSOP Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
L	0.018	0.023	0.030	0.45	0.60	0.75
b	0.007	-	0.012	0.19	-	0.30
c	0.004	-	0.008	0.09	-	0.20
θ	0°	-	8°	0°	-	8°
e	0.026 BSC			0.65 BSC		
D	0.378	0.382	0.386	9.6	9.7	9.8
E	0.169	0.173	0.177	4.3	4.4	4.5

Preliminary

Ordering Information

Part Number	Package Type	Production Flow
IMIC9714-IY	28 PIN SSOP	Commercial, 0ºC to +70ºC
IMIC9714-IT	28 PIN TSSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI, Date Code
C9714-I
Lot #

IMIC9714-IY

Package
Y = SSOP
T = TSSOP

IMI Device Number