IMI145158

SERIAL PROGRAMMED PLL FREQUENCY SYNTHESIZER

Approved Product

Product Description

The IMI145158 is a member of a family of phaselock loop synthesizer ICs from International Microcircuits. This part is a single PLL in a small package for low cost VHF applications. The IMI145158 is programmed with standard 3-wire serial lines: data, clock, and enable.

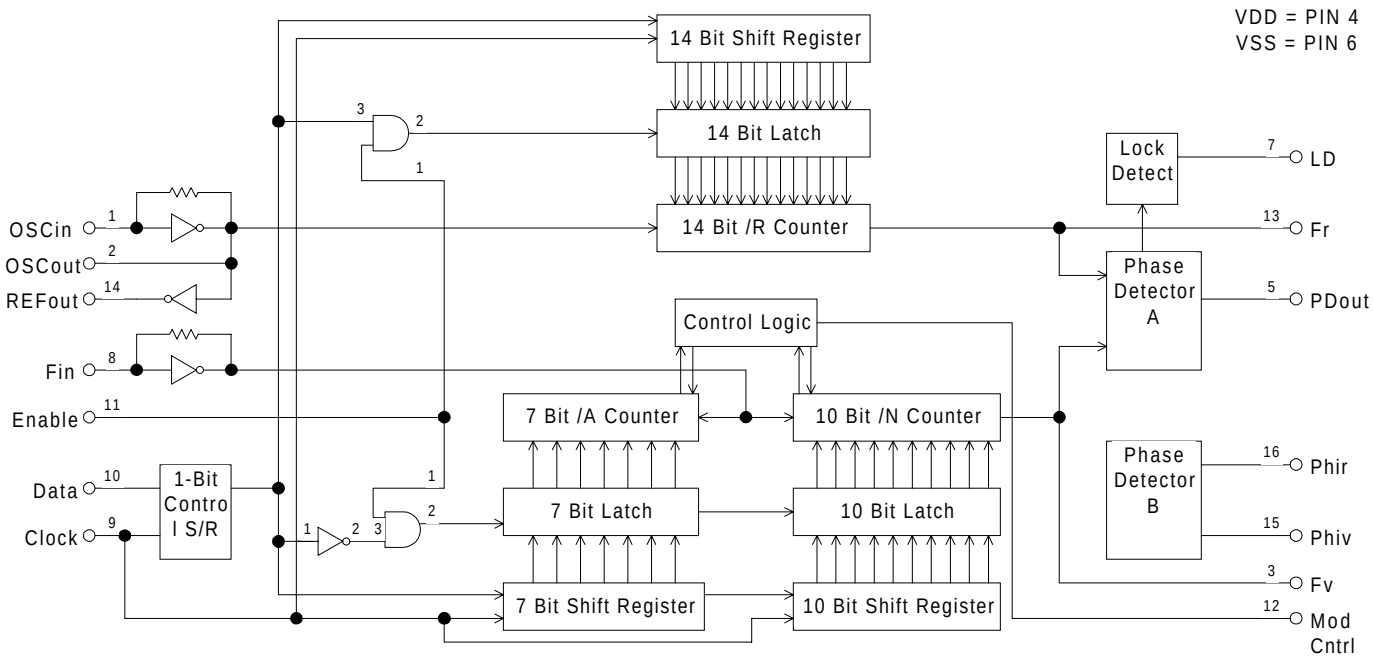
Blocks in the IMI145158 include a dual modulus feedback divider for control of an external dual modulus prescaler. Prescaler ratios up to 128:129. Also included are an "N" counter, reference divider, phase detector, and charge pump. The reference divider is programmable from 1 to 16383. Both divider inputs are biased for high sensitivity to sinewave input signals, and the reference divider input can be configured to operate as a crystal oscillator if desired. A buffered reference signal output is also provided. The phase detector is a Type IV phase-frequency design, which has inherently eliminated the "dead zone" crossover distortion. The loop error signal is provided by both a single-ended charge pump output and standard differential logic outputs.

Performance improvements of the IMI145158 over other single loop CMOS PLL devices are in the operating bandwidth and phase detector noise floor. With its extremely low phase noise floor and wider input bandwidth, prescaler ratios can be minimized to allow wide loop bandwidths for faster settling and lower phase noise.

Product Features

- >145 MHz typical input frequency.
- -160 dBc/Hz total phase detector noise floor.
- No dead zone by design.
- Two phase detector outputs:
  - Current mode charge pump
  - Differential logic
- Unambiguous PLL acquisition.
- 3-line serial programming: data, clock, & enable.
- Compatible with the SPI (Serial Peripheral Interface) on CMOS MCUs.
- 10-bit N counter: Divider range = 1 to 1023.
- 7-bit A counter: Divider range = 0 to 127.
- 14-bit R counter: Divider range = 1 to 16383.
- On- or off-chip reference oscillator operation.
- Buffered & filtered ref output is provided.
- 16 Pin SOIC package

Block Diagram



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Maximum Ratings

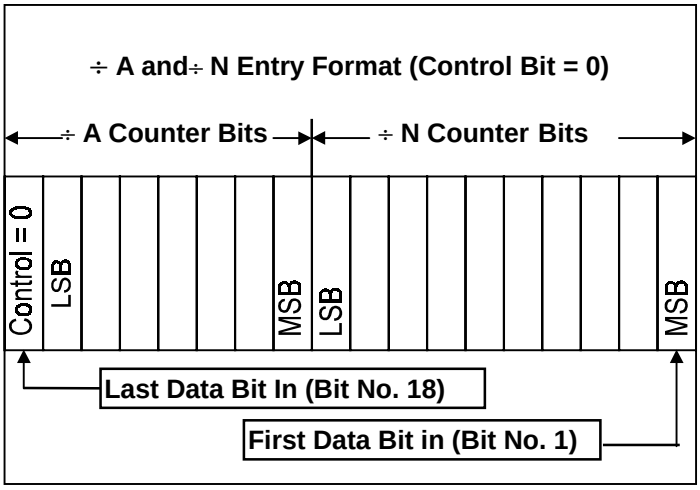
Voltage Relative to VSS:	-0.3V to 7V
Voltage Relative to VDD	0.3V
Storage Temperature:	-65ºC to 150ºC
Ambient Temperature:	-40ºC to 85ºC

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)< VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

Pin Description

Pin Number	Name	Description
1	Xin	Xtal in (or reference signal input) to the reference oscillator / buffer.
2	Xout	Xtal out (or Reference signal output) of the reference oscillator / buffer.
14	REFout	Buffered reference signal.
10	DATA	Positive logic shift register input data. The first 14 bits are the reference or feedback divider programming information, sent MSB first. The final programming bit (control bit) selects which divider this programming information will be loaded into: 1 = the reference divider, and 0 = the feedback divider. 

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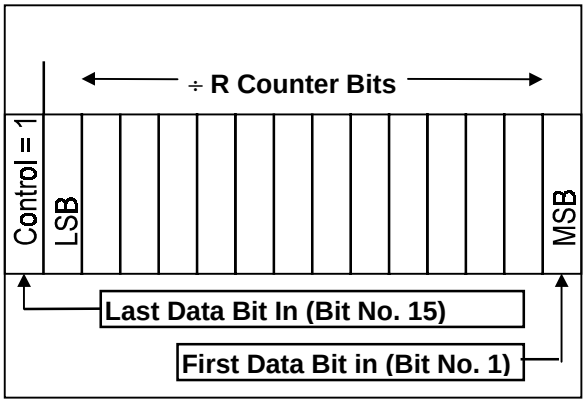
Pin Description (Cont.)

Pin Number	Name	Description
		
9	CLOCK	On each low-to-high transition, clocks one bit into the on-chip shift register from the data input.
11	ENABLE	This signal, when HIGH, latches the information in the shift register into the selected divider.
12	Mod Cntrl	This output generates a signal by the on-chip control logic circuitry for controlling an external dual-modulus prescaler.
8	fin	Feedback divider input signal. Applied to the positive edge triggered counter, this signal is intended to be AC coupled. For CMOS logic level input signals, DC coupling can be used.
4	VDD	Circuit positive power supply.
6	VSS	Circuit ground.
5	PDout	Single-ended charge pump output, usually used with passive loop filters. This signal operated according to this table: ■ Frequency fv > fr at the phase detector: negative pulses. ■ Frequency fv < fr at the phase detector: positive pulses. ■ Frequency fv = fr at the phase detector: high-impedance state.
16	ϕR	Phase detector output. This signal goes LOW when the feedback frequency is too low.
15	ϕV	Phase detector output. This signal goes LOW when the feedback frequency is too high.
7	LD	Lock detect output. When the PLL is locked, this signal will be essentially HIGH, with very narrow negative spikes at the phase detection frequency. If the PLL is out of lock, this signal will pulse LOW.
3	fv	Output of the feedback divider N.
13	fr	Output of the reference divider R.

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PLL Operating Characteristics

VDD = 5 VOLTS												
				-40ºC		25ºC			85ºC			
Characteristics		Symbol		Min	Max	Min	Typ	Max	Min	Max	Unit	Conditions
Dynamic	Max Operating Frequency	fin, fosc	Sine*	160	typ 225	120	170		110	typ 155	MHz	+ 4 dBm 1.0V p-p
			Sine*	75	typ 105	85	120		55	typ 80	MHz	+4 of Bm 1.0 V p-p
	Modulus Control Prop. Delay	MCpd		-	10	-	7.5	10.5	-	12	ns	
	Synthesizer Phase Noise Floor	PDNF					-160				dBc/Hz	@100kHz
	Pin Capacitance	Cin		-	6	-	4	6	-	6	pF	
		Cout		-	8	-	6	8	-	8	pF	
	Phase Det 1 gain	Kd		-		-	0.65		-		ma/Rad	
	Phase Det 2 gain	Kd		-		-	0.8		-		v / Rad	
Static	Input Voltages	VIL			1.5	-		1.5	-	1.5	Vdc	Pins 1, 8 and 10
		VIH		3.5	-	-	3.5	-	3.5	-		
	Input Voltage	Vil		-	0.6	-	-	0.6	0.6	0.6	Vdc	Pins 9 and 11
		VIH		4.2	-	4.2`	-	-	4.2	-		
	Output Voltages	VOL		-	0.05	-	0.0	0.05	-	0.05	Vdc	Iout = 0
		VOH		4.95	-	4.95	5.0	-	4.95	-		
	Output Current	IOL	Logic	2.4	-	2.0	2.8	-	1.6	-		
			OSCout	1.2	-	1.0	1.4	-	0.8	-	mA	VOL = 0.40
		IOH	Logic	-2.4	-	-2.0	-2.8	-	-1.6	-	mA	VOH = 4.0
			OSCout	-1.2	-	-1.0	-1.4	-	-0.8	-	mA	VOH = 4.4
		Icp	CPcur				4.0				mA	for 2Pi Radians
	Supply Currents	IDD			7.0			7.0		7.0	mA	R=128, N=128, A=32
		ISB		-	150	-	40	150	-	150	µA	fosc=fin=0
		IPU					50				µA	VIL = 0

* Sine wave input is not recomended below 10 MHz.

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PLL Operating Characteristics

VDD = 3 VOLTS												
				-40ºC		25ºC			85ºC			
Characteristics		Symbol		Min	Max	Min	Typ	Max	Min	Max	Unit	Conditions
Dynamic	Max Operating Frequency	fin,	Sine*	100		80	115		70		MHz	+4 dBm 1.0V p-p
		fosc	Sine*	60		65	95		50		MHz	+4 dBm 1.0V p-p
	Modulus Control Prop. Delay	MCpd		-	12	-	11	15	-	17	ns	
	Synthesizer Phase Noise Floor	PDNF					-160				dBc/Hz	
	Pin Capacitance	Cin		-	10	-	6	10	-	10	pF	
		Cout		-	10	-	6	10	-	10	pF	
	Phase Det 1 gain	Kd		-		-	0.35		-		ma/Rad	
	Phase Det 2 gain	Kd		-		-	0.48		-		v / Rad	
Static	Input Voltages	VIL		-	0.9	-	-	0.9	-	0.9	Vdc	Pins 1, 8 and 10
		VIH		2.1	-	2.1	1.65	-	2.1	-		
	Input Voltages	VIL		-	0.4	-	-	0.4	-	0.4	Vdc	Pins 9 and 11
		VIH		2.5	-	2.5	-	-	2.5	-		
	Output Voltages	VOL		-	0.05	-	0.0	0.05	-	0.05	Vdc	Iout = 0
		VOH		2.95	-	2.95	3.0	-	2.95	-		
	Output Current	IOL	Logic	1.6	-	1.4	2.0	-	0.8	-		
			OSCout	0.8	-	0.7	1.0	-	0.4	-	mA	VOL = 0.30
		IOH	Logic	-1.6	-	-1.4	-2.0	-	-0.8	-	mA	VOH = 2.4
			OSCout	-0.8	-	-0.7	-1.0	-	-0.4	-	mA	VOH = 2.4
		Icp	CP cur				2.2				mA	for 2Pi Radian
	Supply Currents	IDD			3.0			3.0		3.0	mA	R=128, N=128, A =32
		ISB		-	150	-	40	150	-	150	µA	fosc=fin=0

* Sine wave input is not recommended below 10 MHz.

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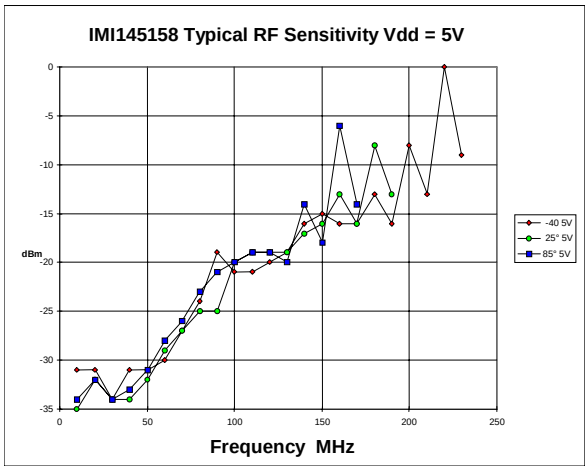

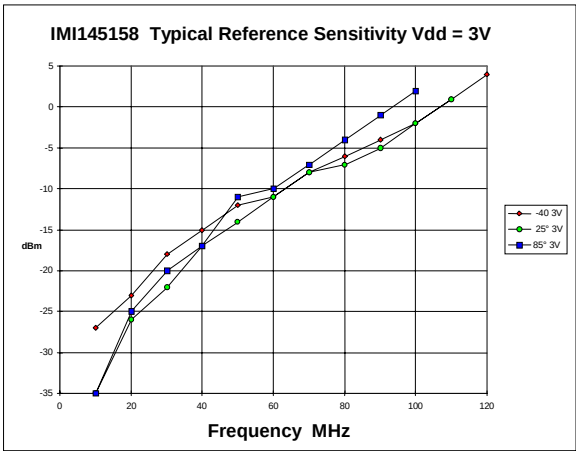

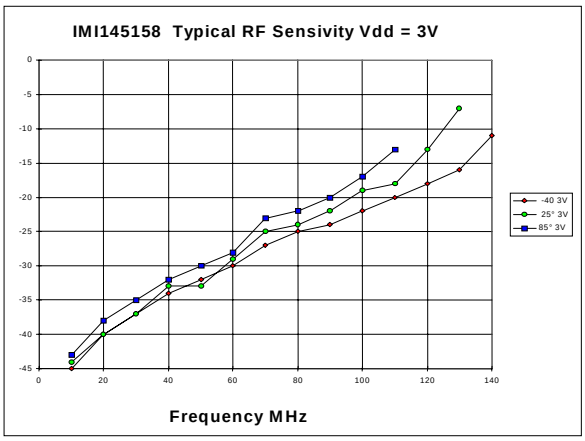

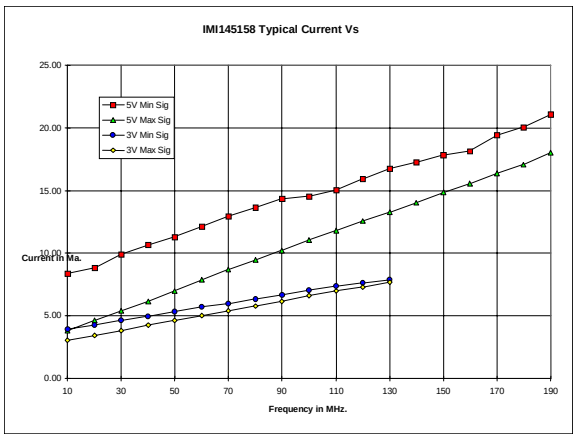

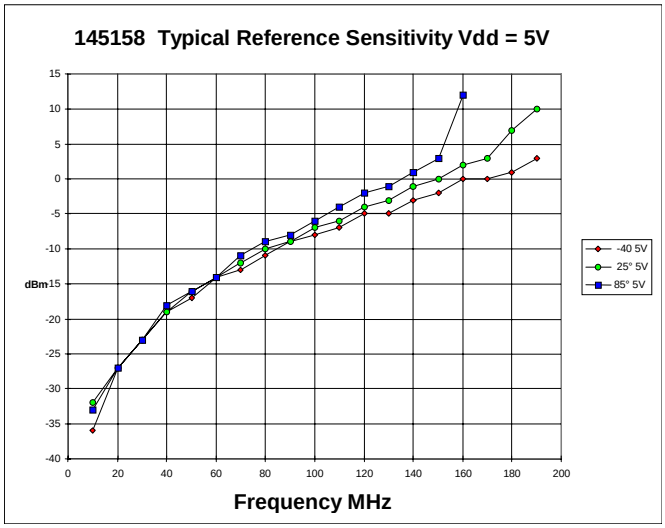

Dual Modulus Prescaling

Dual Modulus prescaling is a wide spread method used to effectively extend the operating frequency of a digital counter without sacrificing any frequency resolution. The key to understanding this method is to remember the basics of division: When any two integers are divided, a quotient and a remainder will result.

When used here in a PLL, the numerator is the required PLL total feedback divider ratio, called $N_{tot.}$ The denominator is the base modulus of the dual modulus prescaler, P. The quotient is applied directly to the N counter, and the remainder is applied directly to the A counter. Both counters count down together toward zero. While the A counter counts, the MC (modulus control) output signal is LOW, setting the prescaler to divide by P + 1. When the A counter reaches zero, the MC output is set HIGH while the N counter continues to count down to zero. When the N counter reaches zero, both counters are reset to the programmed inputs and the cycle is repeated.

Two particular things should be noticed about this process. First, the remainder counts are spread among an equal number of quotient counts by the use of the prescaler modulus P +1. When the remainder has been counted, any remaining quotient counts are handled normally by prescaling by modulus P. This counter is thus performing

$$N_{tot} = A(P+1) + (N-A)P$$

Some algebra on this relation yields

$$N_{tot} = AP+A + NP-AP$$
$$= NP + A$$

which is just the definition of integer division. Second, for this to work, there must be more quotient counts than remainder counts for all possible values of N_{tot} in the synthesizer design. If this were not true, then the N counter will reach zero and cause the entire divider to be reset before the A counter is finished. There is a minimum value for N_{tot} for which this requirement will always hold:

$N_{tot} > P^2 - P.$

Programming Guidelines

The system total divide value (N_{total}) will be dictated by the application:

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N*P+A$$

N is the number programmed into the ÷ N counter; A is the number programmed into ÷ A counter. P and P + 1 are two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷ A counter is programmed from zero through P-1 for a particular value N in the ÷ N counter. N is then incremented to N + 1k, and the ÷ A is sequenced from zero through P - 1 again.

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high, and by P + 1 when its modulus control is low.

For the maximum frequency into the prescaler (FVCO max), the value used for P must be large enough so that:

A. FVCO max divided by P may not exceed the frequency capability of Pin 8 of the IMI145158.
B. The period of FVCO divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control signal.

A useful simplification in the IMI145158 programming code can be achieved by choosing the values for P or 8, 16, 32, or 64, or 128. For these cases, the desired value for N_{total} in binary is used as the program code to the ÷ A counters in the following manner:

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Programming Guidelines (Cont.)

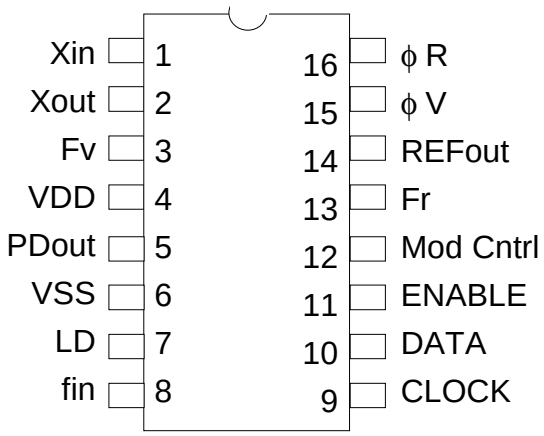
A. Assume the ÷ N counter and ÷ A counter contains "b" bits where 2b = P.

B. Always program all higher order ÷ A counter bits above "b" to zero.

C. Assume the ÷ N counter and ÷ A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10+b bits in length. The MSB of this hypothetical counter is to correspond o the LSB of ÷ A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "new" 10+b bit counter.

Connection Diagram:

SOIC Package



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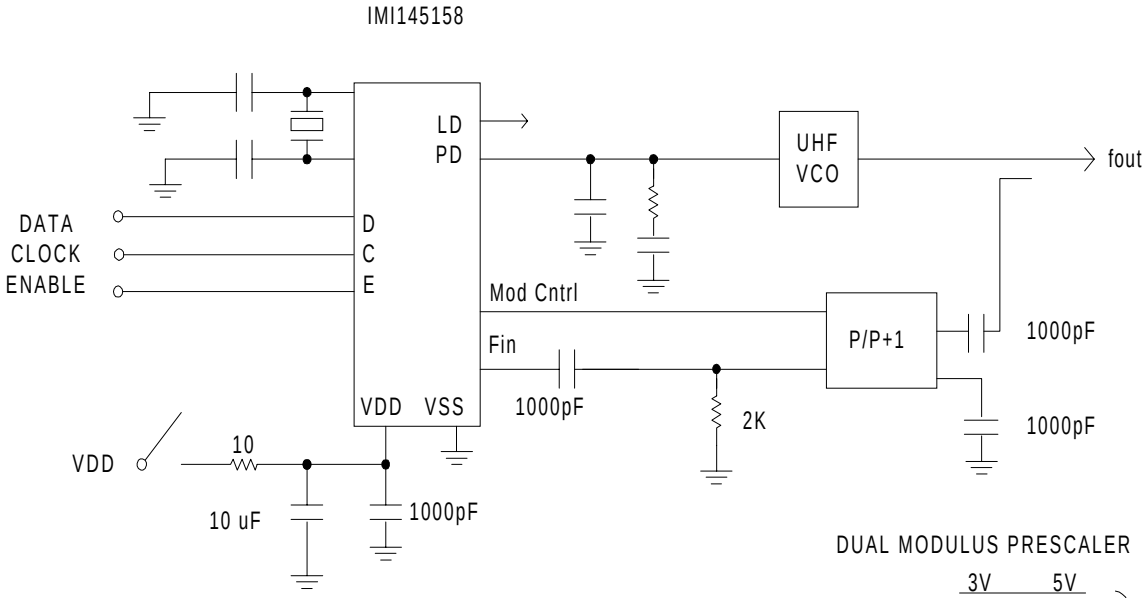
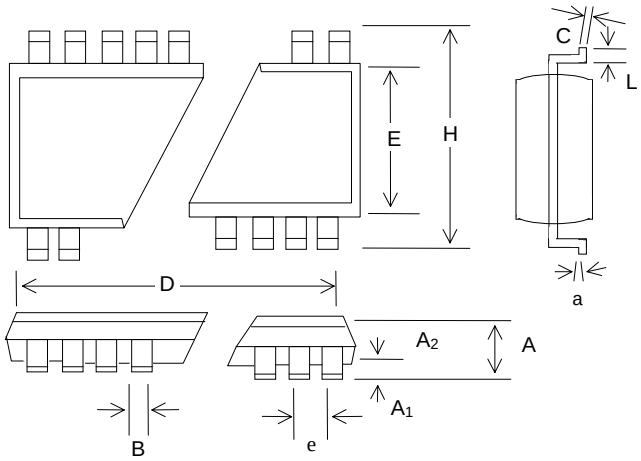
Typical Application Circuit



DUAL MODULUS PRESCALER

	3V	5V	
8/9	700	1100	Maximum Values for f VCO (MHz)
16/17	1400	2200	
32/33	2800	4400	
64/65	5600	8800	

Package Drawing and Dimensions



16 Pin SOIC Outline Dimensions (300 mil)

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.093	-	0.104	2.35	-	2.65
A_1	0.004	-	0.012	0.10	-	0.30
A2	0.089		0.093	2.25		2.35
B	0.013	-	0.020	0.33	-	0.51
C	0.009	-	0.013	0.23	-	0.32
D	0.398	-	0.413	10.10	-	10.50
E	0.291	-	0.299	7.40	-	7.60
e	0.050 BSC			1.27 BSC		
H	0.394	-	0.419	10.00	-	10.65
L	0.016	-	0.050	0.40	-	1.27
a	0º	-	8º	0º	-	8º

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Ordering Information

Part Number	Package Type	Production Flow
IMI145158GXB	16 PIN SOIC	Industrial, -40°C to +85°C

* Please contact factory for other options.

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
145158GXB
Date Code, Lot #