

Low Cost PCMCIA Card Memory Controller

ISS-PCM-002

PCMCIA Card Memory Controller With Support For 256 Bytes Of External EEPROM Attribute Memory

Features

- ✓ Supports PCMCIA PC Card Standard – Release 2.1.
- ✓ Directly connects to PCMCIA Connector without additional components.
- ✓ 2048-bit external Microwire protocol compatible serial EEPROM for Attribute Memory.
- ✓ 3.3 Volts operation.
- ✓ 144-Pin TQFP, Max. Height =1.2 mm Mounted.
- ✓ Usage is Single Devices Per Card.
- ✓ Supports up to 64 Mbytes of:

Flash	EEPROM	SRAM
ROM	OTP	

1.0 Description

The ISS-PCM-002 is a low power, high integration PCMCIA PC Card Standard Release 2.1 compliant interface with no other support devices. A single ISS-PCM-002 is used on each memory card. The device contains a complete address and data buffer, address decoder, memory device selection logic, read and write control logic and a Serial EEPROM access controller for Card Information Structure (CIS). Eight chip enable outputs are provided, supporting 16 memory devices. The device is pinned out for direct connection to the PCMCIA connector without PC trace crossovers. Its 1.0-mm thick body allows population of both sides of a Type 1 PCMCIA card.

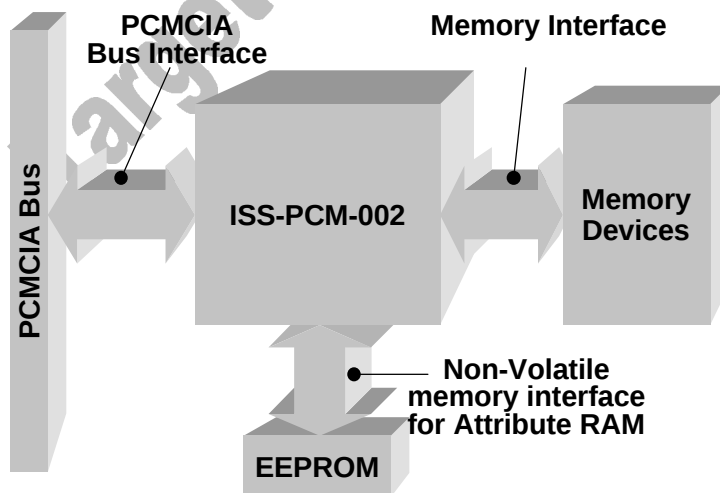


Figure 1: ISS-PCM-002 Interfaces

2.0 Pin Configuration

ISS-PCM-002 pins are defined by the following two tables. The ISS-PCM-002 Pin Description Table lists and describes the function of each signal used in the chip set. The ISS-PCM-002 Physical Pin Assignment Table lists the signals

connected to each pin and the buffer type implemented for the corresponding pin. The pullup resistors included on chip as shown in the table have a nominal value of 375K ohms. A pound, "#", appended to a signal name indicates the signal name indicates the signal is active low.

Table 1: ISS-PCM-002 Pin Description

Name	Type	Description
D[15:0]	Bidir	PCMCIA Data Bus.
A[24:0]	Input	PCMCIA Address Bus.
CE2#	Input	Active low, PCMCIA byte enable for odd byte.
CE1#	Input	Active low, PCMCIA byte enable for even byte.
OE#	Input	Active low, PCMCIA output enable signal.
WE#	Input	Active low, PCMCIA write enable signal.
REG#	Input	PCMCIA signal high for common memory, low attribute memory.
LD[15:0]	Bidir	Local Memory data bus.
LA[24:1]	Output	Local Memory address bus.
SGL/DBL#	Input	Address decoder mode control input.
SEL[1:0]	Input	Address decoder selections inputs.
DEC[2:0]	Input	Address inputs decoded to generate ICE[7:0]# outputs.
LOEH#	Output	Active low local output enable for upper byte of memory.
LOEL#	Output	Active low local output enable for lower byte of memory.
LWEH#	Output	Active low local write enable for upper byte of memory.
LWEL#	Output	Active low local write enable for lower byte of memory.
WP	Output	Write protect.
LWP#	Input	Input from write protect switch.
ATTCE	Output	Chip enable for External Serial EEROM.
ATTCLK	Output	Clock for External Serial EEROM.
ATTDIN	Input	Data from External Serial EEROM.
ATTDOUT	Output	Data to External Serial EEROM.
LCE[7:0]#	Output	Active low local chip enable outputs for 8 pairs of memory devices.
RESET	Input	Active high reset.
LRST#	Output	Inverted output of the RESET input.
WPATT	Input	Active high Attribute Memory protect signal.
R/B#	Output	Output from LR/B# and Attribute Memory Ready/Busy# combined.
LR/B#	Input	Local Ready/Busy# input from common memory.

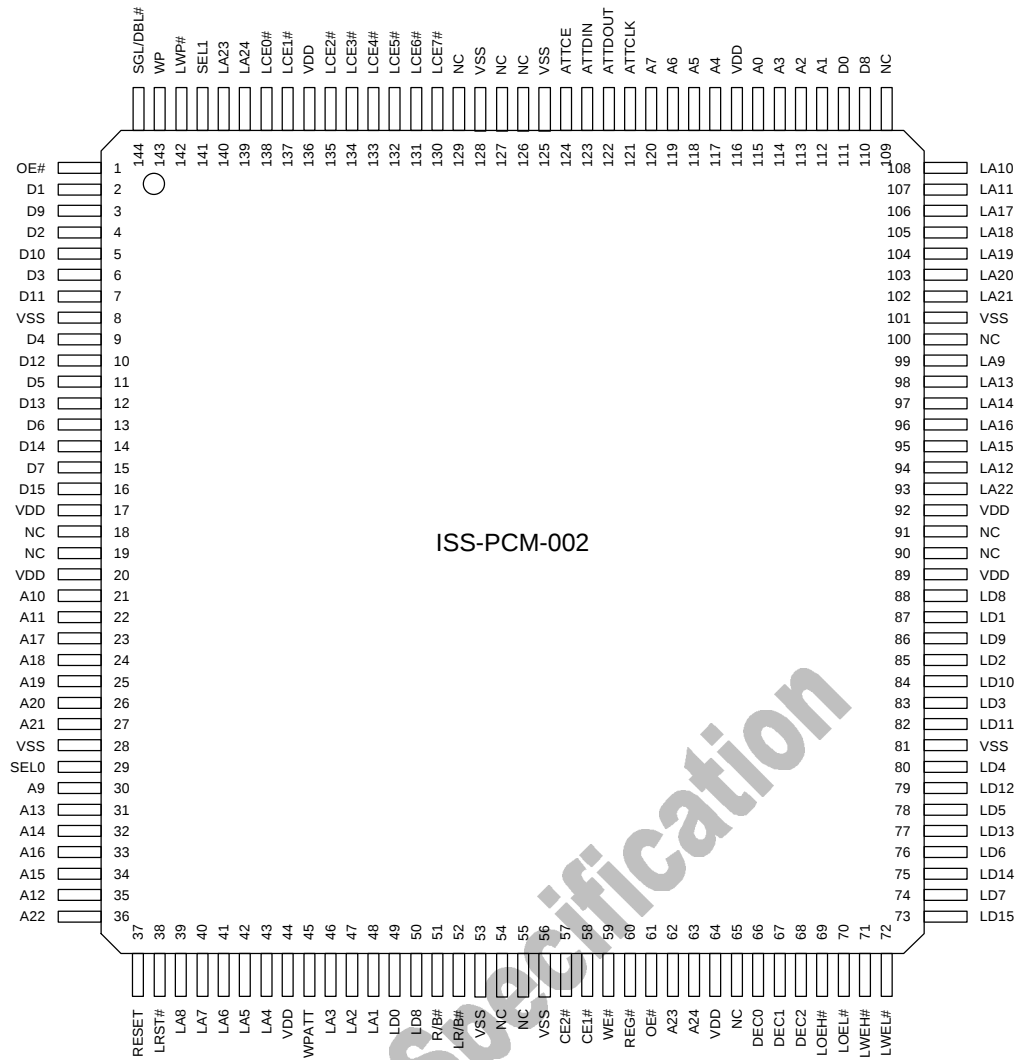
Table 2: ISS-PCM-002 Physical Pin Assignment

Pkg. Pin	Pin Name	Pkg. Pin	Pin Name	Pkg. Pin	Pin Name	Pkg. Pin	Pin Name
1	OE#	37	RESET pd	73	LD15	109	NC
2	D1	38	LRST#	74	LD7	110	D8
3	D9	39	LA8	75	LD14	111	D0
4	D2	40	LA7	76	LD6	112	A1
5	D10	41	LA6	77	LD13	113	A2
6	D3	42	LA5	78	LD5	114	A3
7	D11	43	LA4	79	LD12	115	A0
8	VSS	44	VDD	80	LD4	116	VDD
9	D4	45	WPATT pd	81	VSS	117	A4
10	D12	46	LA3	82	LD11	118	A5
11	D5	47	LA2	83	LD3	119	A6
12	D13	48	LA1	84	LD10	120	A7
13	D6	49	LD0	85	LD2	121	ATTCLK
14	D14	50	LD8	86	LD9	122	ATTDOOUT
15	D7	51	R/B#	87	LD1	123	ATTDIN
16	D15	52	LR/B#	88	A8	124	ATTCE
17	VDD	53	VSS	89	VDD	125	VSS
18	NC	54	NC	90	NC	126	NC
19	NC	55	NC	91	NC	127	NC
20	VDD	56	VSS	92	VDD	128	VSS
21	A10	57	CE2# pu	93	LA22	129	B/A#
22	A11	58	CE1# pu	94	LA12	130	LCE7#
23	A17	59	WE# pu	95	LA15	131	LCE6#
24	A18	60	REG# pu	96	LA16	132	LCE5#
25	A19	61	OE# pu	97	LA14	133	LCE4#
26	A20	62	A23	98	LA13	134	LCE3#
27	A21	63	A24	99	LA9	135	LCE2#
28	VSS	64	VDD	100	RESET pd	136	VDD
29	SELO pu	65	NC	101	VSS	137	LCE1#
30	A9	66	DEC0	102	LA21	138	LCE0#
31	A13	67	DEC1	103	LA20	139	LA24
32	A14	68	DEC2	104	LA19	140	LA23
33	A16	69	LOEH#	105	LA18	141	SEL1 pu
34	A15	70	LOEL#	106	LA17	142	LWP# pu
35	A12	71	LWEH#	107	LA11	143	WP
36	A22	72	LWEL#	108	LA10	144	SGL/DBL# pu

Note:

Pu after a pin name indicates a pull up.

Pd after a pin name indicates a pull down.



ISS-PCM-002

Figure 2: ISS-PCM-002 Outline

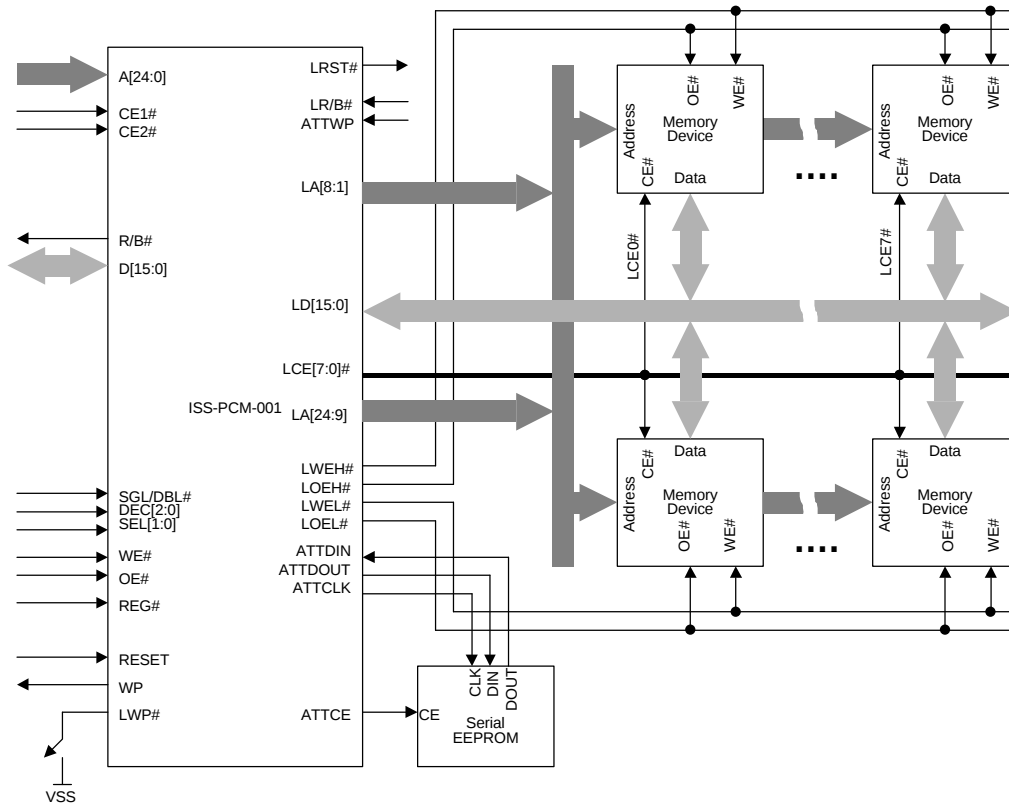


Figure 3: System Block Diagram

3.0 Operation

The ISS-PCM-002 is used to implement PCMCIA Release 2.1 compatible memory cards as shown in the system block diagram and in the internal chip block diagrams. Both PCMCIA signals and memory devices connect directly to the ISS-PCM-002 with no additional components required. The ISS-PCM-002 acts as a data and address buffer and address and control signal decoder for both external memory array and a controller

for accessing the external 2048-bit serial EEPROM which contains the Card Information Structure.

The memory card is mapped into the Common Memory Address space of PCMCIA According to the address signals connected the DEC[2:0], SEL[1:0], and SGL/DBL#. In a typical configuration SGL/DBL# and SEL[1:0] are tied high or left floating since they are pulled up internally. Then DEC[2:0] function as direct

Table 3: Chip Enable Decoder Operation

SGL/DBL# = H			SGL/DBL# = L		
SEL[1:0]	DEC[2:0]	LCE[7:0]#	SEL[1:0]	DEC[2:0]	LCE[7:0]#
XX	000	11111110	00	X00	11111110
XX	001	11111101	00	X01	11111101
XX	010	11111011	00	X10	11111011
XX	011	11110111	00	X11	11110111
XX	100	11101111			
XX	101	11011111	01	XXX	11011111
XX	110	10111111	10	XXX	10111111
XX	111	01111111	11	XXX	01111111

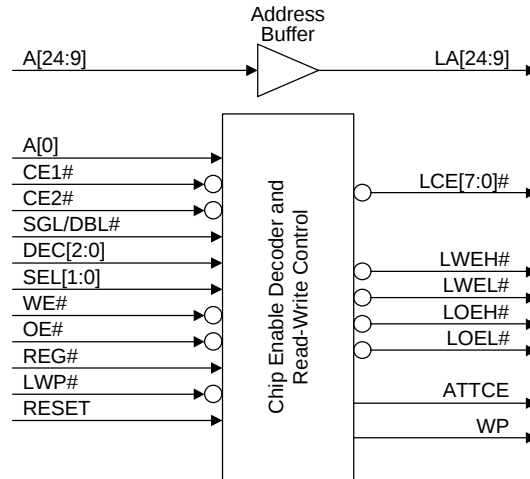


Figure 4: ISS-PCM-002 Decoder Block diagram

inputs to the address/chip enable decoder.

For example, A[25:23] are connected to DEC[2:0] and LA[22:1] are connected to A[21:0] of sixteen 4-Mbytes devices. Note that A0 is used in conjunction with CE1# and CE2# to decode the data access and is not used as a common memory address. A[25:23] then determine which LCE [7:0]# line is active.

Mixed memory size applications can use SGL/DBL# pulled low to enable a mixed mode decoding. This then enables either DEC[2:0] or SEL[1:0] as inputs to the address/chip enable decoder based on the state of SEL[1:0].

For example, the common memory space contains eight 1-Mbyte SRAM devices and six 4-Mbyte Flash devices. A[22:21] are connected to the DEC[1:0] (DEC[2] is a don't care) and A[24:23] are connected to SEL[1:0]. Then

LA[22:1] are used to connect to A[19:0] of the SRAM and A[21:0] of the flash devices. LCE[3:0]# are connected to the four SRAM banks and LCE[7:5]# to the three Flash banks. The SRAM is then memory mapped to the lower 4 Mwords of addressing and the Flash to the next 12 Mwords. All addressing is contiguous. Notice that LCE4# can not be used with this decoding scheme.

The ISS-PCM-002 provides separate output and write enable for the upper and lower bytes of the memory array to implement byte addressing. The assertion of these outputs under the A0, CE2#, CE1#, OE# and WE# is given by Table 4: Read-Write Control Generation when REG# is high.

The LWP# input provides write protection for common memory. When the LWP# is low, assertion of LWEL# and LWEL# is inhibited. The

Table 4: Read-Write Control Generation

OE#	WE#	CE2#	CE1#	A0	LOEL#	LOEH#	LWEL#	LWEH#
1	1	X	X	X	1	1	1	1
0	1	1	1	X	1	1	1	1
0	1	1	0	0	0	1	1	1
0	1	1	0	1	1	0	1	1
0	1	0	1	X	1	0	1	1
0	1	0	0	X	0	0	1	1
1	0	1	1	X	1	1	1	1
1	0	1	0	0	1	1	0	1
1	0	1	0	1	1	1	1	0
1	0	0	1	X	1	1	1	0
1	0	0	0	X	1	1	0	0

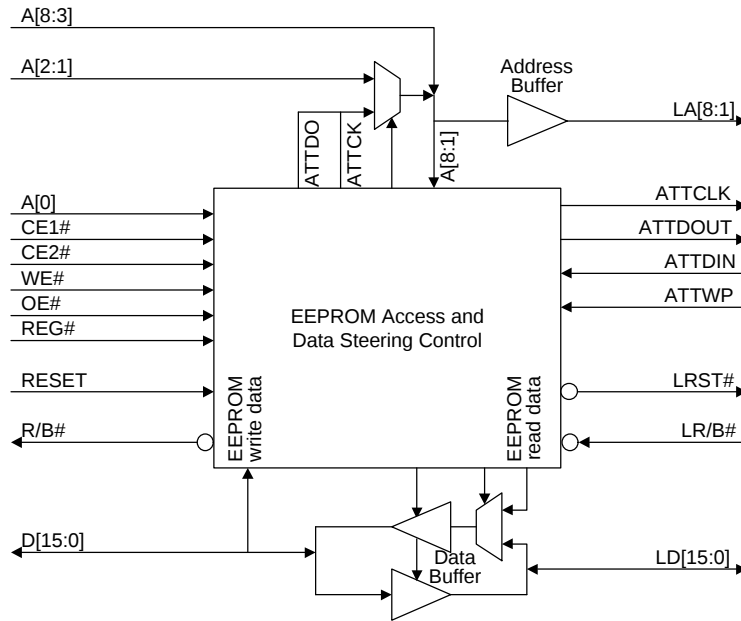


Figure 5: ISS-PCM-002 Datapath Block Diagram

WPATT input provides write for the attribute memory when high. This signal is pulled down internally for applications requiring write protection. In addition, the ISS-PCM-002 is disabled to 3 milliseconds during power up to prevent writes from occurring to either attribute or common memory. The state of the B/A# pin is also latched at this time. The ISS-PCM-002 does not support the optional PCMCIA WAIT# signal.

The ISS-PCM-002 supports both Common and Attribute Memory read and write cycles of word and byte width. Common memory, the external memory devices on the PC card, is selected when REG# is low and can only be accessed in either byte or word mode. Attribute memory, the external serial 2048-bit EEPROM, is selected when REG# is high and can only be accessed as

the even byte of its 512 byte address space. Byte/word addressing is controlled by CE1#, CE2# and A0. OE# functions as an active low output enable. WE# functions as an active low write enable. Memory access functionality is defined by the following table. When Attribute Memory is selected by the assertion of REG#, only the lower data bus, D[7:0] is valid and only even numbered addresses may be accessed.

Accordingly, an entry of "1 or 0" in the REG# of the function table means the access is supported for both Common Memory and Attribute Memory. An entry of "1 only" means the access is supported for Common Memory accesses but not for Attribute Memory accesses.

During word accesses of Common Memory, D[15:0] and LD[15:0] are active. During byte

Table 5: Byte Selection and Data Steering Function

Mode	REG#	CE2#	CE1#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	X	1	1	X	X	X	High Z	High Z
Byte read, even	1 or 0	1	0	0	0	1	High Z	D(even)
Byte read, odd	1 only	1	0	1	0	1	High Z	D(odd)
Word read	1 only	0	0	X	0	1	D(odd)	D(even)
Odd byte only read	1 only	0	1	X	0	1	D(odd)	High Z
Byte write, even	1 or 0	1	0	0	1	0	X	D(even)
Byte write, odd	1 only	1	0	1	1	0	X	D(odd)
Word write	1 only	0	0	X	1	0	D(odd)	D(even)
Odd byte only write	1 only	0	1	X	1	0	D(odd)	X

Accesses (other than odd Byte Only accesses), the PCMCIA transfers take place on D[7:0] and the ISS-PCM-002 performs the required byte lane swapping based on A0 to and from D[15:8] or D[7:0].

The EEPROM access controller includes address and data latches, which are clocked at the leading edge of the effective write pulse that results from the gating of the PCMCIA control signals. Sadwe, Scewe timing parameters shown in the AC timing characteristics guarantee adequate pulse width for the latch clock signals. The actual write is triggered by the rising edge of the first of WE# or CE1# to go high. Access to the external EEPROM Attribute Memory must observe either a 10ms cycle time or wait until R/B# goes inactive before another access can be initiated.

Target Specification

4.0 Electrical Specification

Table 6: Absolute Maximum Ratings

Description	Rating
Supply Voltage, (VDD)	-0.5V to +7.0V
Input Voltage (VIN)	-0.5 to VDD+0.5V
Output Voltage (VOUT)	-0.5 to VDD+0.5V
Power Dissipation (PD)	TBD
Storage Temperature (TSTG)	-65°C to +165°C
Lead Temperature (TL), Soldering, 10 seconds	+260°C

Stresses beyond those listed in Absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions beyond those indicated in the

operational section of this specification is not implied. Exposure to Absolute maximum rating conditions for extended period may affect device reliability.

Table 7: Recommended Operating Conditions

Description	Rating
Supply Voltage (VDD)	3.3V±5%
Operating Temperature (TA)	0°C to 70°C

Table 8: DC Characteristics Under Recommended Operating Conditions

Symbol	Description	Conditions	Min	Max	Units
ICC	VDD Average Supply Current	VDD = 3.3V±5%		150	mA
CIN	Pin input capacitance	f = 1 MHz, T = 25°C, VIN = 0V		12	pf
COU	Pin output capacitance	f = 1 MHz, T = 25°C, VOUT = 0V		12	pf
VIH	Input High Voltage		2.0	5.0	V
VIL	Input Low Voltage		-0.5	0.8	V
VOH	Output High Voltage	IOH = -4.0 mA	2.4	VDD	V
VOL	Output Low Voltage	IOH = 4.0 mA	0	0.4	V
IIL	Input Leakage Current	VSS ≤ VIN ≤ VDD	-10	+10	μA
IOZ	Tri-State Output Leakage Current	VSS ≤ VIN ≤ VDD	-10	+10	μA

Table 9: AC Timing Characteristics

Symbol	Parameter	Min	Max	Notes
Dala	Host address to local address delay		30ns	
Dace	Host address to local chip enable delay		30ns	1
Dcelce	Host chip enable to local chip enable delay		30ns	1
Dcelwe	Host chip enable to local write enable delay		25ns	1
Dwelwe	Host write enable to local write enable delay		25ns	1
Dceld	Host chip enable to local data delay		50ns	
Dweld	Host write enable to local data delay		50ns	
Ddld	Host data to local data delay		25ns	
Dceloe	Host chip enable to local output enable delay		25ns	1
Doeloe	Host output enable to local output enable delay		25ns	1
Dced	Host chip enable to host data delay		50ns	
Doed	Host output enable to host data delay		50ns	
Dlidd	Local data to host data delay		25ns	
Sadwe	Host address and data setup time with respect to host write enable for attribute memory EEPROM write	25ns		
Scewe	Host chip enable setup time with respect to host write enable for attribute memory EEPROM write	150ns		
Hadwe	Host address and data hold time with respect to host write enable for attribute memory EEPROM write	10ns		
Hcewe	Host chip enable hold time with respect to host write enable for attribute memory EEPROM write	10ns		
Twe	Host write enable width for attribute memory EEPROM write		150ns	
Dwerb	Host write enable to chip R/B# delay		50ns	
Trb	Chip R/B# width		10ms	
Sceoe	Host chip enable setup time with respect to host output enable for attribute memory EEPROM read	0ns		
Saoe	Host address setup time with respect to host output enable for attribute memory EEPROM read	0ns		
Hceoe	Host chip enable hold time with respect to host output enable for attribute memory EEPROM read	150ns		
Haoe	Host address hold time with respect to host output enable for attribute memory EEPROM read	150ns		
Doerb	Host output enable to chip R/B# delay		50ns	
Ddrb	Host data valid to chip R/B# delay	50ns		
Doed	Host output enable to host data invalid delay	50ns		
DIrbrb	Local R/B# to chip R/B# delay			1,2
Drsta	Host reset to chip active delay		50ns	2
Drsti	Host reset to chip inactive delay		50ns	2

Notes:

1. Symmetrical for assertion and de-assertion.
2. Not shown in timing diagrams.

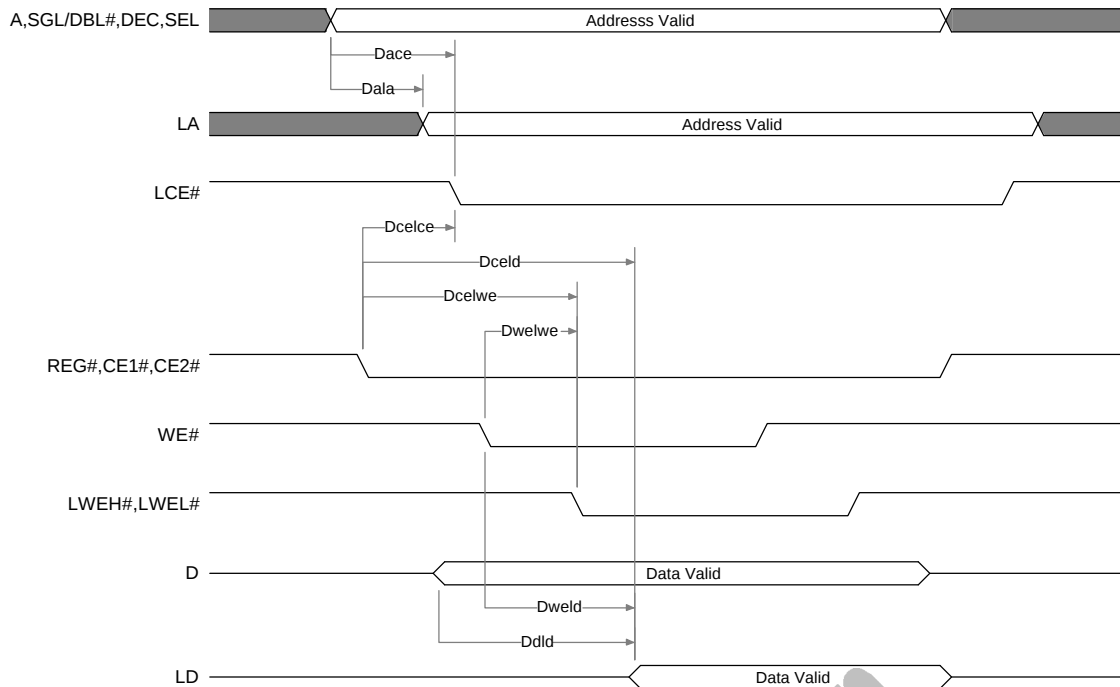


Figure 6: Write to common memory.

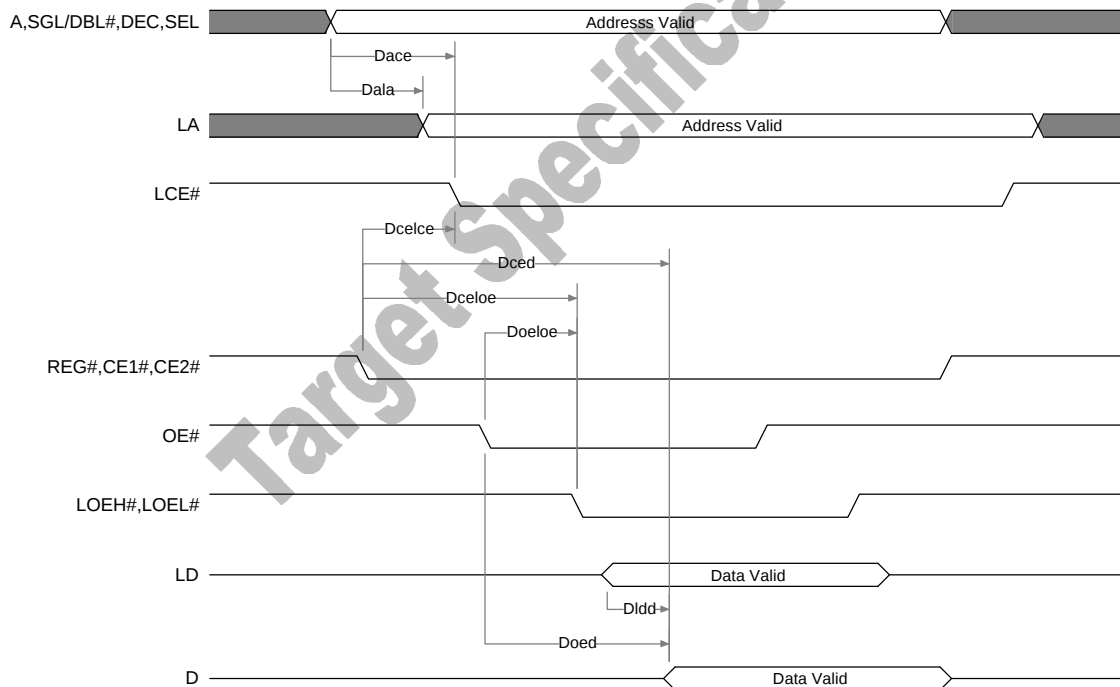


Figure 7: Read from common memory.

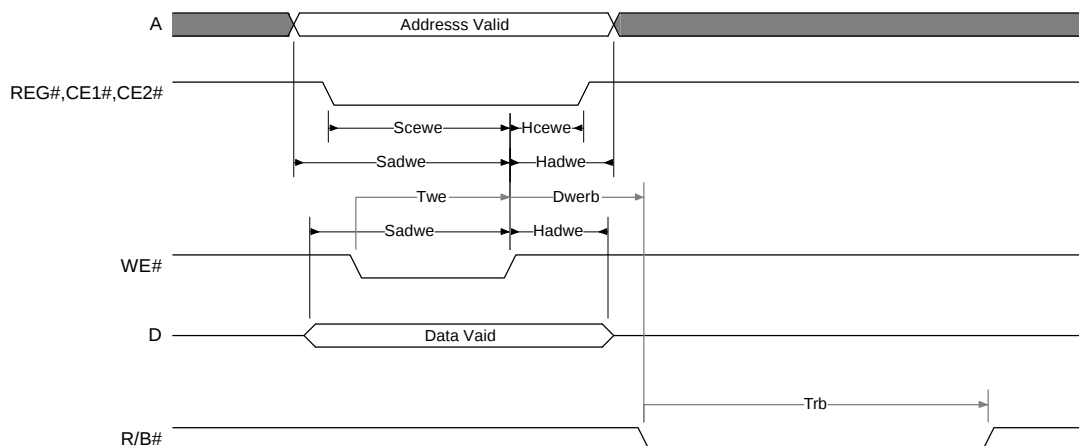


Figure 8: Write to Attribute Memory.

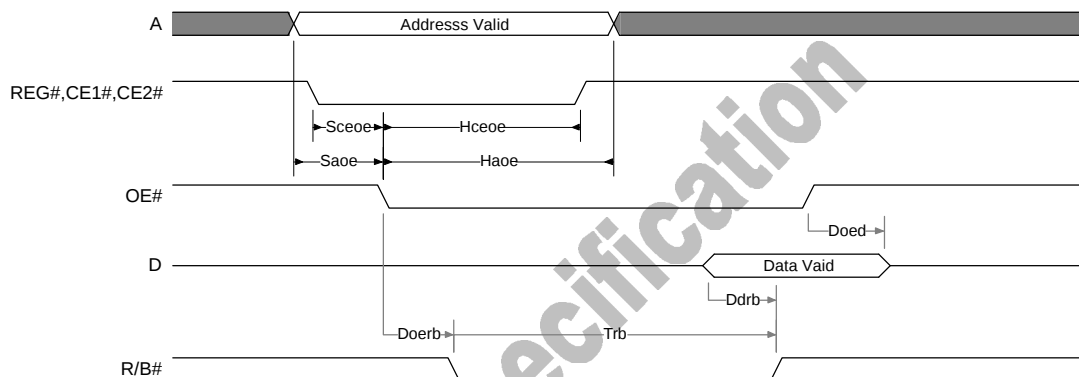


Figure 9: Read from Attribute memory.

5.0 Sales Information

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