PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8737-11

LOW SKEW ÷1/÷2 3.3V LVPECL CLOCK GENERATOR

GENERAL DESCRIPTION

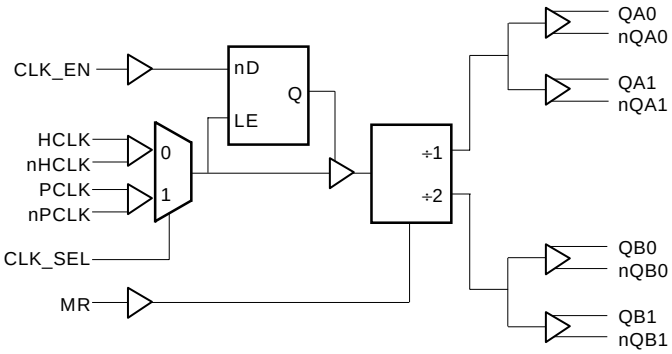
The ICS8737-11 is very low skew, 3.3V LVPECL Clock Generator/Divider and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8737-11 is designed to translate any differential signal levels to 3.3V LVPECL levels. The output enable is synchronous which eliminates the runt clock pulses which occur during asynchronous enabling and disabling of the outputs.

Guaranteed output and part-to-part skew characteristics make the ICS8737-11 ideal for those clock distribution applications demanding well defined performance and repeatability.

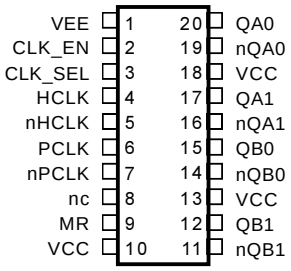
FEATURES

- 2 divide by 1 differential 3.3V LVPECL outputs; 2 divide by 2 differential 3.3V LVPECL outputs
- Selectable differential HSTL and LVPECL clock inputs
- LVCMOS / LVTTL control inputs
- Translates any differential input signal (DCM, HSTL, LVDS, SSTL) to LVPECL levels without external bias networks
- Translates any single-ended input signal (LVCMOS, LVTTL, GTL) to LVPECL levels with resistor bias on nCLK input
- Translates any single-ended input signal (LVCMOS, LVTTL, GTL) to inverted LVPECL levels with resistor bias on CLK input
- Output frequency up to 700MHz
- 75ps output skew
- 3.3V operating supply voltages
- 20 lead TSSOP
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8737-11

20-Lead TSSOP
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	VEE	Power		Power supply pin. Connect to ground.
2	CLK_EN	Power	Pullup	Output enable. Controls enabling and disabling of clock outputs.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH selects differential HSTL inputs. When LOW selects differential PECL inputs. LVCMOS / LVTTL interface levels.
4	HCLK	Input	Pulldown	Non-inverting differential HSTL clock input.
5	nHCLK	Input	Pullup	Inverting differential HSTL clock input.
6	PCLK	Input	Pulldown	Non-inverting differential PECL clock input.
7	nPCLK	Input	Pullup	Inverting differential PECL clock input.
8	nc	Unused		Unused pin.
9	MR	Input	Pulldown	Resets the output divider.
10, 13, 18	VCC	Power		Input power supply pin. Connect to 3.3V.
11, 12	nQB1, QB1	Output		Differential clock outputs. LVPECL interface levels.
14, 15	nQB0, QB0	Output		Differential clock outputs. LVPECL interface levels.
16, 17	nQA1, QA1	Output		Differential clock outputs. LVPECL interface levels
19, 20	nQA0, QA0	Output		Differential clock outputs. LVPECL interface levels

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	HCLK, nHCLK					pF
		PCLK, nPCLK					pF
		CLK_SEL, CLK_EN, MR					pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3A. CONTROL INPUTS FUNCTION TABLE

Inputs			Outputs			
MR	CLK_EN	CLK_SEL	QA0 thru QA1	nQA0 thru nQA1	QB0 thru QB1	nQB0 thru nQB1
1	X	X	LOW	HIGH	LOW	HIGH
0	0	0	LOW	HIGH	LOW	HIGH
0	0	1	LOW	HIGH	LOW	HIGH
0	1	0	Active	Active	Active	Active
0	1	1	Active	Active	Active	Active

In the active mode the state of the output is a function of the HCLK , nHCLK and PCLK, nPCLK inputs as described in Table 3B.

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs		Outputs				Input to Output Mode	Polarity
HCLK or PCLK	nHCLK or nPCLK	QAx	nQAx	QBx	nQBx		
0	0	LOW	HIGH	LOW	HIGH	Differential to Differential	Non Inverting
1	1	HIGH	LOW	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential input be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a 10KΩ resistor from the input pin to VDD, 10KΩ resistor from the input pin to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is VDD/2 ± 300mV.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDDI + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VCC	Input Power Supply Voltage		3.135	3.3	3.465	V
IEE	Power Supply Current			37		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, VCC = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK_SEL, CLK_EN, MR		2		3.765	V
VIL	Input Low Voltage	CLK_SEL, CLK_EN, MR		-0.3		0.8	V
IIH	Input High Current	CLK_EN				5	µA
		CLK_SEL, MR				150	µA
IIL	Input Low Current	CLK_EN		-150			µA
		CLK_SEL, MR		-5			µA

TABLE 4C. LVHSTL DC CHARACTERISTICS, VCC = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	HCLK				150	µA
		nHCLK				5	µA
IIL	Input Low Current	HCLK		-5			µA
		nHCLK		-150			µA
VPP	Peak-to-Peak Input Voltage			0.1		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1, 2			0.13		1.3	V

NOTE 1: Common mode voltage for HSTL is defined as the crossover voltage. VCMR is compatible with DCM, LVDS, LVPECL and SSTL input levels.
NOTE 2: For single ended applications the maximum input voltage for HCLK and nHCLK is VDD + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, VCC = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	PCLK, nPCLK		2.135		2.42	V
VIL	Input Low Voltage	PCLK, nPCLK		1.49		1.825	V
IIH	Input High Current	PCLK				150	µA
		nPCLK				5	µA
IIL	Input Low Current	PCLK		-5			µA
		nPCLK		-150			µA
VPP	Peak-to-Peak Input Voltage			0.15		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1			1.5		VDD	V
VOH	Output High Voltage; NOTE 2, 3		VDD = 3.3V	1.9		2.3	V
VOL	Output Low Voltage; NOTE 2, 3		VDD = 3.3V	1.2		1.6	V
VSWING	Peak-to-Peak Output Voltage Swing			0.6		0.85	V

NOTE 1: Common mode input voltage for LVPECL is defined as the minimum VIH. For single ended applications, VIHmax is VDD + 0.3V.
NOTE 2: Noted output levels are for VDD equal to 3.3V. Output levels will vary 1:1 with VDD.
NOTE 3: Outputs terminated with 50Ω to VDD - 2V. The power dissipation of a terminated output pair is 30mW.

TABLE 5. AC CHARACTERISTICS, VCC = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency					700	MHz
tpLH	Propagation Delay, Low-to-High; NOTE 2			1.0		1.6	ns
tpHL	Propagation Delay, High-to-Low; NOTE 2			1.0		1.4	ns
tsk(o)	Output Skew; NOTE 3					75	ps
tsk(b)	Bank Skew	Bank A				30	ps
		Bank B				30	ps
tsk(pp)	Part-to-Part; NOTE 4	HCLK, nHCLK				150	ps
		PCLK, nPCLK				150	ps
tjit(Ø)	Input-to-Output Jitter; NOTE 5					0	ps
tR	Output Rise Time		30% to 70%	100		450	ps
tF	Output Fall Time		30% to 70%	100		450	ps
tDC	Output Pulse Width			48	50	52	%
tS	Clock Enable Setup Time			1.0			ns
tH	Clock Enable Hold Time			0.5			ns

NOTE 1: All parameters measured at 500MHz unless noted otherwise.
NOTE 2: Measured from the differential input crossing point to the differential output crossing point.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from the 50% point of the input to the differential output crossing point.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Measured from 50% of like inputs to the differential output crossing point.
NOTE 5: Measured by triggering on input signal and measuring the largest displacement between output cycles.

PACKAGE OUTLINE - G SUFFIX

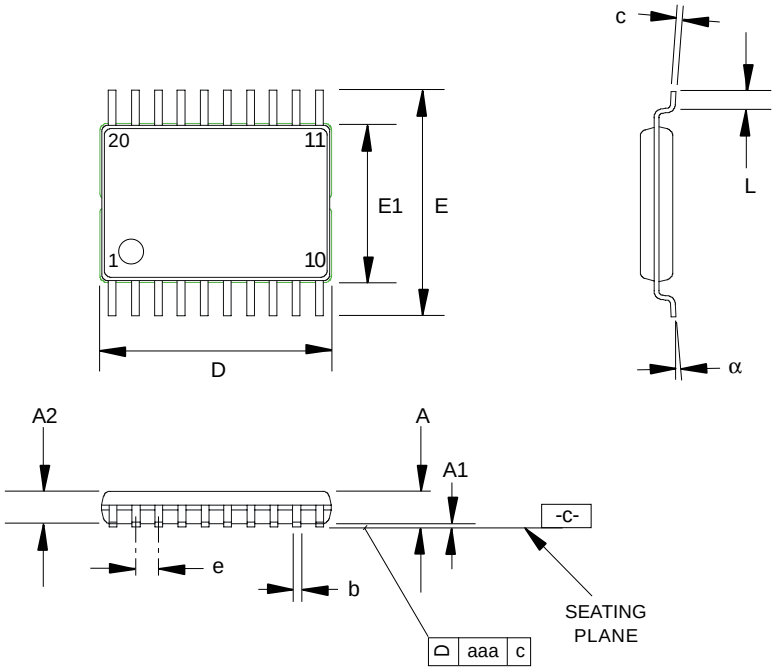


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
N	20			
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	6.40	6.60	.252	.260
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		.0256 BASIC	
L	0.45	0.75	.018	.030
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8737AG-11	ICS8737AG-11	20 lead TSSOP	74	0°C to 70°C
ICS8737AGT-11	ICS8737AG-11	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C