



Integrated
Circuit
Systems, Inc.

ICS8634-01

1-TO-5 DIFFERENTIAL-TO-LVPECL

ZERO DELAY BUFFER

GENERAL DESCRIPTION



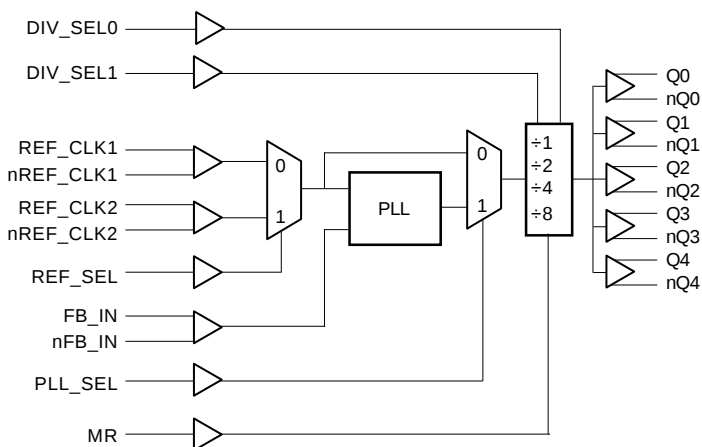
The ICS8634-01 is a high performance LVPECL zero delay buffer and a member of the HiPerClockS™ family of High Performance Clocks Solutions from ICS. The VCO operates at a frequency range of 250MHz to 500MHz.

Utilizing one of the outputs as feedback to the PLL output frequencies up to 250MHz can be regenerated with zero delay with respect to the input. Dual reference clock inputs support redundant clock or multiple reference applications.

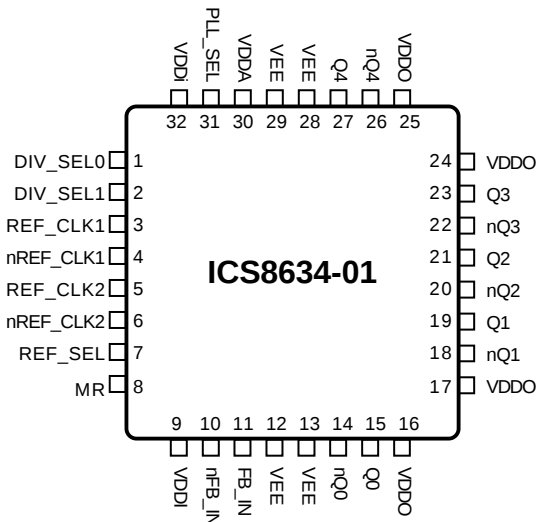
FEATURES

- Fully integrated PLL
- 5 LVPECL outputs each with the ability to drive 50Ω to VTT
- 31.25MHz to 250MHz output frequency range
- Spread Smart™ for regenerating spread spectrum clocks
- Differential reference clock inputs accept any differential input signal
- Differential reference clock inputs will accept single ended input signal with one of the inputs biased with a resistor network
- 31.25MHz to 250MHz input frequency range
- LVCMOS / LVTTTL control inputs
- 3.3V operating supply voltage
- 32 lead low-profile QFP (LQFP), 7mm x 7mm x 1.4mm package body, 0.8mm package lead pitch
- 0°C to 70°C ambient operating temperature
- Industrial temperature version available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	DIV_SEL0	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTTL interface levels.
2	DIV_SEL1	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTTL interface levels.
3	REF_CLK1	Input	Pulldown	Non-inverting differential clock input.
4	nREF_CLK1	Input	Pullup	Inverting differential clock input.
5	REF_CLK2	Input	Pulldown	Non-inverting differential clock input.
6	nREF_CLK2	Input	Pullup	Inverting differential clock input.
7	REF_SEL	Input	Pulldown	Differential clock select input. When Low selects REF_CLK2 or nREF_CLK2. When HIGH selects REF_CLK1 or nREF_CLK1.
8	MR	Input	Pulldown	Resets dividers and determine state of the outputs. LVCMOS / LVTTTL interface levels.
9	VDDI	Power		Input and core power supply pin. Connect to 3.3V.
10	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay".
11	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay".
12, 13 28, 29	VEE	Power		Ground pins. Connect to ground.
14, 15	nQ0, Q0	Output		Differential clock outputs. 50Ω typical output impedance. LVPECL interface levels.
16, 17, 24, 25	VDDO	Power		Output power supply pins. Connect to 3.3V.
18, 19	nQ1, Q1	Output		Differential clock outputs. 50Ω typical output impedance. LVPECL interface levels.
20, 21	nQ2, Q2	Output		Differential clock outputs. 50Ω typical output impedance. LVPECL interface levels.
22, 23	nQ3, Q3	Output		Differential clock outputs. 50Ω typical output impedance. LVPECL interface levels..
26, 27	nQ4, Q4	Output		Differential clock outputs. 50Ω typical output impedance. LVPECL interface levels.
30	VDDA	Power		PLL power supply pin. Connect to 3.3V.
31	PLL_SEL	Input	Pullup	Selects between the PLL and the reference clock as the input to the dividers. When HIGH select PLL. When LOW selects reference clock. LVCMOS / LVTTTL interface levels.
32	VDDI	Power		Output power supply pin. Connect to 3.3V.



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TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	REF_CLK1, nREF_CLK1, REF_CLK2, nREF_CLK2, FB_IN, nFB_IN		TBD		pF
		DIV_SEL0, DIV_SEL1, REF_SEL, PLL_SEL, MR		TBD		pF
RPULLUP	Input Pullup Resistor			51		K Ω
RPULLDOWN	Input Pulldown Resistor			51		K Ω

TABLE 3. CONTROL INPUTS FUNCTION TABLE

DIV_SEL1	DIV_SEL0	FREQUENCY (MHz)	
		MINIMUM	MAXIMUM
0	0	250	250
0	1	125	250
1	0	62.5	125
1	1	31.25	62.5

TABLE 4. PLL INPUT REFERENCE CHARACTERISTICS, VDDI=VDDA=3.3V $\pm$ 5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fREF	Input Reference Frequency		20		250	MHz
tR	Input Rise Time	Measured at 20% to 80% points			TBD	ns
tF	Input Fall Time	Measured at 20% to 80% point			TBD	ns
tDC	Input Reference Duty Cycle		TBD		TBD	%



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD+0.5 V
Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 5A. POWER SUPPLY DC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDA	Analog Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
IEE	Power Supply Current				100	mA

TABLE 5B. DIFFERENTIAL DC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	REF_CLK1, REF_CLK2, FB_IN	VIN = 3.465V		150	μA
		nREF_CLK1, nREF_CLK2, nFB_IN	VIN = 3.465V		5	μA
IIL	Input Low Current	REF_CLK1, REF_CLK2, FB_IN	VIN = 0V	-5		μA
		nREF1, nREF2, nFB_IN	VIN = 0V	-150		μA

NOTE: For REF_CLK1, nREF_CLK1 and REF_CLK2, nREF_CLK2 input levels, see VPP and VCMR in AC Characteristics table.

TABLE 5C. LVCMOS DC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	DIV_SEL0, DIV_SEL1, REF_SEL, PLL_SEL, MR	2		3.765	V
VIL	Input Low Voltage	DIV_SEL0, DIV_SEL1, REF_SEL, PLL_SEL, MR	-0.3		0.8	V
IIH	Input High Current	SEL0, SEL1, REF_SEL, MR	VIN = 3.465V		150	μA
		PLL_SEL	VIN = 3.465V		5	μA
IIL	Input Low Current	SEL0, SEL1, REF_SEL, MR	VIN = 0V	-5		μA
		PLL_SEL	VIN = 0V	-150		μA



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TABLE 5D. LVPECL DC CHARACTERISTICS, $V_{DDI}=V_{DDA}=V_{DDO}=3.3V\pm5\%$, $T_A=0^{\circ}C$ TO $70^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1	VDD = 3.3V	1.9		2.3	V
VOL	Output Low Voltage; NOTE 1	VDD = 3.3V	1.2		1.6	V
VSWING	Peak-to-Peak Output Voltage Swing					V

NOTE 1: Outputs terminated with 50Ω to ground. The power dissipation of a terminated output pair is 32mW.

TABLE 6. AC CHARACTERISTICS, $V_{DDI}=V_{DDA}=V_{DDO}=3.3V\pm5\%$, $T_A=0^{\circ}C$ TO $70^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Output Frequency				250	MHz
VPP	Peak-to-Peak Input Voltage	f = 250MHz	.15		1.3	V
VCMR	Common Mode Input Voltage	f = 250MHz	0.7		VCC	V
tpD	Propagation Delay,	PLL_SEL=0V, 0MHz ≤ f ≤ 622MHz	2.4		3.3	ns
t(∅)	PLL Reference Zero Delay; NOTE 2	PLL_SEL=3.3V, fREF=133, fVCO=266	-80	21.5	120	ps
tsk(o)	Output Skew; NOTE 3				35	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 4			25	50	ps
tL	PLL Lock Time				1	mS
tR	Output Rise Time		200		700	ps
tF	Output Fall Time		200		700	ps
tPW	Output Pulse Width	0MHz ≤ f ≤ 250MHz	tCYCLE/2 - 200	tCYCLE/2	tCYCLE/2 + 200	ps
		f = 250MHz	1.8	2	2.2	ns

NOTE 1: All parameters measured at fMAX unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.

NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as the variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent pairs of cycles.



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PACKAGE OUTLINE - Y SUFFIX

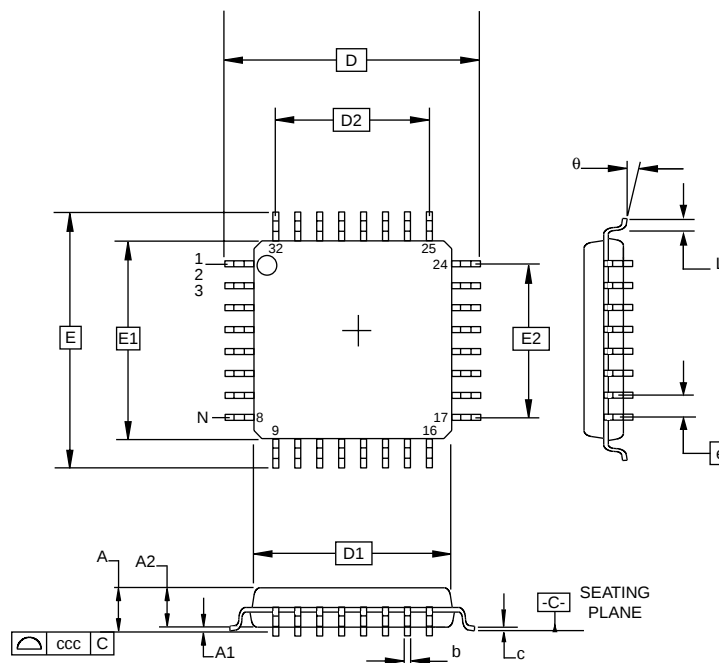


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026



TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8634Y-01	ICS8634-01	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8634-01T	ICS8634-01	32 Lead LQFP on Tape and Reel	2000	0°C to 70°C

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