Integrated Circuit Systems, Inc.

ICS8535-01

LOW SKEW, 1-TO-4 LVCMOS-TO-LVPECL FANOUT BUFFER

GENERAL DESCRIPTION

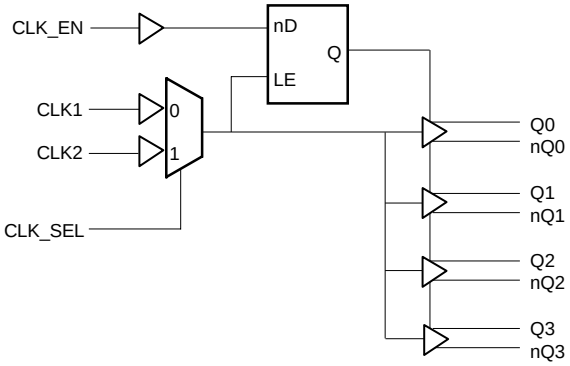
The ICS8535-01 is a low skew, high performance clock fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8535-01 has multiple clock inputs that accept LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The output enable is synchronous which eliminates the runt clock pulses which occur during asynchronous enabling and disabling of the outputs.

Guaranteed output and part-to-part skew characteristics make the ICS8535-01 ideal for those applications demanding well defined performance and repeatability.

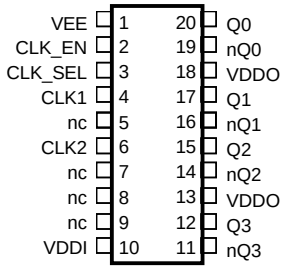
FEATURES

- 4 differential 3.3V LVPECL outputs
- Multiple LVCMOS / LVTTL clock inputs for redundant and multiple frequency fanout applications
- Translates LVCMOS and LVTTL levels to 3.3V LVPECL levels
- 30ps output skew
- LVCMOS / LVTTL control inputs
- 3.3V operating supply
- 20 lead TSSOP
- 0°C to 70°C ambient operating temperature
- Industrial temperature version available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8535-01

20-Lead TSSOP
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	VEE	Power		Negative power supply pin. Connect to power supply ground.
2	CLK_EN	Input	Pullup	Synchronous clock enable. When HIGH clock outputs follows clock input. When LOW, Q outputs are force low, nQ outputs are force high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH selects CLK2 input. When LOW selects CLK1 input. LVCMOS / LVTTL interface levels.
4	CLK1	Input	Pulldown	LVCMOS / LVTTL clock input.
6	CLK2	Input	Pulldown	LVCMOS / LVTTL clock input.
5, 7, 8, 9	nc	Unused		Unused pins.
10, 13, 18	VDD	Power		Power supply pin. Conncect to 3.3V.
11, 12	nQ3, Q3	Output		Differential clock outputs. LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential clock outputs. LVPECL interface levels.
16, 17	nQ1, Q1	Output		Differential clock outputs. LVPECL interface levels.
19, 20	nQ0, Q0	Output		Differential clock outputs. LVPECL interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	CLK1, CLK2					pF
		CLK_EN, CLK_SEL					pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3A. CONTROL INPUTS FUNCTION TABLE

Inputs		Outputs	
CLK_EN	**CLK_SEL**	**Q0 thru Q3**	**nQ0 thru nQ3**
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	Active	Active
1	1	Active	Active

In the active mode the state of the output is a function of the CLK1 and CLK2 inputs as described in Table 3B.

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs	Outputs	
CLK1 or CLK2	**Q0 thru Q3**	**nQ0 thru nQ3**
0	LOW	HIGH
1	HIGH	LOW

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDD + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD	Power Supply Voltage		3.135	3.3	3.465	V
IEE	Quiescent Power Supply Current				50	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK1, CLK 2		2		3.765	V
		CLK_EN, CLK_SEL		2		3.765	V
VIL	Input Low Voltage	CLK1, CLK 2		-0.3		1.3	V
		CLK_EN, CLK_SEL		-0.3		0.8	V
IIH	Input High Current	CLK1, CLK 2, CLK_SEL				150	µA
		CLK_EN				5	µA
IIL	Input Low Current	CLK1, CLK 2, CLK_SEL		-5			µA
		CLK_EN,		-150			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1, 2	VDD = 3.3V	1.9		2.3	V
VOL	Output Low Voltage; NOTE 1, 2	VDD = 3.3V	1.2		1.6	V
VSWING	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Noted output levels are for VDD equal to 3.3V. Output levels will vary 1:1 with VDD.
NOTE 2: Outputs terminated with 50Ω to VDD - 2V. The power dissipation of a terminated output pair is 30mW.

TABLE 5. AC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency					266	MHz
tpLH	Propagation Delay, Low-to-High; NOTE 2			1.0		1.9	ns
tpHL	Propagation Delay, High-to-Low; NOTE 2			1.0		1.9	ns
tsk(o)	Output Skew; NOTE 3				11	30	ps
tsk(pp)	Part-to-Part; NOTE 4	CLK1				150	ps
		CLK2				150	ps
tjit(Ø)	Input-to-Output Jitter; NOTE 5					0	ps
tR	Output Rise Time		30% to 70%	100		700	ps
tF	Output Fall Time		30% to 70%	100		700	ps
tDC	Output Pulse Width			48	50	52	%
tS	Clock Enable Setup Time			1.0			ns
tH	Clock Enable Hold Time			2.0			ns

NOTE 1: All parameters measured at 266 MHz unless noted otherwise.
NOTE 2: Measured from the 50% point of the input to the differential output crossing point.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the differential input crossing point to the differential output crossing point.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and
with equal load conditions. Measured from the 50% point of like inputs to the differential output crossing point.
NOTE 5: Measured by triggering on input signal and measuring the largest displacement between output cycles.

PACKAGE OUTLINE - G SUFFIX

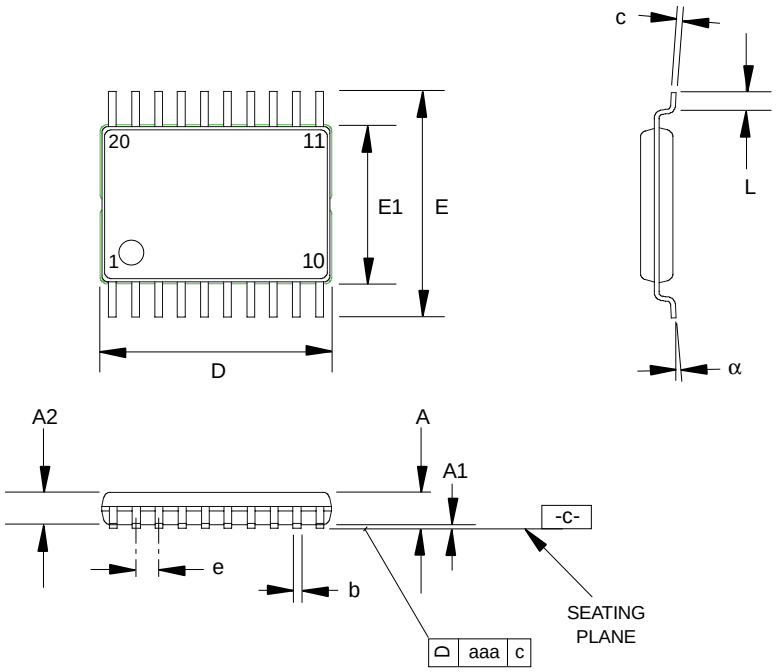


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	4.90	5.10	.193	.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		.0256 BASIC	
L	0.45	0.75	.018	.030
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8535AG-01	ICS8535AG-01	20 lead TSSOP	75 per tube	0°C to 70°C
ICS8535AG-01T	ICS8535AG-01	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C