Integrated Circuit Systems, Inc.

ICS8532-01

LOW SKEW, 1-TO-17 3.3V LVPECL FANOUT BUFFER

GENERAL DESCRIPTION

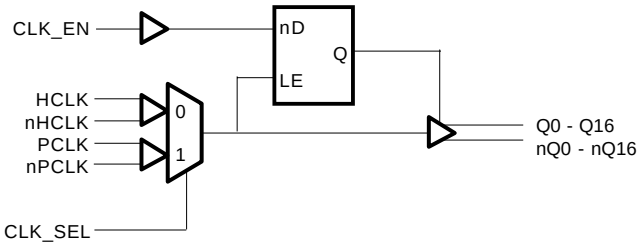
The ICS8532-01 is a very low skew, 1-to-17, 3.3V LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8532-01 has selectable clock inputs that accept either HSTL or PECL input levels. The clock enable is synchronous which eliminates the runt clock pulses which occur during asynchronous enabling and disabling of the outputs.

Guaranteed output and part-to-part skew characteristics make the ICS8532-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

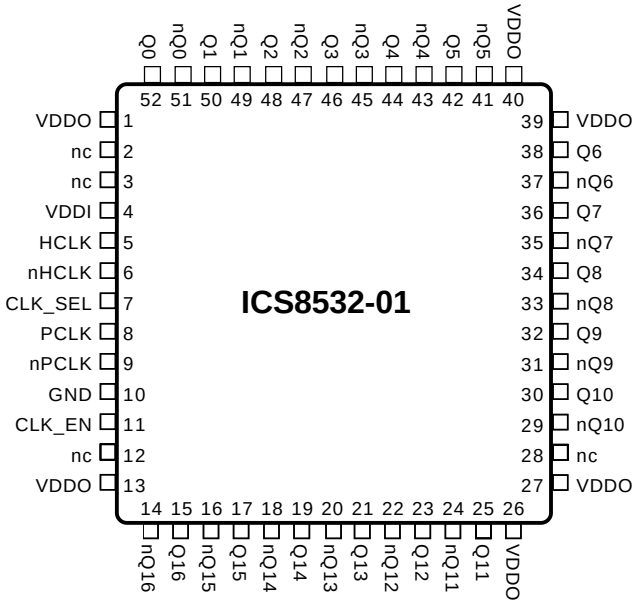
FEATURES

- 17 differential 3.3V LVPECL outputs
- Selectable differential HSTL or PECL clock inputs
- Translates any differential input signal to 3.3V LVPECL
- Translates any single-ended input signal (LVCMOS, LVTTL, GTL) to LVPECL levels with resistor bias on nCLK input
- Translates any single-ended input signal (LVCMOS, LVTTL, GTL) to inverted LVPECL levels with resistor bias on CLK input
- Output frequency up to 500MHz
- 50ps output skew
- 3.3V operating supply voltage
- 52 lead low-profile QFP (LQFP), 10mm x 10mm x 1.4mm package body, 0.65mm package lead pitch
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



52-Lead LQFP
Y package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 13, 26, 27, 39, 40	VDDO	Power		Output power supply. Connect to 3.3V.
4	VDDI	Power		Input power supply. Connect to 3.3V.
2, 3, 12, 28	nc	Unused		Unused pins.
5	HCLK	Input	Pulldown	Non-inverting differential HSTL clock input.
6	nHCLK	Input	Pullup	Inverting differential HSTL clock input.
7	CLK_SEL	Input	Pulldown	Selects between HSTL or PECL clock inputs. LVTTL / LVCMOS interface levels.
8	PCLK	Input	Pulldown	Non-inverting differential PECL clock input.
9	nPCLK	Input	Pullup	Inverting differential PECL clock input.
10	GND	Power		Connect to ground.
11	CLK_EN	Input	Pullup	Synchronous control for enabling and disabling clock outputs. LVTTL / LVCMOS interface levels.
14, 15	nQ16, Q16	Output		Differential output pair. 3.3V LVPECL interface level.
16, 17	nQ15, Q15	Output		Differential output pair. 3.3V LVPECL interface level.
18, 19	nQ14, Q14	Output		Differential output pair. 3.3V LVPECL interface level.
20, 21	nQ13, Q13	Output		Differential output pair. 3.3V LVPECL interface level.
22, 23	nQ12, Q12	Output		Differential output pair. 3.3V LVPECL interface level.
24, 25	nQ11, Q11	Output		Differential output pair. 3.3V LVPECL interface level.
29, 30	nQ10, Q10	Output		Differential output pair. 3.3V LVPECL interface level.
31, 32	nQ9, Q9	Output		Differential output pair. 3.3V LVPECL interface level.
33, 34	nQ8, Q8	Output		Differential output pair. 3.3V LVPECL interface level.
35, 36	nQ7, Q7	Output		Differential output pair. 3.3V LVPECL interface level.
37, 38	nQ6, Q6	Output		Differential output pair. 3.3V LVPECL interface level.
41, 42	nQ5, Q5	Output		Differential output pair. 3.3V LVPECL interface level.
43, 44	nQ4, Q4	Output		Differential output pair. 3.3V LVPECL interface level.
45, 46	nQ3 Q3	Output		Differential output pair. 3.3V LVPECL interface level.
47, 48	nQ2, Q2	Output		Differential output pair. 3.3V LVPECL interface level.
49, 50	nQ1, Q1	Output		Differential output pair. 3.3V LVPECL interface level.
51, 52	nQ0, Q0	Output		Differential output pair. 3.3V LVPECL interface level.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	HCLK, nHCLK					pF
		PCLK, nPCLK					pF
		CLK_EN, CLK,SEL					pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3A. CONTROL INPUTS FUNCTION TABLE

Inputs		Outputs	
CLK_EN	**CLK_SEL**	**Q0 thru Q16**	**nQ0 thru nQ16**
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	Active	Active
1	1	Active	Active

In the active mode the state of the output is a function of the HCLK, nHCLK and PCLK, nPCLK inputs as described in Table 3B.

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
HCLK or PCLK	**nHCLK or nPCLK**	**Q0 thru Q16**	**nQ0 thru nQ16**		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a resistor to VDDI, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is approximately VDDI/2 ± 300mV.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDDI + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
IDDI	Input Power Supply Current			46	60	mA

TABLE 4B. LVHSTL DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	HCLK	VIN = VDDI = 3.465V			150	µA
		nHCLK	VIN = VDDI = 3.465V			5	µA
IIL	Input Low Current	HCLK	VIN = 0V, VDDI = 3.465V	-5			µA
		nHCLK	VIN = 0V, VDDI = 3.465V	-150			µA
VPP	Peak-to-Peak Input Voltagle		3.135V ≤ VDDI ≤ 3.465V	0.1		1.3	V
VCMR	Common Mode Input Voltage; NOTE1		3.135V ≤ VDDI ≤ 3.465V	0.13		1.3	V

NOTE 1: Common mode voltage for HSTL is defined as the crossover voltage. VCMR is compatible with DCM, LVDS and SSTL inputs.

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Current	CLK_EN, CLK_SEL	3.135V ≤ VDDI ≤ 3.465V	2		3.765	V
VIL	Input Low Current	CLK_EN, CLK_SEL	3.135V ≤ VDDI ≤ 3.465V	-0.3		0.8	V
IIH	Input High Current	CLK_SEL	VIN = VDDI = 3.465V			150	µA
		CLK_EN	VIN = VDDI = 3.465V			5	µA
IIL	Input Low Current	CLK_SEL	VIN = 0V, VDDI = 3.465V	-5			µA
		CLK_EN	VIN = 0V, VDDI = 3.465V	-150			µA

TABLE 4D. LVPECL DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	PCLK	VIN = VDDI = 3.465V			150	µA
		nPCLK	VIN = VDDI = 3.465V			5	µA
IIL	Input Low Current	PCLK	VIN = 0V, VDDI = 3.465V	-5			µA
		nPCLK	VIN = 0V, VDDI = 3.465V	-150			µA
VPP	Peak-to-Peak Input Voltage		3.135V ≤ VDDx ≤ 3.465V	0.1		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1		3.135V ≤ VDDx ≤ 3.465V	1.5		3.3	V
VOH	Output High Voltage; NOTE 2, 3		VDDI = VDDO = 3.3V	1.9		2.3	V
VOL	Output Low Voltage; NOTE 2, 3		VDDI = VDDO = 3.3V	1.2		1.5	V
VPPO	Peak-to-Peak Output Voltage		3.135V ≤ VDDx ≤ 3.465V	0.6			V

NOTE 1: Common mode voltage for LVPECL is defined as the minimum VIH.
NOTE 2: Output levels vary 1:1 with VDDI.
NOTE 3: Outputs terminated with 50Ω to VDDO-2V. The power dissipation of a terminated output is 30mW per differential pair.

TABLE 5. AC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				500	MHz
tpLH	Propagation Delay, Low-to-High; NOTE 2	0 ≤ f ≤ 500MHz	1.3		2.5	ns
tpHL	Propagation Delay, High-to-Low; NOTE 2	0 ≤ f ≤ 500MHz	1.3		2.5	ns
tsk(o)	Output Skew; NOTE 3	0 ≤ f ≤ 500MHz			50	ps
tsk(pp)	Part-to-Part Skew; NOTE 4	0 ≤ f ≤ 500MHz		80	250	ps
tR	Output Rise Time	30% to 70%	100		300	ps
tF	Output Fall Time	30% to 70%	100		300	ps
tPW	Output Pulse Width	0 ≤ f ≤ 500MHz	tCYCLE/2 - 0.25	tCYCLE/2	tCYCLE/2 + 0.25	ns
tDC	Output Duty Cycle	0 ≤ f ≤ 266MHz	48	50	52	%
		266 ≤ f ≤ 500MHz	47	50	53	%
tS	Output Enable Setup Time		0.5			ns
tH	Output Enable Hold Time		0.5			ns

NOTE 1: All parameters measured at 500MHz unless noted otherwise.
NOTE 2: Measured from input differential crossing point to the output differential crossing point for differential input levels. Measured from VDDI/2 to the output differential crossing point for single-ended input levels.
NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions. Measured from the 50% point of the input to the differential output crossing point.
NOTE 4: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions. Measured from 50% of like inputs to the differential output crossing point.

FIGURE 1A, 1B - INPUT CLOCK WAVEFORMS

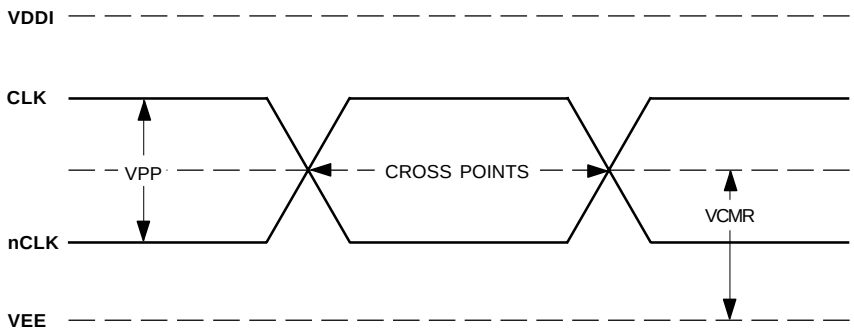


FIGURE 1A - HSTL DIFFERENTIAL INPUT LEVELS

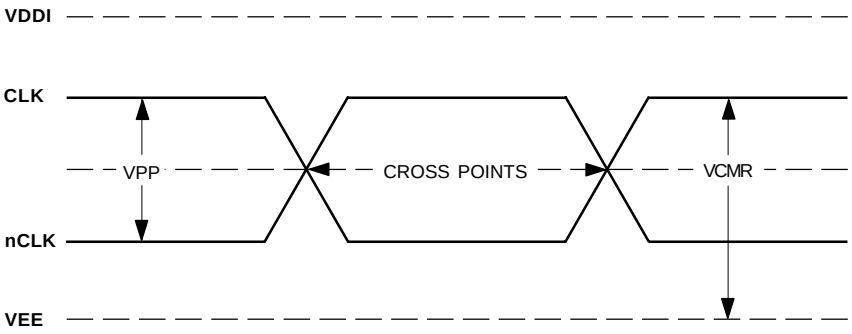


FIGURE 1B - LVPECL DIFFERENTIAL INPUT LEVEL

FIGURE 2A - DIFFERENTIAL INPUT TIMING WAVEFORMS

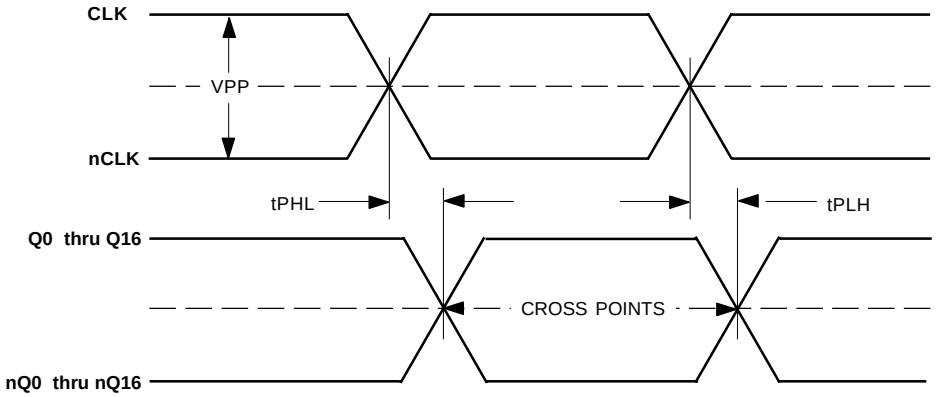


FIGURE 2A - PROPAGATION DELAYS

fin = 500MHz, Vpp = 300mV, tr = tf = 200ps

FIGURE 2B - SINGLE ENDED CLK INPUT TIMING WAVEFORMS

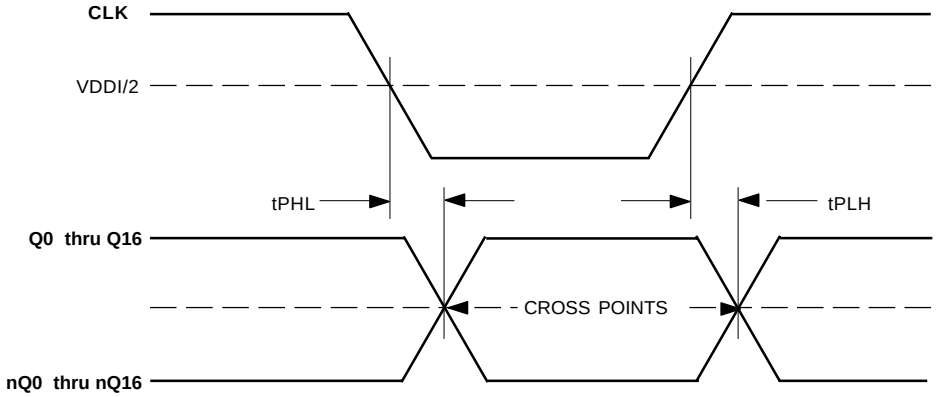


FIGURE 2A - PROPAGATION DELAYS

fin = 500MHz, Vpp = 3.3V, tr = tf = 600ps

FIGURE 2C - SINGLE ENDED nCLK INPUT TIMING WAVEFORMS

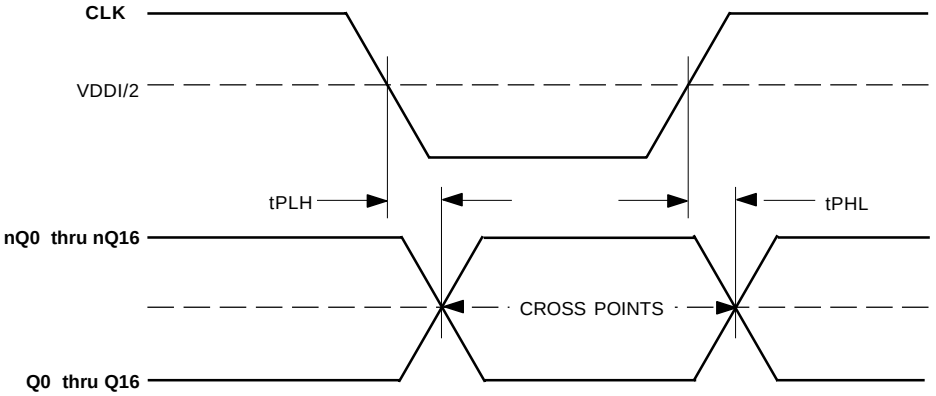


FIGURE 2A - PROPAGATION DELAYS

fin = 250MHz, Vpp = 3.3V, tr = tf = 600ps

FIGURE 3A - OUTPUT SKEW DEFINITION & WAVEFORMS

Output Skew - Skew between any outputs. Outputs operating at the same temperature, supply voltages and with equal load conditions.

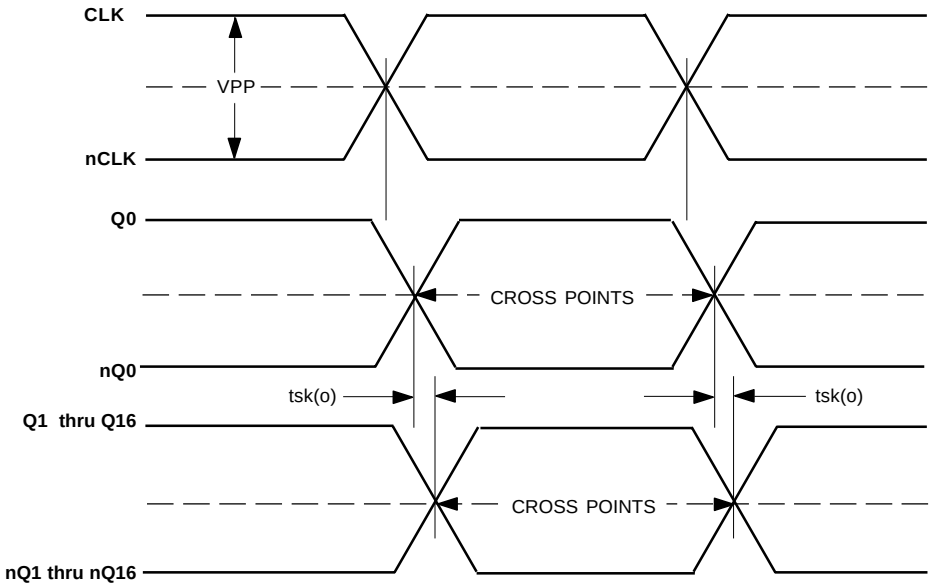


FIGURE 3A - OUTPUT SKEW

fin = 500MHz, Vpp = 300mV, tr = tf = 200ps

FIGURE 3B - PART-TO-PART SKEW DEFINITION & WAVEFORMS

Part-to-Part Skew - Skew between any outputs on different parts. Outputs operating at the same temperature, supply voltages and with equal load conditions.

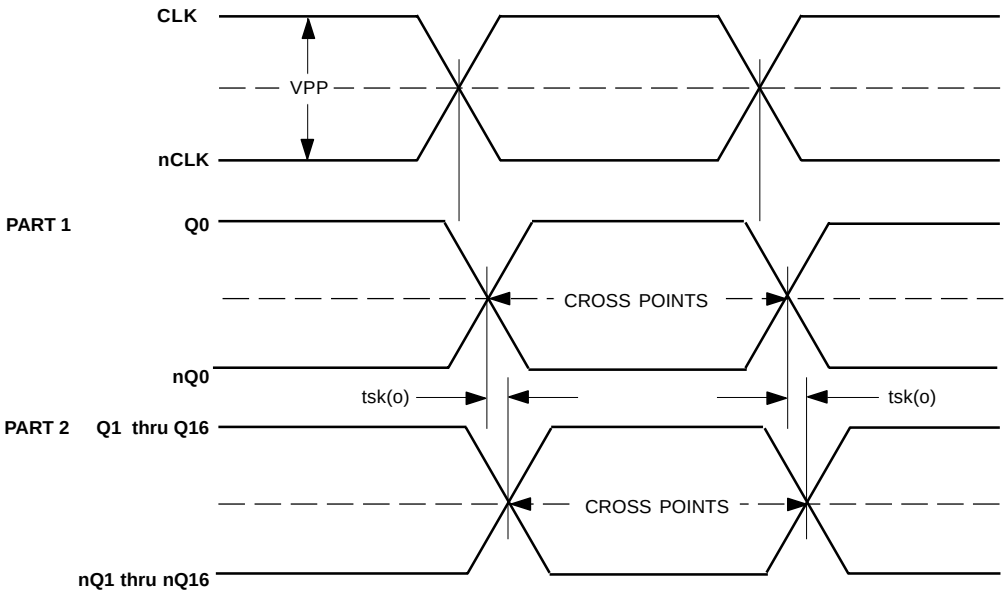


FIGURE 3B - PART-TO-PART SKEW

fin = 500MHz, Vpp = 300mV, tr = tf = 200ps

PACKAGE OUTLINE - Y SUFFIX

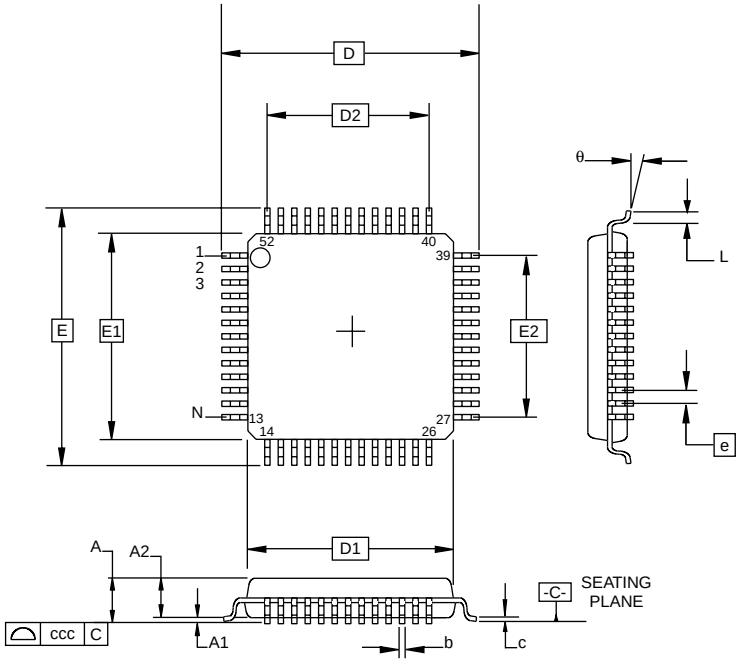


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**BCC**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N		52	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
c	0.09		0.20
D		12.00 BASIC	
D1		10.00 BASIC	
D2		7.80	
E		12.00 BASIC	
E1		10.00 BASIC	
E2		7.80	
e		0.65 BASIC	
L	0.45		0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8532AY-01	ICS8532AY-01	52 Lead LQFP	160 per tray	0°C to 70°C
ICS8532AY-01T	ICS8532AY-01	52 Lead LQFP on Tape and Reel	2000	0°C to 70°C