Integrated Circuit Systems, Inc.

ICS85304-01

LOW SKEW, 1-TO-5 3.3V LVPECL FANOUT BUFFER

GENERAL DESCRIPTION

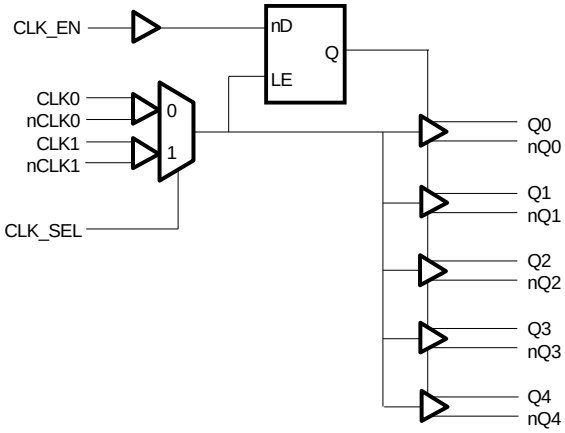
The ICS85304-01 is a low skew, high performance 1-to-5 clock fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS85304-01 has selectable clock inputs that accept any differential levels. The clock enable is synchronous which eliminates the runt clock pulses which occur during asynchronous enabling and disabling of the outputs.

Guaranteed output and part-to-part skew characteristics make the ICS85304-01 ideal for those applications demanding well defined performance and repeatability.

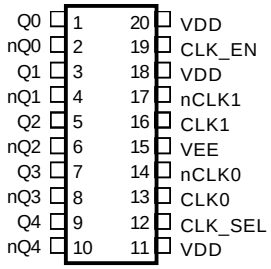
FEATURES

- 5 differential 3.3V LVPECL outputs
- Multiple clock inputs support redundant clock or multiple frequency applications
- Accepts any differential input levels (HSTL, LVDS, LVPECL, SSTL) and translates to 3.3V LVPECL levels
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Translates single-ended input signal to inverted 3.3V LVPECL levels with resistor bias on CLK input
- 35ps output skew
- LVCMOS / LVTTL control inputs
- 3.3V operating supply
- 20 lead TSSOP
- 0°C to 70°C ambient operating temperature
- Industrial temperature range available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85304-01

20-Lead TSSOP
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential clock outputs. 3.3V LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential clock outputs. 3.3V LVPECL interface levels.
5, 6	Q2, nQ2	Output		Differential clock outputs. 3.3V LVPECL interface levels.
7, 8	Q3, nQ3	Output		Differential clock outputs. 3.3V LVPECL interface levels.
9, 10	Q4, nQ4	Output		Differential clock outputs. 3.3V LVPECL interface levels.
11, 18, 20	VDD	Power		Power supply pin. Connect to 3.3V.
12	CLK_SEL	Input	Pulldown	Clock select input. When HIGH selects CLK1, nCLK1 inputs. When LOW selects CLK0, nCLK0.
13	CLK0	Input	Pulldown	Non-inverting differential clock input. Any differential level.
14	nCLK0	Input	Pullup	Inverting differential clock input. Any differential level.
15	VEE	Power		Power supply pin. Connect to ground.
16	CLK1	Input	Pulldown	Non-inverting differential clock input. Any differential level.
17	nCLK1	Input	Pullup	Inverting differential clock input. Any differential level.
19	CLK_EN	Input	Pullup	Synchronous clock enable. When HIGH clock outputs follow clock input. When LOW, Q outputs are forced low. LVTTL / LVCMOS interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	CLK0, nCLK0			TBD		pF
		CLK1, nCLK1			TBD		pF
		CLK_EN, CLK_SEL			TBD		pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3A. CONTROL INPUTS FUNCTION TABLE

Inputs		Outputs	
CLK_EN	**CLK_SEL**	**Q0 thru Q4**	**nQ0 thru nQ4**
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	Active	Active
1	1	Active	Active

In the active mode the state of the output is a function of the CLK0, nCLK0 and CLK1, nCLK1 inputs as described in Table 3B.

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK0 or CLK1	**nCLK1 or nCLK1**	**Q0 thru Q4**	**nQ0 thru nQ4**		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential input be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a 10KΩ resistor from the input pin to VDD, a 10KΩ resistor from the input pin to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is VDD/2 ±300mV.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDD + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD	Power Supply Voltage		3.135	3.3	3.465	V
IEE	Power Supply Current				55	mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	nCLK0, nCLK1	VDD = VIN = 3.465V			5	µA
		CLK0, CLK1	VDD = VIN = 3.465V			150	µA
IIL	Input Low Current	nCLK0, nCLK1	VDD = 3.465V, VIN = 0V	-150			µA
		CLK0, CLK1	VDD = 3.465V, VIN = 0V	-5			µA
VPP	Peak-to-Peak Input Voltage			0.15		1.3	V
VCMR	Common Mode Input Voltage			1.5		VDD	V

TABLE 4C. LVCMOS / LVTTL CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK_EN, CLK_SEL		2		3.765	V
VIL	Input Low Voltage	CLK_EN, CLK_SEL		-0.3		0.8	V
IIH	Input High Current	CLK_EN				5	µA
		CLK_SEL				150	µA
IIL	Input Low Current	CLK_EN		-150			µA
		CLK_SEL		-5			µA

TABLE 4D. LVPECL DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1, 2	VDD = 3.3V	1.9		2.3	V
VOL	Output Low Voltage; NOTE 1, 2	VDD = 3.3V	1.2		1.6	V
VSWING	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Noted output levels are for VDD equal to 3.3V. Output levels will vary 1:1 with VDD.
NOTE 2: Outputs terminated with 50Ω s to VDD - 2V. The power dissipation of a terminated output pair is 30mW.

TABLE 5. AC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				650	MHz
tpLH	Propagation Delay, Low-to-High; NOTE 2	66.7 ≤ *f* ≤ 650MHz	1.0		2.1	ns
tpHL	Propagation Delay, High-to-Low; NOTE 2	66.7 ≤ *f* ≤ 650MHz	1.0		2.1	ns
tsk(o)	Output Skew; NOTE 3				35	ps
tsk(pp)	Part-to-Part; NOTE 4				150	ps
tjit(Ø)	Input-to-Output Jitter; NOTE 5				0	ps
tR	Output Rise Time	20% to 80% < 500MHz	275		650	ps
		20% to 80%≥ 500MHz	225		500	ps
tF	Output Fall Time	20% to 80% < 500MHz	275		650	ps
		20% to 80%≥ 500MHz	225		500	ps
tPW	Output Pulse Width		tCYCLE/2 - 40	tCYCLE/2	tCYCLE/2 + 40	ps
tS	Clock Enable Setup Time		1.0			ns
tH	Clock Enable Hold Time		0.5			ns
VSWING (AC)	Peak-to-Peak Output Voltage Swing		400		700	mV

NOTE 1: All parameters measured at 500MHz unless noted otherwise.
NOTE 2: Measured from the differential input crossing point to the differential output crossing point.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from the differential input cross point to the differential output crossing point.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Measured from the differential input cross point of like inputs to the differential output crossing point.
NOTE 5: Measured by triggering on input signal and measuring the largest displacement between output cycles.

PACKAGE OUTLINE - G SUFFIX

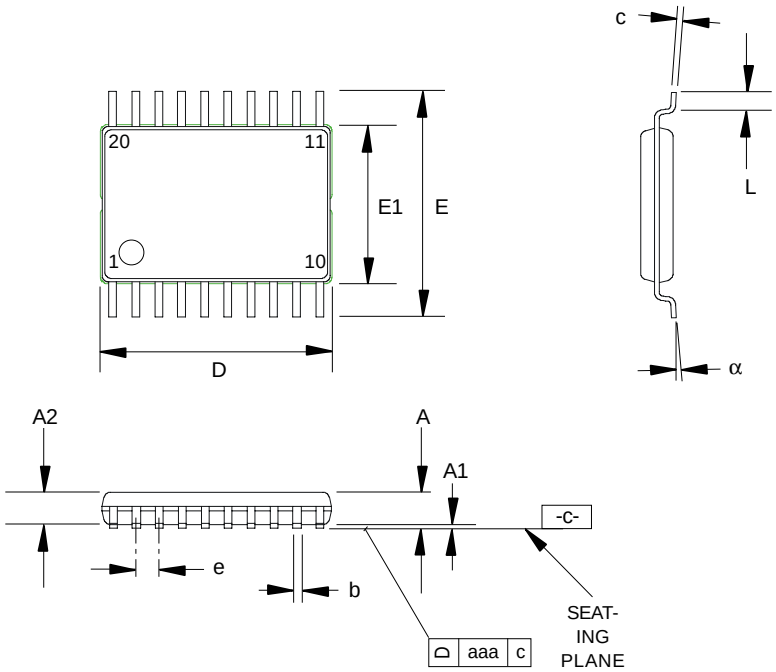


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
N	20			
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	4.90	5.10	.193	.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		.0256 BASIC	
L	0.45	0.75	.018	.030
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS85304AG-01	ICS85304AG-01	20 lead TSSOP	75 per tube	0°C to 70°C
ICS85304AG-01T	ICS85304AG-01	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C