IBM13T4644MPB
IBM13T8644MPB

4M/8M x 64 SDRAM SO DIMM

Features

- 144 Pin JEDEC Standard, 8 Byte Small Outline Dual-In-line Memory Module
- 4/8Mx64 Synchronous DRAM SO DIMM
- Performance:

		-10	Units
$\overline{CAS}$ Latency		3	
f_{CK}	Clock Frequency	100	MHz
t_{CK}	Clock Cycle	10	ns
t_{AC}	Clock Access Time	7	ns

- Inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have 4 internal banks
- Fully Synchronous to positive Clock Edge
- Data Mask for Byte Read/Write control
- Programmable Operation
- CAS Latency: 2, 3
  - Burst Type: Sequential or Interleave
  - Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
  - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 12/8/2 Addressing (Row/Column/Bank)
- 4096 refresh cycles distributed across 64ms
- Serial Presence Detect
- Card size: 2.66” x 1.15” x 0.096” (4MX64)
- Card size: 2.66" x 1.15" x 0.149" (8MX64)
- Gold contacts
- SDRAMs in TSOP Type II Package

Description

IBM13T8644MPB is a 144-pin Synchronous DRAM Small Outline Dual In-line Memory Module (SO DIMM) which is organized as a 8Mx64 high-speed memory array. The SO DIMM uses eight 4Mx16 SDRAMs in 400mil TSOP II packages. The IBM13T4644MPB is a 32MB single bank half populated version made with four 4Mx16 TSOP II devices. The SO DIMM achieves high speed data transfer rates of up to 100MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

The SO DIMM is intended to comply with all JEDEC standards set for 144 pin SDRAM SO DIMMs.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs.

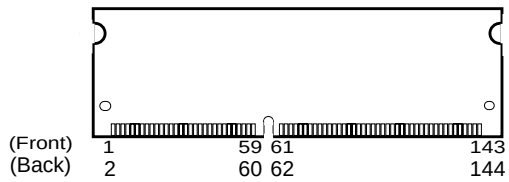
All inputs are sampled at the positive edge of each externally supplied clock (CK0, CK1). Internal operating modes are defined by combinations of the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$, DQMB, and CKE0 signals. A command decoder initiates the necessary timings for each operation. A 12 bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any access operation, the $\overline{CAS}$ latency, burst type, burst length, and burst operation type must be programmed into the SO DIMM by address inputs A0-A9 during the Mode Register Set cycle.

The SO DIMM uses serial presence detects implemented via a serial EEPROM using the two pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All IBM 144-pin SO DIMMs provide a high performance, flexible 8-byte interface in a 2.66" long space-saving footprint. Related products are in the EDO DRAM SO DIMM family.

Card Outline



Pin Description

CK0, CK1	Clock Inputs	DQ0 - DQ63	Data Input/Output
CKE0, CKE1*	Clock Enable	DQMB0 - DQMB7	Data Mask
$\overline{RAS}$	Row Address Strobe	V_{DD}	Power (3.3V)
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	NC	No Connect
$\overline{S0}$, $\overline{S1}$*	Chip Selects	SCL	Serial Presence Detect Clock Input
A0 - A9, A11	Address Inputs	SDA	Serial Presence Detect Data Input/Output
A10 /AP	Address Input/Autoprecharge	SA0-2	Serial Presence Detect Address Inputs
BA0 - BA1	SDRAM Bank Address		

Note: Pin Descriptions are NC for 4Mx64

Pinout

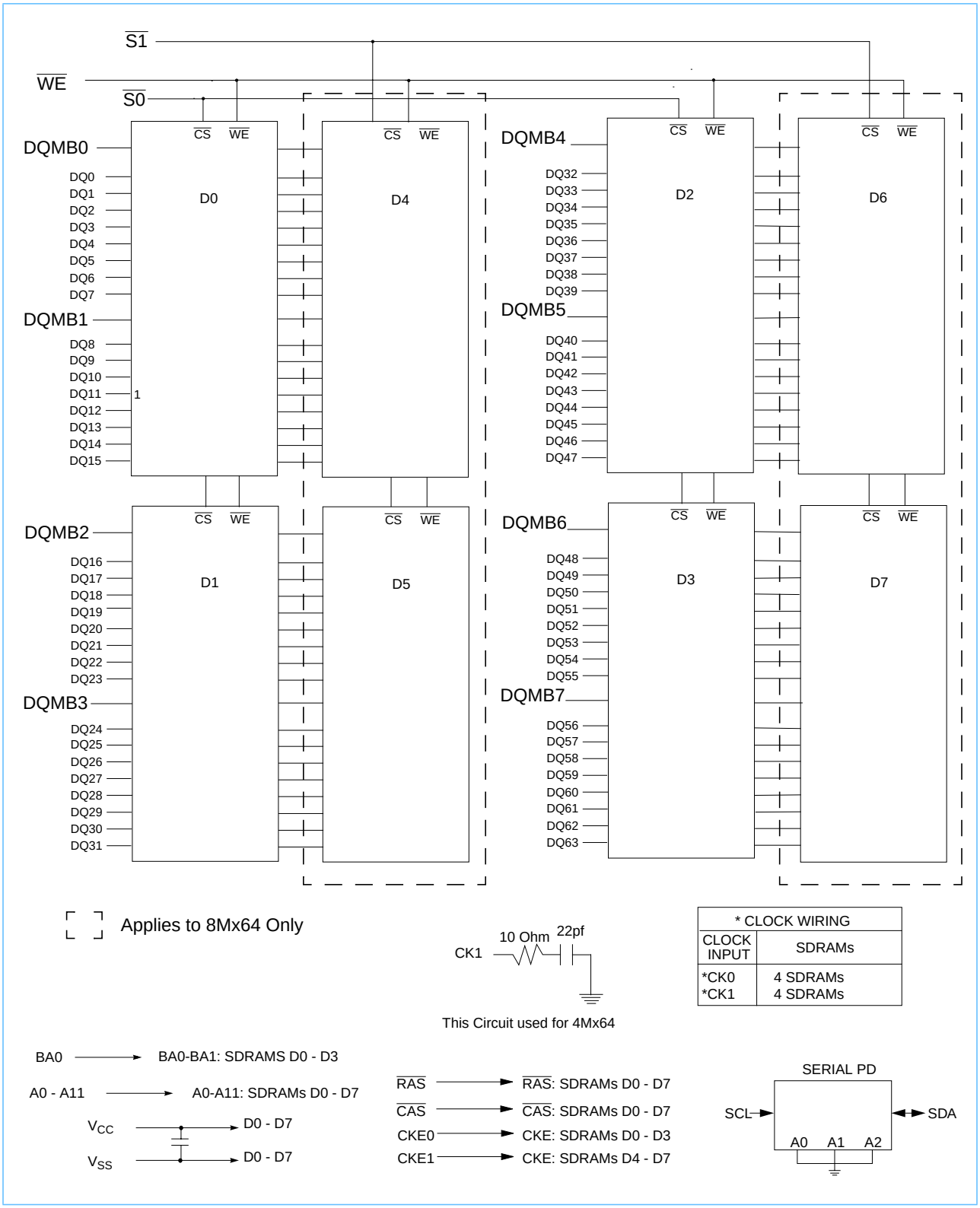
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	2	V_{SS}	37	DQ8	38	DQ40	71	$\overline{S1}$*	72	NC	107	V_{SS}	108	V_{SS}
3	DQ0	4	DQ32	39	DQ9	40	DQ41	73	DU	74	CK1*	109	A9	110	BA1
5	DQ1	6	DQ33	41	DQ10	42	DQ42	75	V_{SS}	76	V_{SS}	111	A10/AP	112	A11
7	DQ2	8	DQ34	43	DQ11	44	DQ43	77	NC	78	NC	113	V_{DD}	114	V_{DD}
9	DQ3	10	DQ35	45	V_{DD}	46	V_{DD}	79	NC	80	NC	115	DQMB2	116	DQMB6
11	V_{DD}	12	V_{DD}	47	DQ12	48	DQ44	81	V_{DD}	82	V_{DD}	117	DQMB3	118	DQMB7
13	DQ4	14	DQ36	49	DQ13	50	DQ45	83	DQ16	84	DQ48	119	V_{SS}	120	V_{SS}
15	DQ5	16	DQ37	51	DQ14	52	DQ46	85	DQ17	86	DQ49	121	DQ24	122	DQ56
17	DQ6	18	DQ38	53	DQ15	54	DQ47	87	DQ18	88	DQ50	123	DQ25	124	DQ57
19	DQ7	20	DQ39	55	V_{SS}	56	V_{SS}	89	DQ19	90	DQ51	125	DQ26	126	DQ58
21	V_{SS}	22	V_{SS}	57	NC	58	NC	91	V_{SS}	92	V_{SS}	127	DQ27	128	DQ59
23	DQMB0	24	DQMB4	59	NC	60	NC	93	DQ20	94	DQ52	129	V_{DD}	130	V_{DD}
25	DQMB1	26	DQMB5	VOLTAGE KEY				95	DQ21	96	DQ53	131	DQ28	132	DQ60
27	V_{DD}	28	V_{DD}	61	CK0	62	CKE0	97	DQ22	98	DQ54	133	DQ29	134	DQ61
29	A0	30	A3	63	V_{DD}	64	V_{DD}	99	DQ23	100	DQ55	135	DQ30	136	DQ62
31	A1	32	A4	65	$\overline{RAS}$	66	$\overline{CAS}$	101	V_{DD}	102	V_{DD}	137	DQ31	138	DQ63
33	A2	34	A5	67	$\overline{WE}$	68	CKE1*	103	A6	104	A7	139	V_{SS}	140	V_{SS}
35	V_{SS}	36	V_{SS}	69	$\overline{S0}$	70	NC	105	A8	106	BA0	141	SDA	142	SCL
												143	V_{DD}	144	V_{DD}

Note: * Pin Assignments are NC for 4Mx64

Ordering Information

Part Number	Organization	Clock Cycle	Leads	Dimension	Power
IBM13T4644MPB-10T	4Mx64	10ns	Gold	2.66" x 1.15" x 0.096"	3.3V
IBM13T8644MPB-10T	8Mx64	10ns	Gold	2.66" x 1.15" x 0.149"	3.3V

4M/8Mx64 SDRAM SO DIMM Block Diagram



IBM13T4644MPB
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4M/8M x 64 SDRAM SO DIMM

Serial Presence Detect (Part 1 of 2)

Byte #	Description		SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production		128	80	
1	Total Number of Bytes in Serial PD device		256	08	
2	Fundamental Memory Type		SDRAM	04	
3	Number of Row Addresses on Assembly		12	0C	
4	Number of Column Addresses on Assembly		8	08	
5	Number of DIMM Banks	4Mx64	1	01	
		8Mx64	2	02	
6 - 7	Data Width of Assembly		x64	4000	
8	Voltage Interface Level of this Assembly		LVTTL	01	
9	SDRAM Device Cycle Time at CL=3		10.0ns	A0	
10	SDRAM Device Access Time from Clock at CL=3		7.0ns	70	
11	DIMM Configuration Type		Non-Parity	00	
12	Refresh Rate/Type		SR/1x(15.625µs)	80	
13	Primary SDRAM Device Width		x16	10	
14	Error Checking SDRAM Device Width		N/A	00	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access		1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported		1,2,4,8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks		4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported		2, 3	06	
19	SDRAM Device Attributes: $\overline{CS}$ Latency		0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency		0	01	
21	SDRAM Module Attributes		Unbuffered	00	
22	SDRAM Device Attributes: General		Wr-1/Rd Burst, Precharge All, Auto-Precharge, V_{DD} ±10%	0E	
23	Minimum Clock Cycle at CL=2		15.0ns	F0	
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2		8.0ns	80	
25	Minimum Clock Cycle Time at CL=1		N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=1		N/A	00	
27	Minimum Row Precharge Time (t_{RP})		30ns	1E	
28	Minimum Row Active to Row Active delay (t_{RRD})		20ns	14	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})		30ns	1E	
30	Minimum $\overline{RAS}$ Pulse width (t_{RAS})		60ns	3C	
31	Module Bank Density		32MB	08	
32	Address and Command Setup Time Before Clock		3.0	30	
33	Address and Command Setup Time After Clock		1.0	10	
34	Data Input Setup Time Before Clock		3.0	30	
35	Data Input Hold Time After Clock		1.0	10	
36 - 61	Reserved		Undefined	00	
62	SPD Revision		02	02	
63	Checksum for bytes 0 - 62		Checksum Data	cc	1
64 - 71	Manufacturers' JEDEC ID Code		IBM	A400000000000000	
72	Module Manufacturing Location		Toronto, Canada	91	
			Vimercate, Italy	53	

1. cc = Checksum Data byte, 00-FF (Hex)
2. "R" = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte "R"
4. yy = Binary coded decimal year code, 00-99 (Decimal) '00-63 (Hex)
5. ww = Binary coded decimal week code, 01-52 (Decimal) '01-34 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)

Serial Presence Detect (Part 2 of 2)

Byte #	Description		SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
73 - 90	Module Part Number	4M x 64	ASCII '13T4644MP"R"-10T'	313354343634344D50rr 2D31305420202020	2, 3
		8M x 64	ASCII '13T8644MP"R"-10T'	313354383634344D50rr 2D31305420202020	
91 - 92	Module Revision Code		"R" plus ASCII blank	rr20	
93 - 94	Module Manufacturing Date		Year/Week Code	yyww	4, 5
95 - 98	Module Serial Number		Serial Number	ssssssss	6
99 - 125	Reserved		Undefined	00	
126	Module Supports this Clock Frequency		66MHz	66	
127	Attributes for Clock Frequency defined in byte 126		2, 3	C6	
128 - 255	Open for Customer Use		Undefined	00	

1. cc = Checksum Data byte, 00-FF (Hex)
2. "R" = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte "R"
4. yy = Binary coded decimal year code, 00-99 (Decimal) '00-63 (Hex)
5. ww = Binary coded decimal week code, 01-52 (Decimal) '01-34 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)

Recommended DC Operating Conditions (T_A= 0 to 70°C)

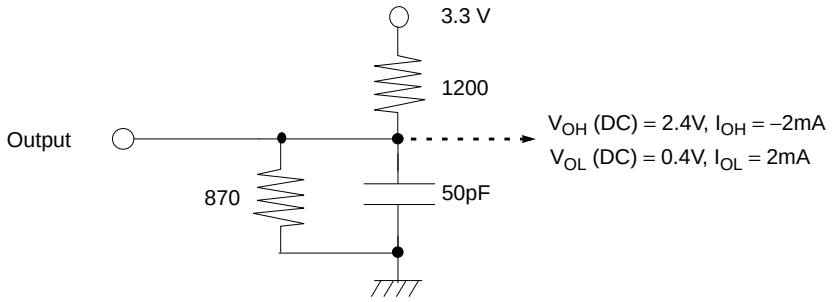
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	3.0	V_{DD} + 0.3	V	1
V_{IL}	Input Low Voltage	–0.3	0.0	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Organization		Units
		4Mx64 Max.	8Mx64 Max	
C_{I1}	Input Capacitance (A0 - A9, A10/AP, BA0, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	37	53	pF
C_{I2}	Input Capacitance (CKE, CKE1)	33	33	pF
C_{I3}	Input Capacitance ($\overline{S0}$, $\overline{S1}$)	34	34	pF
C_{I4}	Input Capacitance (CK0, CK1)	40	40	pF
C_{I5}	Input Capacitance (DQMB0 - DQMB7)	8	12	pF
C_{I6}	Input Capacitance (SCL)	12	12	pF
C_{IO1}	Input/Output Capacitance (DQ0 - DQ63)	12	18	pF
C_{IO2}	Input/Output Capacitance (SDA)	15	15	pF

DC Output Load Circuit



Output Characteristics (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter		4x64 Min.	4x64 Max.	8x64 Min.	8x64 Max.	Units	Notes
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ V_{DD}), All Other Pins Not Under Test = 0V	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0, CK0, A0-A9, A10/AP, A11, BA0	–4	+4	–8	+8	µA	
		$\overline{S0}$	–4	+4	–8	+8		
		$\overline{S1}$	—	—	–4	+4		
		DQMB0-7	–1	+1	–2	+2		
		SCL	–2	+2	–4	+4		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ V_{DD})	DQ0 - 63	–1	+1	–2	+2	µA	
		SDA	–2	+2	–2	+2		
V_{OH}	Output Level (LVTTL) Output "H" Level Voltage (I_{OUT} = –2.0mA)		2.4	—	2.4	—	V	1
V_{OL}	Output Level (LVTTL) Output "L" Level Voltage (I_{OUT} = +2.0mA)		—	0.4	—	0.4		

1. See DC output load circuit.

Operating, Standby and Refresh Currents (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

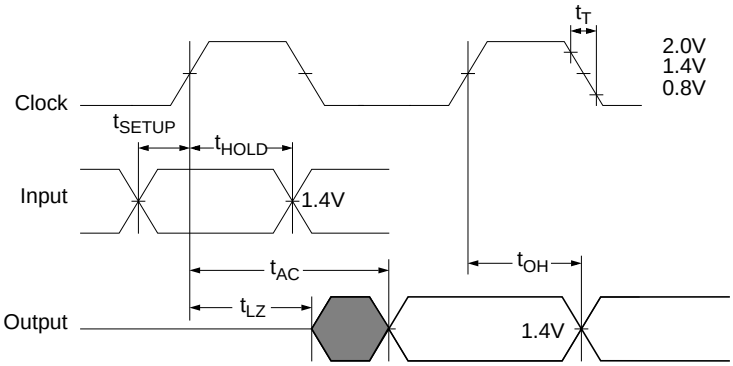
Parameter	Symbol	Test Condition	Organization		Units	Notes
			4Mx64	8Mx64		
Operating Current $t_{RC} = t_{RC}(min)$, t_{CK} = min Active-Precharge command cycling without Burst operation	I_{DD1}	1 bank operation	220	340	mA	1, 3, 4
Precharge Standby Current in Power Down Mode	I_{DD2P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{S0}$, $\overline{S1}$ =V_{IH}(min)	4	8	mA	2, 3, 10
	I_{DD2PS}	CKE ≤ V_{IL}(max), t_{CK} = Infinity, $\overline{S0}$, $\overline{S1}$ =V_{IH}(min)	4	8	mA	2
Precharge Standby Current in Non-Power Down Mode	I_{DD2N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{S0}$, $\overline{S1}$ =V_{IH} (min)	100	200	mA	2, 8
	I_{DD2NS}	CKE ≥ V_{IH}(min), t_{CK} = Infinity, $\overline{S0}$, $\overline{S1}$ =V_{IH} (min)	20	40	mA	2
No Operating Current (Active state: 4 bank)	I_{DD3N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{S0}$, $\overline{S1}$ =V_{IH} (min)	120	240	mA	2, 8
	I_{DD3P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{S0}$, $\overline{S1}$ =V_{IH} (min) (Power Down Mode)	28	56	mA	2, 9, 10
Burst Operating Current	I_{DD4}	t_{CK} = min, Read/ Write command cycling	360	480	mA	1, 4, 8
Auto (CBR) Refresh Current	I_{DD5}	t_{CK} = min, CBR command cycling	440	560	mA	1, 8
Self Refresh Current	I_{DD6}	CKE0 ≤ 0.2V	1.6	3.2	mA	2
Serial PD Device Standby Current	I_{SB5}	V_{IN} = GND or V_{DD}	30	30	µA	5
Serial PD Device Active Power Supply Current	I_{CCA}	SCL Clock Frequency = 100KHz	1	1	mA	6

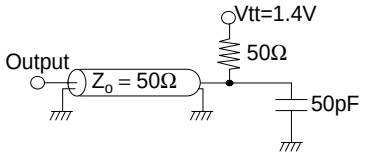
1. For the 8Mx64 card (2 bank) the specified values are for one DIMM bank in the specified mode, and the other DIMM bank in Active Standby (I_{DD3N}).
2. For the 8Mx64 card (2 bank) the specified values are for both DIMM banks operating in the specified mode.
3. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed once during t_{CK} (min).
4. The specified values are obtained with the output open.
5. V_{DD} = 3.3V
6. Input pulse levels V_{DD} x 0.1 to V_{DD} x 0.9, input rise and fall times 10ns, input and output timing levels V_{DD} x 0.5, output load 1 TTL gate and CL=100pf.
7. Input signals are changed once during t_{CK} (min).
8. Input signals are changed once during three clock cycles.
9. Active Standby current will be higher if clock suspend is entered during a Burst Read cycle (add 1mA per DQ).
10. Input signals are stable.

AC Characteristics (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

1. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the 1.40V crossover point.
3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume t_T=1ns.
5. In addition to meeting the transition rate specification, the clock and CKEn must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

AC Characteristics Diagrams





AC Output Load Circuit

Clock and Clock Enable Parameters

Symbol	Parameter	–10		Units	Notes
		Min.	Max.		
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	10	1000	ns	
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	15	1000	ns	1
t_{AC3}	Clock Access Time, $\overline{CAS}$ Latency = 3	—	7	ns	2
t_{AC2}	Clock Access Time, $\overline{CAS}$ Latency = 2	—	8	ns	2
t_{CKH}	Clock High Pulse Width	3	—	ns	3
t_{CKL}	Clock Low Pulse Width	3	—	ns	3
t_{CES}	Clock Enable Set-up Time	3	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	ns	
t_{SB}	Power down mode Entry Time	0	10	ns	
t_T	Transition Time (Rise and Fall)	0.5	10	ns	

1. For 66MHz clock, $\overline{CAS}$ Latency = 2.
2. Access time is measured at 1.4V. See AC output load circuit above.
3. t_{CKH} is the pulse width of CK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CK measured from the negative edge to the positive edge referenced to V_{IL} (max).

Common Parameters

Symbol	Parameter	–10		Units	Notes
		Min.	Max.		
t_{CS}	Command Setup Time	3	—	ns	
t_{CH}	Command Hold Time	1	—	ns	
t_{AS}	Address and Bank Select Set-up Time	3	—	ns	
t_{AH}	Address and Bank Select Hold Time	1	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	30	—	ns	1
t_{RC}	Bank Cycle Time	90		ns	1
t_{RAS}	Active Command Period	60	100000	ns	1
t_{RP}	Precharge Time	30	—	ns	1
t_{RRD}	Bank to Bank Delay Time	20	—	ns	1
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	—	CLK	
t_{RSC}	Mode Register Set Cycle Time	20	—	ns	1

1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Refresh Cycle

Symbol	Parameter	–10		Units	Notes
		Min.	Max.		
t_{REF}	Refresh Period	—	64	ms	1
t_{SREX}	Self Refresh Exit Time	10	—	ns	

1. 4096 cycles.

Read Cycle

Symbol	Parameter	–10		Units	Notes
		Min.	Max.		
t_{OH}	Data Out Hold Time	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	0	—	ns	
t_{HZ3}	Data Out to High Impedance Time	3	7	ns	1
t_{HZ2}	Data Out to High Impedance Time	3	8	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels

Write Cycle

Symbol	Parameter	–10		Units
		Min.	Max.	
t_{DS}	Data In Set-up Time	3	—	ns
t_{DH}	Data In Hold Time	1	—	ns
t_{DPL3}	Data input to Precharge, CL=3	10	—	ns
t_{DPL2}	Data input to Precharge, CL=2	15	—	ns
t_{DQW}	DQM Write Mask Latency	0	—	CLK

Presence Detect Read and Write Cycle

Symbol	Parameter	Min.	Max.	Units	Notes
f_{SCL}	SCL Clock Frequency		100	kHZ	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns	
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs	
t_{LOW}	Clock Low Period	4.7		µs	
t_{HIGH}	Clock High Period	4.0		µs	
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs	
$t_{HD:DAT}$	Data in Hold Time	0		µs	
$t_{SU:DAT}$	Data in Setup Time	250		ns	
t_r	SDA and SCL Rise Time		1	µs	
t_f	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs	
t_{DH}	Data Out Hold Time	300		ns	
t_{WR}	Write Cycle Time		15	ms	1

1. The Write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal Erase/Program cycle. During the Write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address

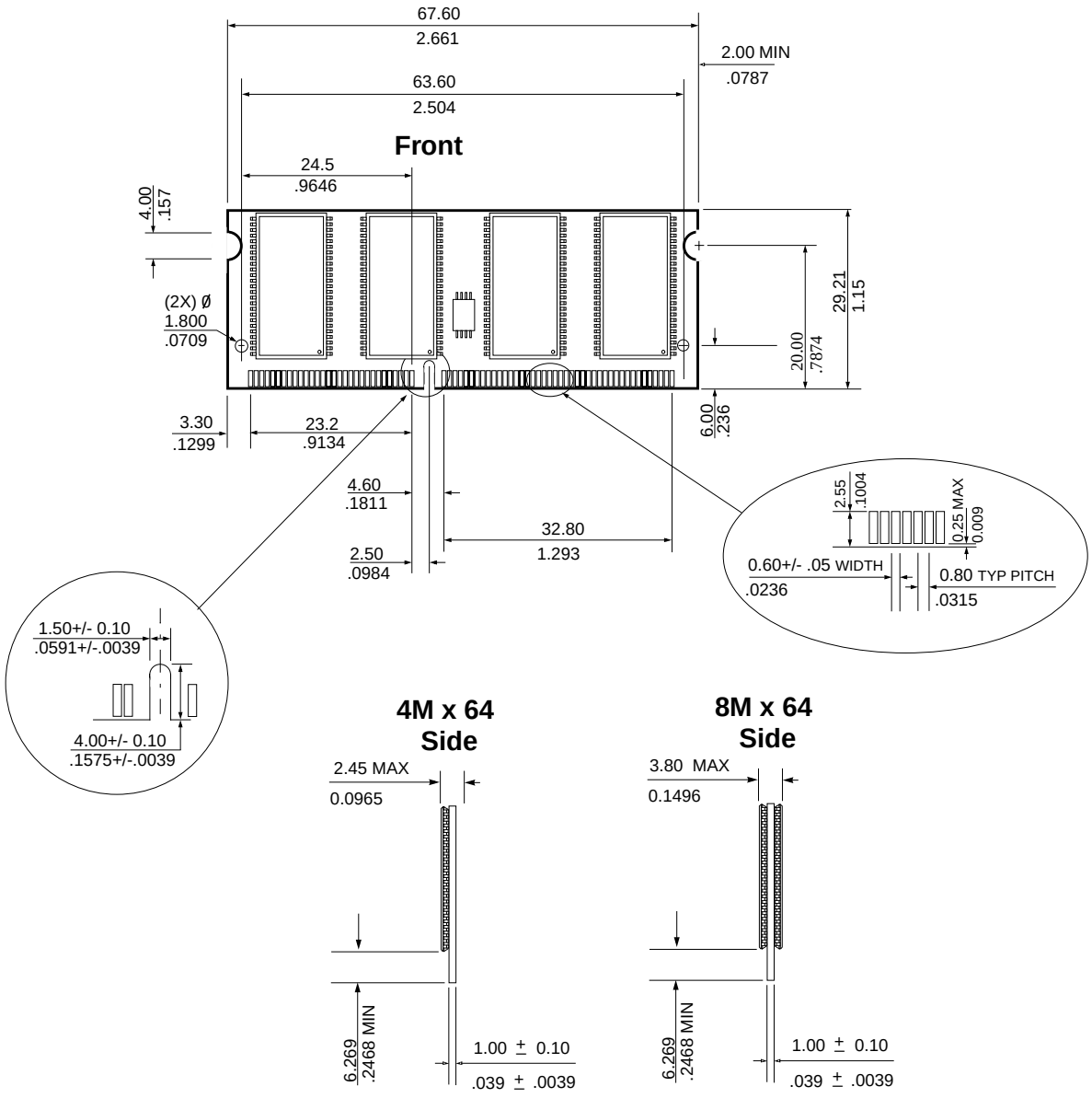
Functional Description and Timing Diagrams

Refer to the IBM 64Mb Synchronous DRAM data sheet, document 19L3264.E35855A, for the functional description and timing diagrams for SDRAM operation.

Refer to the IBM Application Notes: *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

All AC timing information refers to the timings at the SDRAM devices.

Layout Drawing



Note: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Revision Log

Rev	Contents of Modification
4/98	Initial Release
6/98	Changes to leakage current, IDD3P, clock access to reflect changes to SDRAM specification. Updated Serial Presence Detect table with SPD rev2 data
9/98	Added Die Revision to part numbers
3/99	Changed DQ capacitance $C_{I01,}$ Changed I_{DD2P}, I_{DD2PS}, I_{DD3P}, I_{DD5P}
5/99	Changed line 127 in Serial Presence Detect table.

Discontinued (8/99 - last order; 12/99 - last ship)

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