Apollo 2 Chipset

Full Rate Hardware-Based Controllerless ADSL Chipset for PCs

Features

- ANSI T1.413 Issue 2, ITU-T G.992.1 (G.dmt) compliant
- PCI controller based 3 chip solution
- Discrete multitone (DMT) modulation
- Full rate operation with 8 Mbps downstream data rate and 640 kbps upstream rate
- Full rate adaptive modem at 32 kbps steps
- Up to 18,000 feet in distance
- Support for Windows® 98 and 2000 (NT 5.0)
- Low power consumption
- Integrated 32-bit 33 MHz master/slave interface
- PCI 2.1 power management specification compliant
- Full ATM protocol stacks implementation over ADSL, including ATM TC layer, ATM layer with traffic shaping, AAL layer (AAL5 & SAR), PPP over ATM and Classical IP over ATM for Windows 98/2000 (NT 5.0)
- Supports third party host-based V.90 solution support via standard AC'97-link interface
- UTOPIA specification level I v1.0 and level II v2.01 compliant

General Description

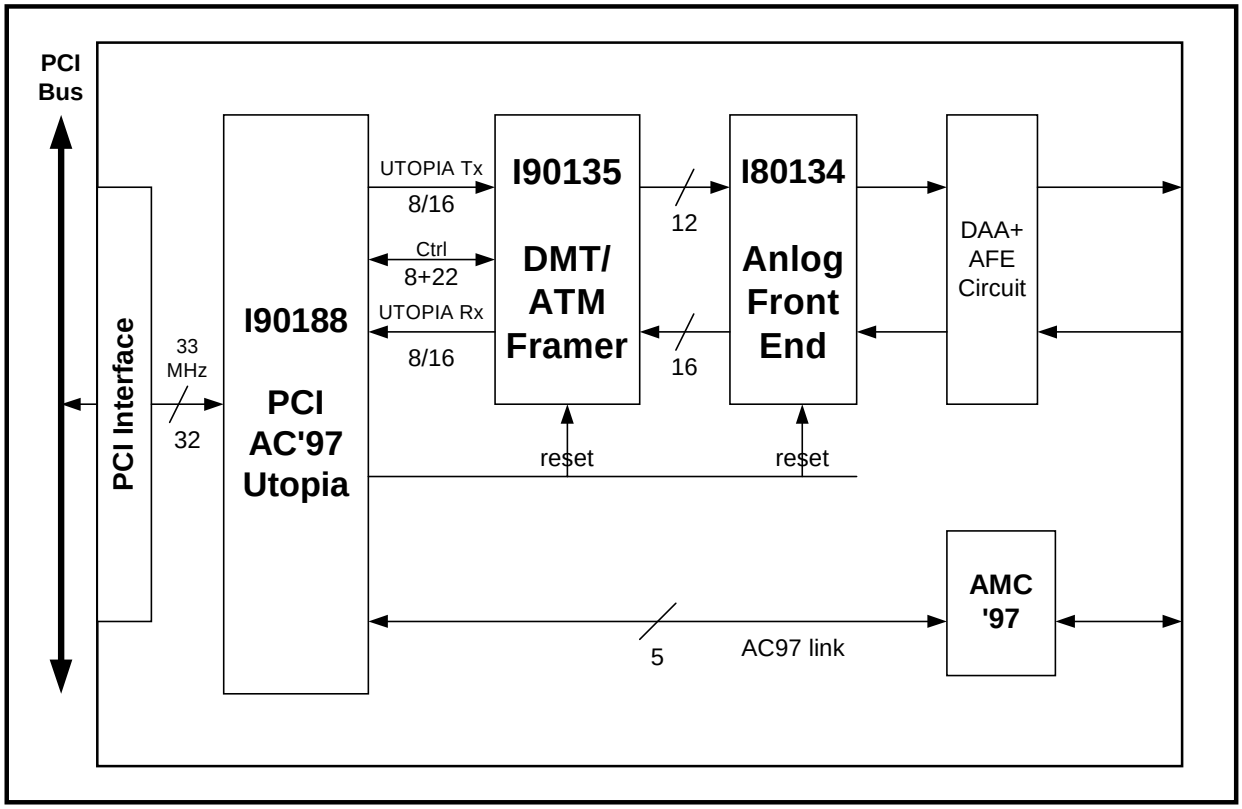
The Apollo 2 is a controllerless, full rate ADSL modem solution consisting of an integrated analog front end (I80134), a DMT transceiver and ATM framer (I90135), a PCI/Utopia interface chip (I90188) and Microsoft NDIS 5.0 miniport driver.

The Apollo 2 ADSL Chipset solution is designed for internal PCI modem cards and optimized for PCs.

The Apollo 2 Chipset eliminates the expensive microcontroller normally required in an ADSL modem. By leveraging a fraction of a PC's host processor's power, the Apollo 2 Chipset is able to achieve full ADSL rate as specified in ANSI T1.413 issue 2, ITU-T G.992.1 (G.dmt) at a much lower cost than competitive ADSL chipsets.

Apollo 2 also provides a host-based V.90 modem option via a standard AC'97-link. The selection between ADSL and V.90 can be done by simply changing the configuration in the software.

System Block Diagram



The ITeX ADSL Modem Chipset

The Apollo 2 Chipset solution consists of a DMT transceiver and ATM framer (I90135), an analog front end (I80134), a proprietary PCI Utopia interface (I90188) and NDIS 5.0 miniport driver.

The Chipset Functions

The chip functions are depicted in the system block diagram.

The functions included in each IC are as follows:

- **Analog Front End (I80134)**

This CMOS IC contains the analog functions required in the transceiver. In order to cope with the high attenuation of the line and in order to keep acceptable noise level of the signal, automatic gain control amplifiers have been implemented at the analog front of the transmission and reception paths. Then, the signal is passed through low pass filters to eliminate the echo signal and out-of-band interferences.

The AD and DA converters provide 12 bit resolution at 8.8 MHz sampling rate. In the transmission path, the control of the external hybrid drivers is done by an integrated highly linear line pre-driver.

- **DMT Transceiver and ATM Framer (I90135)**

This CMOS IC contains all the digital functional blocks required for the following functions.

1) DMT Modulation and Demodulation
The I90135 digitally implements the Quadrature-Amplitude Modulation (QAM) mapper/demapper, which allows up to 14 bits coding per tone (a constellation of 16383 points).

The device implements the necessary Inverse- and Fast Fourier Transform (IFFT, FFT), the Time- and Frequency-Domain Equalizer (TEQ, FEQ) plus timing units and voltage controlled Crystal oscillator (VCXO).

2) Framing Functions
The I90135 implements framing functions for the generic and ATM Transmission Convergence (TC) layers. The generic TC consists of data scrambling and Reed-Solomon error correction in both latency paths.

The ATM TC includes cell level functions (such as cell delineation, insertion/extraction of idle cells, payload scrambling, HEC check) and data frame generation.

3) Interface to ATMF standard UTOPIA bus
The IC contains the ATM related functions to interface with the ATM UTOPIA bus and supports level 1 and 2 modes.

- **PCI/Utopia Interface Chip (I90188)**

The I90188 consists of the following sub-systems.

- PCI Bus Master
  The PCI local bus interface has a 32-bit data path at 33 MHz. It has both DMA and PIO data transfer capability. DMA is for ADSL data transfer. PIO is for AC'97-link.

- UTOPIA-I and II Interface
  The ATM cell interface unit provides a standard data path between ATM layer (I90188) and PHY (ATM TC in I90135) devices. The ATM cell interface follows the ATM Forum standard UTOPIA specification, and it provides interface to I90135.
- DC'97
  DC'97 is the digital controller of the AC'97 specification. It can interface with any AC'97 compliant V.90 modem.
- I90135 Control Register
  The I90135 configuration interface unit provides the interface for the PC host to configure the registers in I90135 through PCI bus.

- **Apollo 2 Software**

The Apollo 2 Software is a Microsoft NDIS 5.0 miniport driver that provides the control functions of the I90135 (DMT Transceiver and ATM Framer). Additionally, ATM over ADSL functions implement the ATM protocol stacks, such as ATM layer with traffic shaping, AAL layer (AAL5 & SAR), PPP over ATM and Classical IP over ATM. The Apollo 2 Software is designed for Windows® 98 and Windows 2000 (NT 5.0) platforms.

Table 1: Summary of Characteristics ADSL Chips

I80134 4.3125 kHz tone spacing ADC 12 bit resolution, 8.832 MHz sampling rate DAC 12 bit resolution. 8.832 MHz sampling rate Analog/tunable low-pass filters Upstream channel fc 138 kHz, <1dB ripple Downstream channel fc 1100 kHz, <1 dB ripple AGC range: 0..31 dB in steps of 1 dB (Rx) -15..0 dB in steps of 1 dB (Tx predriver) Package: 64 LQFP
I80135 DMT modulation max number of bit per tone: 14 bits (16383 constellation points) max number of tones: 256 tones RS encoder: max codeword 256 bytes ATM Processor: ATM cell buffering Cell counting Insert/extract, idle/unassigned ATM cells (rate adaptation) ATM HEC generation module (CCITT 1.432) ATM payload scrambler: payload width: 48 bytes UTOPIA Level 1 and 2 Interface STM interface Package: 144 PQFP
I90188 PCI Interface Compliant with PCI Specification V2.2 32-bit address/data bus Bus frequency up to 33 MHz Supports PCI master/slave PIO Power management with D0 and D3 hot capability Supports both +3.3v or +5V PCI interfaces Utopia Interface Utopia Level 1 and 2 support 8-bit data path Full duplex Cell base only I90135 Configuration register Interface AC'97 Digital Controller Compliant with AC'97 Component Specification R2.1 Provides standard AC-link interface for AC'97 modem codec Supports both +3.3v or +5V AC'97 interfaces Dedicated PCB Control Pins +3.3V & +5V Power Supplies Package: 160-pin PQFP

Package

The I90135 is housed in a 144-pin PQFP package, the I80134 is available in a 64-pin LQFP, and the I90188 is in a 160-pin PQFP package.