Integrated Solutions Group

# 5 V CATV MODEM RF RECEIVER

# ISG1000

## FEATURES

- **DOCSIS COMPLIANT:**
  91-860 MHz RF BW
- **INTERFACES DIRECTLY WITH QAM DEMOD ICs**
- **LOW PHASE NOISE:**
  -83 dBc/Hz @ 10 KHz
- **BUILT IN DIPLEXER:**
  with >40 dB Isolation
- **BUSINESS CARD SIZE:**
  3.4" x 2.0" x 0.5"
- **RUGGED DESIGN/NO MICROPHONICS:**
  All SMD Components "Coiless"
- **LOW POWER CONSUMPTION:**
  RX: 1.2 Watts
- **EUROPEAN AND DIRECT SAMPLING VERSIONS AVAILABLE**

## DESCRIPTION AND APPLICATIONS

The ISG1000 is a complete RF receiver designed for use in digital cable modem and settop applications. The receiver integrates a DOCSIS compliant diplex filter, triple conversion receiver and incorporates RF path for external TX section (see Figure 1). The diplex filter provides over 40 dB of isolation between the TX band and the RX band. The receiver section provides channel selectivity and converts QAM carriers to low IF sampling frequency for digital signal processing.

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5 V, $V_{CC2}$ = 24 V, $T_A$ = 25°C)

| PART NUMBER | | | ISG1000 | | |
|---|---|---|---|---|---|
| **SYMBOLS** | **PARAMETERS** | **UNITS** | **MIN** | **TYP** | **MAX** |
| **RF Performance (Rx)** | | | | | |
| $f_{OP}$ | Operating Frequency Range | MHz | 91 | | 860 |
| | Input Signal Level | dBmV | -20 | | 15 |
| | Gain Range | dB | 25 | | 75 |
| $V_{AGC}$ | Automatic Gain Control Voltage RF | | 0 | | 3.3 |
| $V_{AGC}$ | Automatic Gain Control Voltage IF | | 0 | | 3.3 |
| $NF_{MAX}$ | Noise Figure (Max Gain) | dB | | 8 | 10 |
| | Phase Noise at 10 kHz Offset | dBc/Hz | | -83 | -80 |
| | LO Radiation at RF Input | dBm | | -40 | |
| | Resolution | KHz | | 62.5 | |
| | Lock Time | µsec. | | 600 | |
| | Input Impedance (Nominal) | ohms | | 75 | |
| $RL_{IN}$ | Input Return Loss | dB | 6 | | |
| | Channel Bandwidth USA | MHz | | 6 | |
| | Output Frequency[1] | MHz | 5.70 | 5.75 | 5.80 |
| | Passband Ripple | dB | | 1 | 2 |
| | Image Rejection | dB | 50 | | |
| | Inband Group Delay | ns | | | 100 |
| | CSO[2] | dBc | | | 45 |
| | CTB[2] | dBc | | | 45 |
| | Frequency Offset | KHz | -50 | | +50 |

Notes:
1. Optional Output Frequency of 43.75 MHz Available
2. 110 Channels at +15 dBmV/tone
3. Temperature performance parameters will vary slightly.

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5 V, $V_{CC2}$ = 24 V, $T_A$ = 25°C)

| PART NUMBER | | | ISG1000 | | |
|---|---|---|---|---|---|
| **SYMBOLS** | **PARAMETERS** | **UNITS** | **MIN** | **TYP** | **MAX** |
| **RF Performance Specs (Upstream)** | | | | | |
| | Operation frequency | MHz | 5 | | 42 |
| | Output Return Loss at F-connector | dB | 6 | | |
| | Insertion Loss | dB | | | 1.5 |
| | Isolation from Tx to Rx | dB | 40 | | |
| | Inband group delay | dsec | | | 100 |
| **Power Requirements** | | | | | |
| | Supply Voltage V1 Rx | V | 4.75 | 5 | 5.25 |
| | Supply Voltage V2 Rx | V | 20 | 24 | 31.5 |
| **Supply Current** | | | | | |
| $I_{CC1}$ (Rx) | Supply Current 1 (Rx) | mA | | 240 | 320 |
| $I_{CC2}$ (Rx) | Supply Current 2 (Rx) | mA | | 1.5 | 2 |
| **Physical Interface** | | | | | |
| | To the CATV Network<br><br>To the Motherboard | | | Female<br>F-Connector<br>16 Pin Header | |
| **Physical Dimensions** | | | | | |
| | L x W x H | | 3.4 x 2.0 x 0.5" | | |
| **Environmental Specs** | | | | | |
| $T_{OP}$ | Operating Temperature[3] | °C | -5 | | 60 |
| $T_{STG}$ | Storage Temperature | °C | -40 | | 75 |

## ABSOLUTE MAXIMUM RATINGS

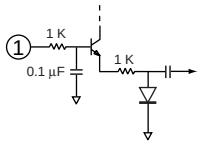
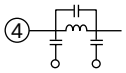
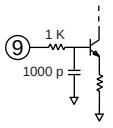
($T_C$ = 25 °C unless otherwise noted)

| SYMBOLS | PARAMETERS | UNITS | RATINGS |
|---|---|---|---|
| $V_{IN}$ | RF Input Voltage | dBmV | 60 |
| $V_{CC1}$ (Rx) | Supply Voltage 1 (Rx) | V | 6 |
| $V_{CC2}$ (Rx) | Supply Voltage 2 (Rx) | V | 35 |
| $T_{OP}$ | Operating Temperature | °C | -10 to 60 |
| $T_{STG}$ | Storage Temperature | °C | -55 to 150 |
| $T_{SOL}$ | Soldering Temperature | °C | 260 |
| $t_{SOL}$ | Soldering Time | sec. | 4 |

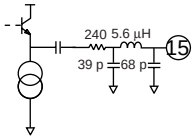
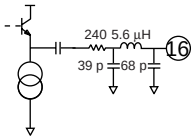
Note:

1. Operation in excess of any one of these parameters may result in permanent damage.

## PIN FUNCTIONS

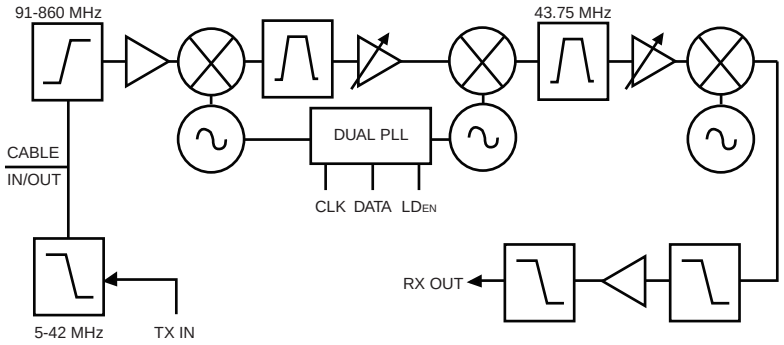
| Pin No. | Pin Name | Description | Equivalent Circuit |
|---|---|---|---|
| 1 | $RF_{AGC}$ | The $RF_{AGC}$ pin is used to adjust gain in the dual conversion tuner. This pin has a positive gain vs. AGC slope. 20 dB of gain control is available by varying the voltage from 0.5 V to 3.3 V. |  |
| 2 | N/C | | |
| 3 | N/C | | |
| 4 | $T_{XIN}$ | $T_{XIN}$ is the $T_X$ input to the diplexer. The input frequency range spans 5-42 MHz. |  |
| 5 | N/C | | |
| 6 | N/C | | |
| 7 | $V_{CC2}$ ($R_X$) | The $V_{CC2}$ ($R_X$) pin powers the loop filter for the first LO. A bias of 24 V - 30 V is required and maximum current draw is 2 mA. | |
| 8 | $V_{CC1}$ ($R_X$) | The $V_{CC1}$ ($R_X$) pin powers the entire $R_X$ section. A bias of 5 V is required and nominal current draw is 250 mA. | |
| 9 | $IF_{AGC}$ | The $IF_{AGC}$ pin is used to adjust gain in the final downconverter stage of the $R_X$ section. The pin has a positive gain vs. AGC slope. 30 dB of gain control is available by varying the voltage from 0.5 to 2.0 V. |  |
| 10 | GND | Ground. | |

## PIN FUNCTIONS

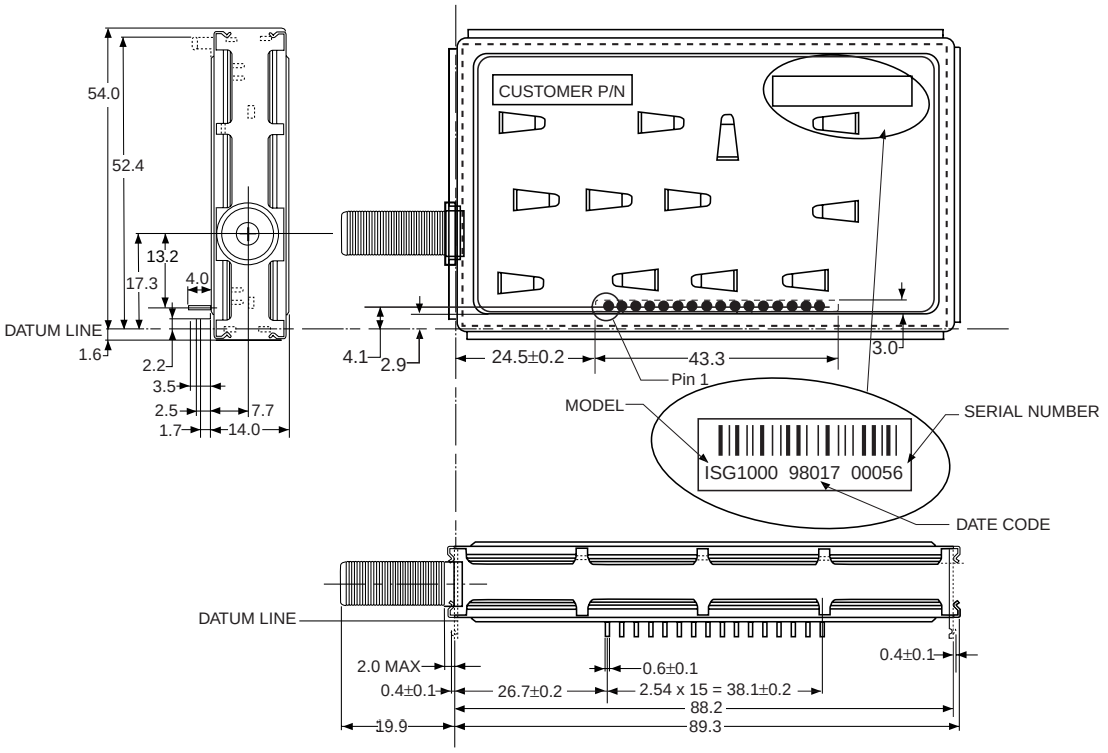
| Pin No. | Pin Name | Description | Equivalent Circuit |
|---|---|---|---|
| 11 | CLK | Clock pin for the dual PLL. High impedance CMOS input. Data for the various latches is clocked in on the rising edge into a 20-bit shift register. | |
| 12 | DATA | Serial data pin for the dual PLL. High impedance CMOS input. MSB entered first. The last two bits are the control bits. | |
| 13 | LDEN | Latch enable pin for the dual PLL. High impedance CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 latches determined by the 2 control bits. | |
| 14 | GND | Ground. | |
| 15 | IFOUT+ | Non-inverting final IF output. |   |
| 16 | IFOUT– | Inverting final IF output. |   |

Note:
1. For programming information, refer to National LMX2336 data sheet (http://www.national.com)

## FIGURE 1



## OUTLINE DIMENSIONS (Units in mm)




Pin Connections

1. RF AGC
2. NC
3. NC
4. TX IN
5. NC
6. NC
7. $V_{CC2}$ (RX)
8. $V_{CC1}$ (RX)
9. IF AGC
10. GND
11. CLK
12. DATA
13. LD EN
14. GND
15. IF OUT+
16. IF OUT–

**Table 1. Programmable Modes**

| C1 | C2 | R16 | R17 | R18 | R19 | R20 |
|---|---|---|---|---|---|---|
| 0 | 0 | RF2 Phase Detector Polarity | RF2 $I_{CP_O}$ | RF2 $D_O$ TRI-STATE | RF2 LD | RF2 $F_O$ |
| 0 | 1 | RF1 Phase Detector Polarity | RF1 $I_{CP_O}$ | RF1$D_O$ TRI-STATE | RF1 LD | RF1 $F_O$ |

| C1 | C2 | N19 | N20 |
|---|---|---|---|
| 1 | 0 | RF2 Prescaler | Pwdn RF2 |
| 1 | 1 | RF1 Prescaler | Pwdn RF1 |

**Table 2. Mode Select Truth Table**

| | Phase Detector Polarity[3] | $D_O$ TRI-STATE | $I_{CP_O}$[1] | RF1 Prescaler | RF2 Prescaler | Pwdn[2] |
|---|---|---|---|---|---|---|
| 0 | Negative | Normal Operation | LOW | 64/65 | 64/65 | pwrd up |
| 1 | Positive | TRI-STATE | HIGH | 128/129 | 128/129 | pwrd dn |

Notes:

1. The $I_{CP_O}$ LOW Current State = 1/4 x $I_{CP_O}$ HIGH Current.
2. Activitation of the RF2 PLL or RF1 PLL powerdown modes result in the disabling of the respective N counter divider and debiasing of its respective $f_{IN}$ inputs (to a high impedance state). The powerdown function is gated by the charge pump to prevent unwanted frequency jumps. Once the powerdown program mode is loaded, the part will go into powerdown mode when the charge pump reaches a TRI-STATE condition. The R counter and Oscillator functionality does not become disabled until both RF2 and RF1 powerdown bits are activated. The $OSC_{IN}$ is connected to $V_{CC}$ through a 100 kΩ resistor and the $OSC_{OUT}$ goes HIGH when this condition exists. The MICROWAVE™ control register remains active and capable of loading and latching data during all the powerdown modes.
3. Phase Detector Polarity
   Depending upon VCO characteristics, the R16 bits should be set accordingly:
   When VCO characteristics are positive like (1), R16 should be set HIGH, when VCO characteristics are negative like (2), R16 should be set LOW.

**VCO CHARACTERISTICS**

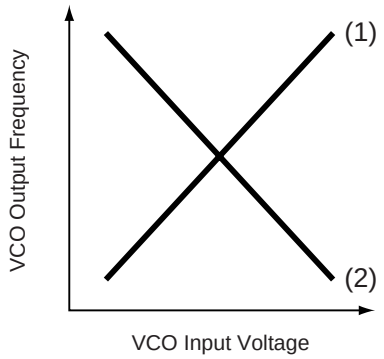


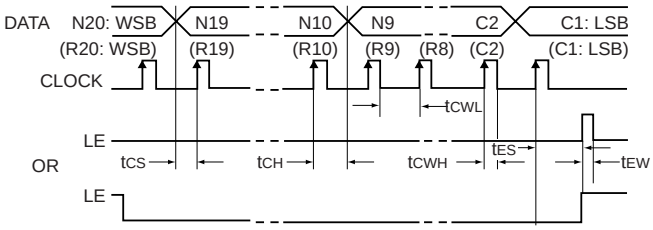

**Table 3. The FoLD Output Truth Table**

| RF1 R (19) (RF1 LD) | RF2 R (19) (RF2 LD) | RF1 R (20) (RF1 Fo) | RF2 R (20) (RF2 Fo) | FoLD Output State |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disabled[1] |
| 0 | 1 | 0 | 0 | RF2 Lock Detect[2] |
| 1 | 0 | 0 | 0 | RF1 Lock Detect[2] |
| 1 | 1 | 0 | 0 | RF1/RF2 Lock Detect[2] |
| X | 0 | 0 | 1 | RF2 Reference Divider Output |
| X | 0 | 1 | 0 | RF1 Reference Divider Output |
| X | 1 | 0 | 1 | RF2 Programmable Divider Output |
| X | 1 | 1 | 0 | RF1 Programmable Divider Output |
| 0 | 0 | 1 | 1 | Fastlock[3] |
| 0 | 1 | 1 | 1 | For internal use only |
| 1 | 0 | 1 | 1 | For internal use only |
| 1 | 1 | 1 | 1 | Counter Reset[4] |

X - Don't care condition

Notes:
1. When the FoLD output is disabled, it is actively pulled to a low logic state.
2. Lock detect output provided to indicate when the VCO frequency is in "lock". When the loop is locked and a lock detect mode is selected, the pin's output is HIGH, with narrow pulses LOW. In the RF1/RF2 lock detect mode a locked condition is indicated when RF2 and RF1 are both locked.
3. The Fastlock mode utilized the FoLD output pin to switch a second loop filter damping resistor to ground during fastlock operation. Activation of Fastlock occurs whenever the RF loop's Icpo magnitude bit #17 is selected HIGH (while the #19 and #20 mode bits are set for Fastlock).
4. The Counter Reset mode bits R19 and R20 when activated reset all counters. Upon removal of the Reset bits the N counter resumes counting in "close" alignment with R counter. (The maximum error is one prescaler cycle). If the Reset bits are activated the R counter is also forced to Reset, allowing smooth acquisition upon powering up.

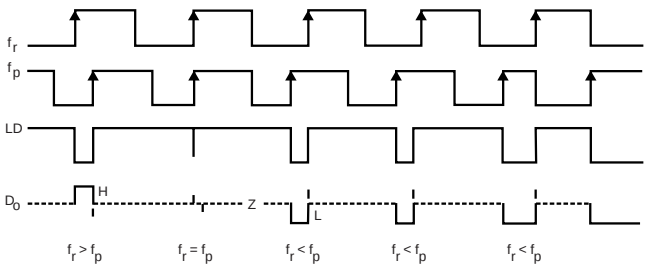
**Serial Data Input Timing**




Notes:
1. Parenthesis data indicates programmable reference divider data.
2. Data shifted into register on clock rising edge.
3. Data is shifted in MSB first.

Test Conditions:
The Serial Data Input Timing is tested using a symmetrical waveform around VCC/2. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2 V @ VCC = 2.7 V and 2.6 V @ VCC = 5.5 V.

**Phase Comparator and Internal Charge Pump Characteristics.**




Notes:
1. Phase difference detection range: -2π to +2π

2. The minimum width pump up and pump down current pulses occur at the Do pin when the loop is locked.