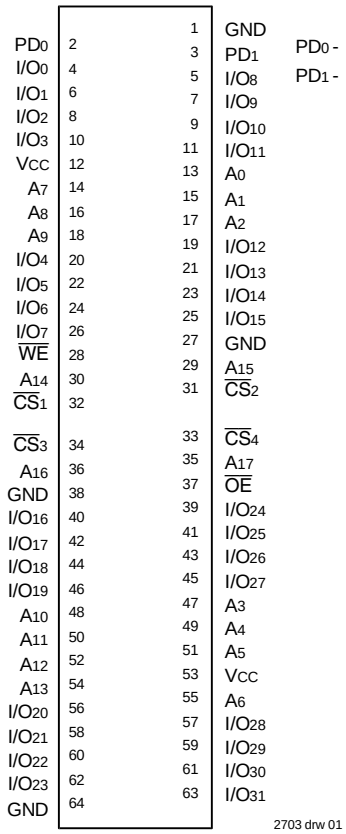
256K x 32
CMOS Static RAM Module

IDT7MP4045
IDT7MP4145

Features

- **High density 1 megabyte static RAM module (IDT7MP4145 upgradeable to 4 megabyte, IDT7MP4120)**
- **Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or 64 pin SIMM (Single In-line Memory Module) for IDT7MP4045 and 72 pin SIMM (Single In-line Memory Module) for IDT7MP4145**
- **Very fast access time: 15ns (max.)**
- **Surface mounted plastic components on an epoxy laminate (FR-4) substrate**
- **Single 5V (±10%) power supply**
- **Multiple GND pins and decoupling capacitors for maximum noise immunity**
- **Inputs/outputs directly TTL-compatible**

Pin Configuration 7MP4045(1)



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ZIP, SIMM
Top View

NOTE:

1. Pins 2 and 3 (PD_0 and PD_1) are read by the user to determine the density of the module. If PD_0 reads GND and PD_1 reads GND, then the module has a 256K depth.

Description

The IDT7MP4045/4145 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4045 is available with access time as fast as 10ns with minimal power consumption.

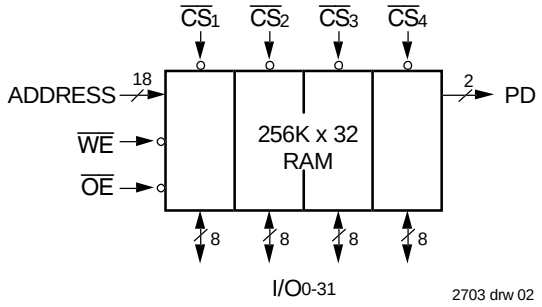
The IDT7MP4045 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64 pin SIMM (Single In-line Memory Module) where as the 7MP4145 is packaged in a 72 pin SIMM (Single In-line Memory Module). The 4045 ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.365 inches wide. The 7MP4045 ZIP is only 0.585 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4045/4145 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Identification pins are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD pins to determine a 256K depth.

The contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches minimum of selective gold.

Functional Block Diagram



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DECEMBER 1999

Pin Names

I/O_{0-31}	Data Inputs/Outputs
A_{0-17}	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_{0-1}	Depth Identification
V_{CC}	Power
GND	Ground
NC	No Connect

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Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	20	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	V_{IN} = 0V	70	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

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NOTE:
1. This parameter is guaranteed by design but not tested.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

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NOTE:
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%

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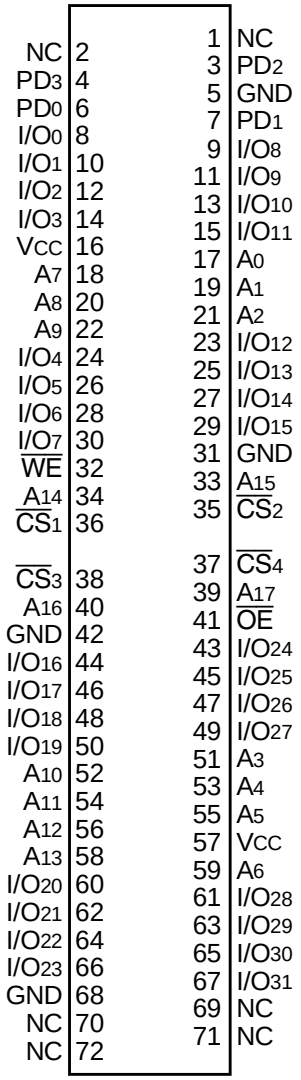
Pin Configuration 7MP4145[1]



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SIMM Top View

NOTE:
1. Pins 3,4,6,and 7 (PD_{0-3}) are read by the user to determine the density of the module. If PD_0, PD_1 read GND and PD_2, PD_3 read OPEN, then the module has a 256K depth.

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	D_{IN}	Active

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Absolute Maximum Ratings(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

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NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics
(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage Current (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Outputs Open	—	1360	mA
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, f = f_{MAX}, Outputs Open	—	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, f = 0 V_{IN} > V_{CC} - 0.2V or < 0.2V	—	120	mA

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AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

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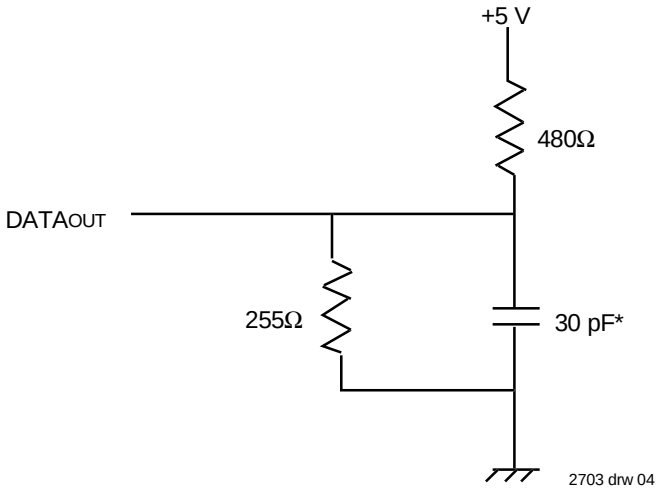

Figure 1. Output Load
*Includes scope and jig.

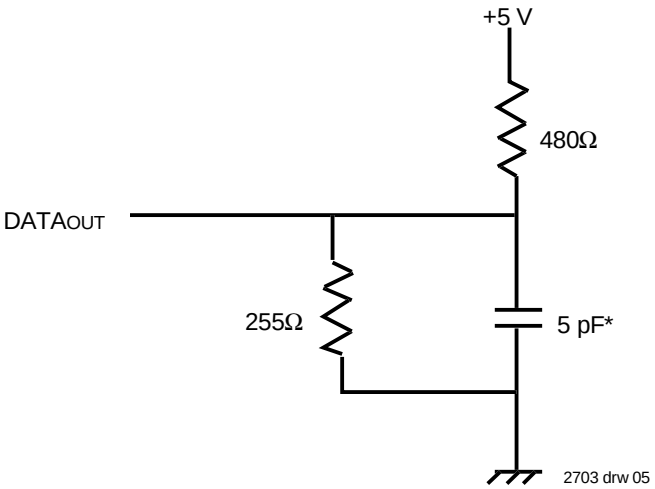

Figure 2. Output Load
(for t_{OLZ},t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

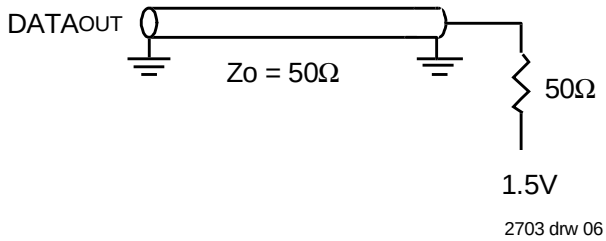

Figure 3. Alternate Output Load

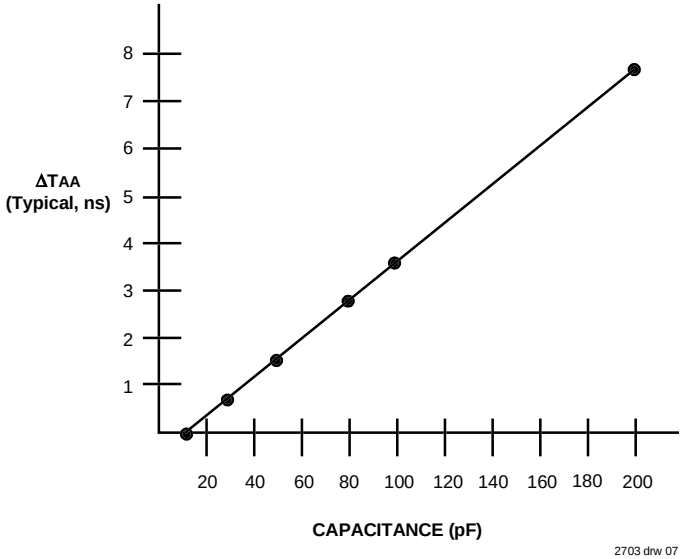

Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC Electrical Characteristics

(Vcc = 5V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP4045SxxZ, 7MP4045/4145SxxM						Unit
		-15		-20		-25		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	8	—	10	—	12	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	8	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	15	—	20	—	25	ns
Write Cycle								
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{CW}	Chip Select to End-of-Write	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	8	—	13	—	15	ns
t_{DW}	Data to Write Time Overlap	10	—	12	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	0	—	0	—	0	—	ns

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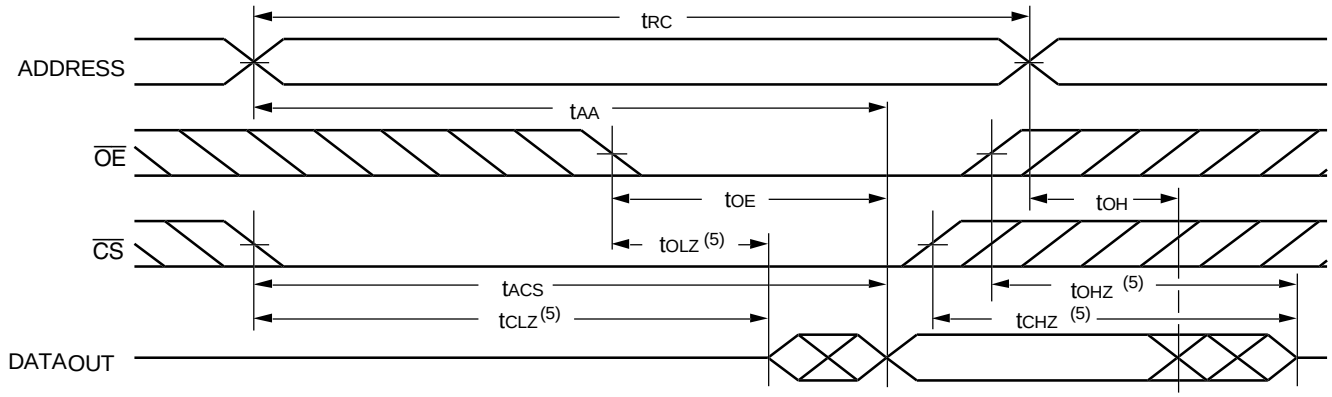
NOTE:

1. This parameter is guaranteed by design but not tested.

Timing Waveform of Read Cycle No. 1(1)



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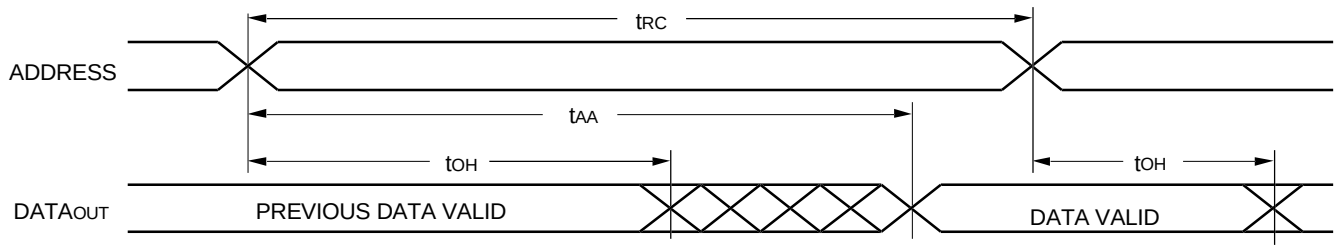
Timing Waveform of Read Cycle No. 2(1,2,4)



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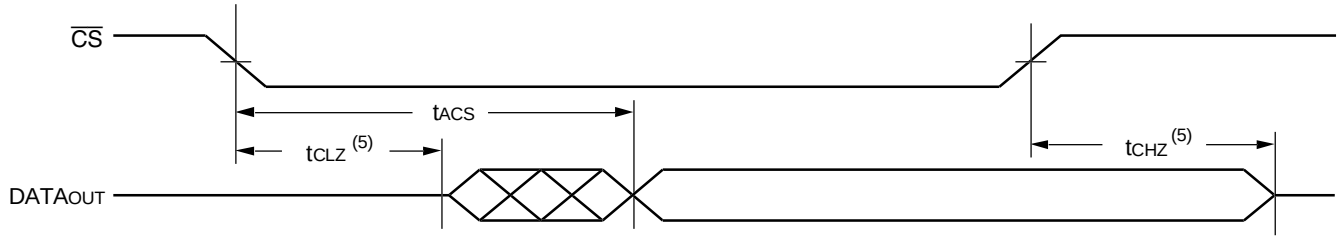
Timing Waveform of Read Cycle No. 3(1,3,4)



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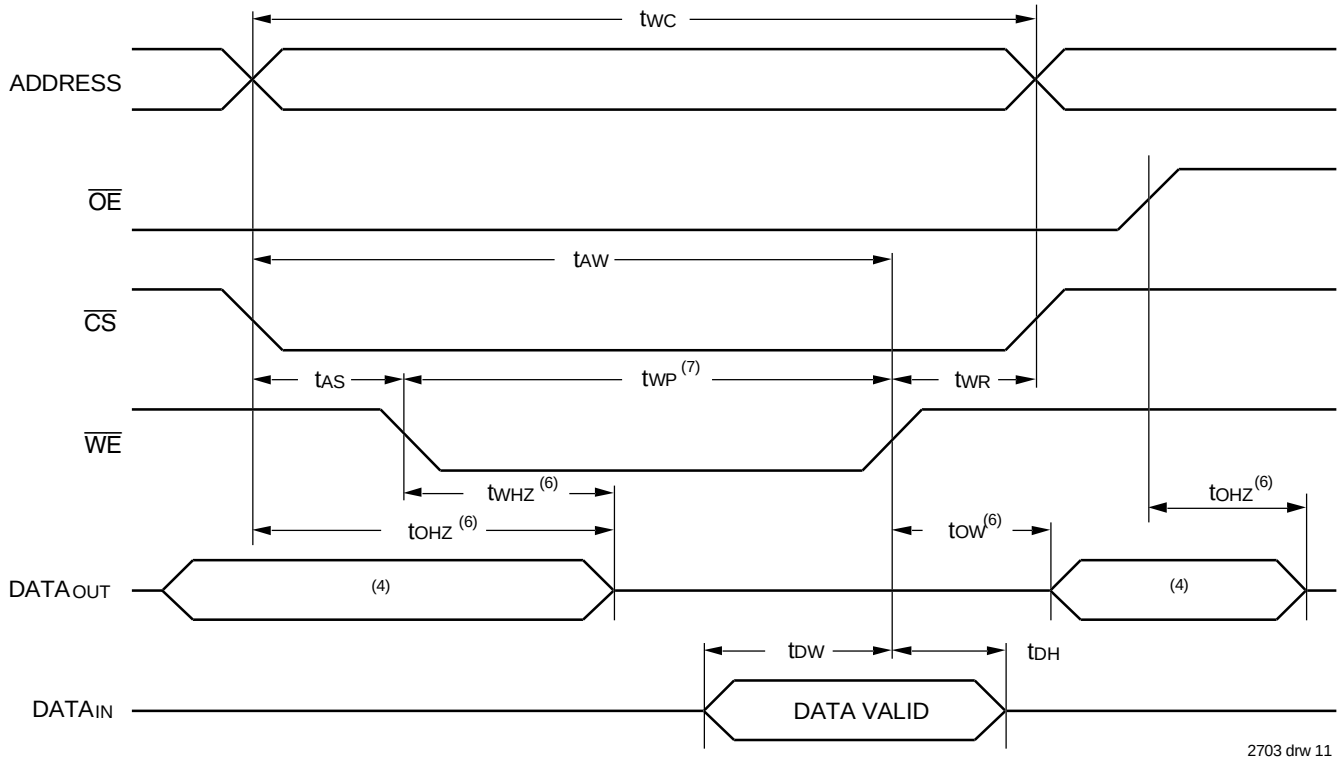
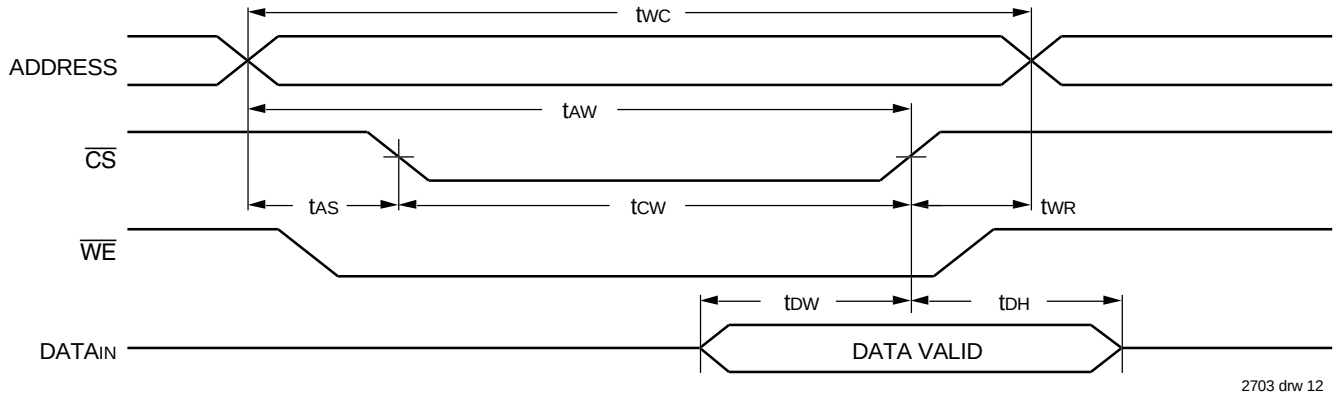
NOTES:

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled) (1,2,3,7)



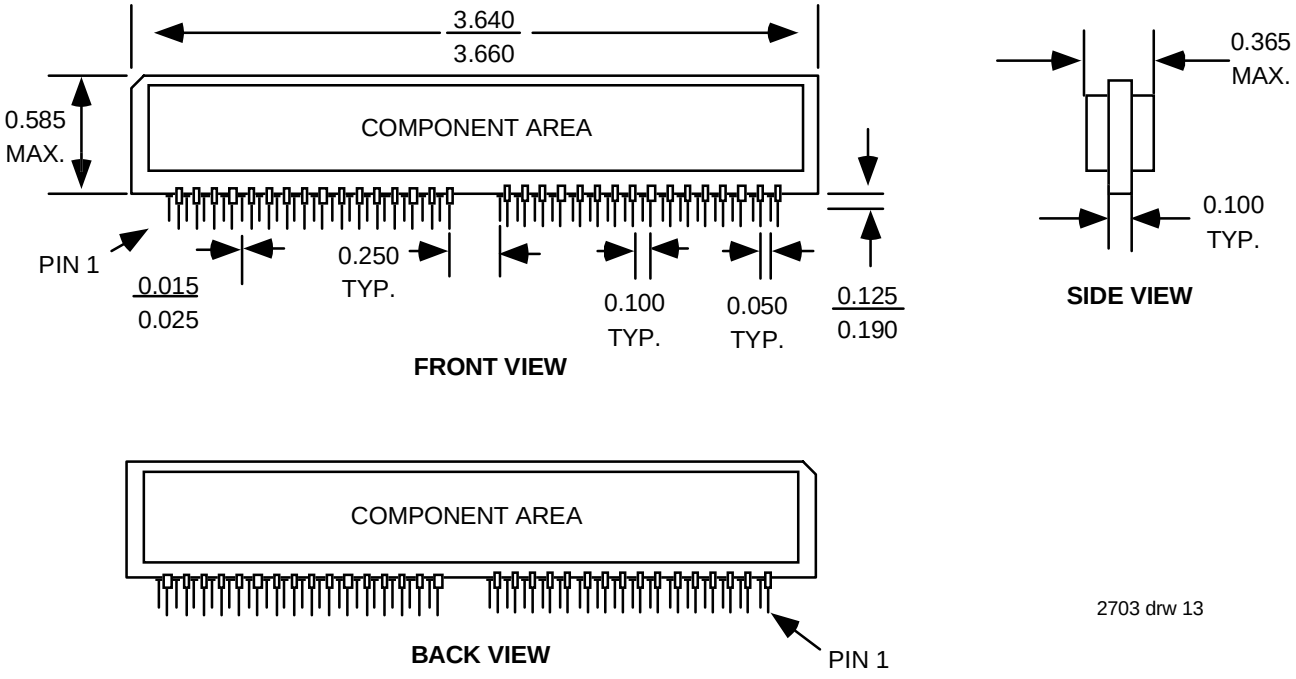
Timing Waveform of Wdite Cycle No. 2 ($\overline{CS}$ Controlled)(1,2,3,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

Package Dimensions

7MP4045 ZIP VERSION



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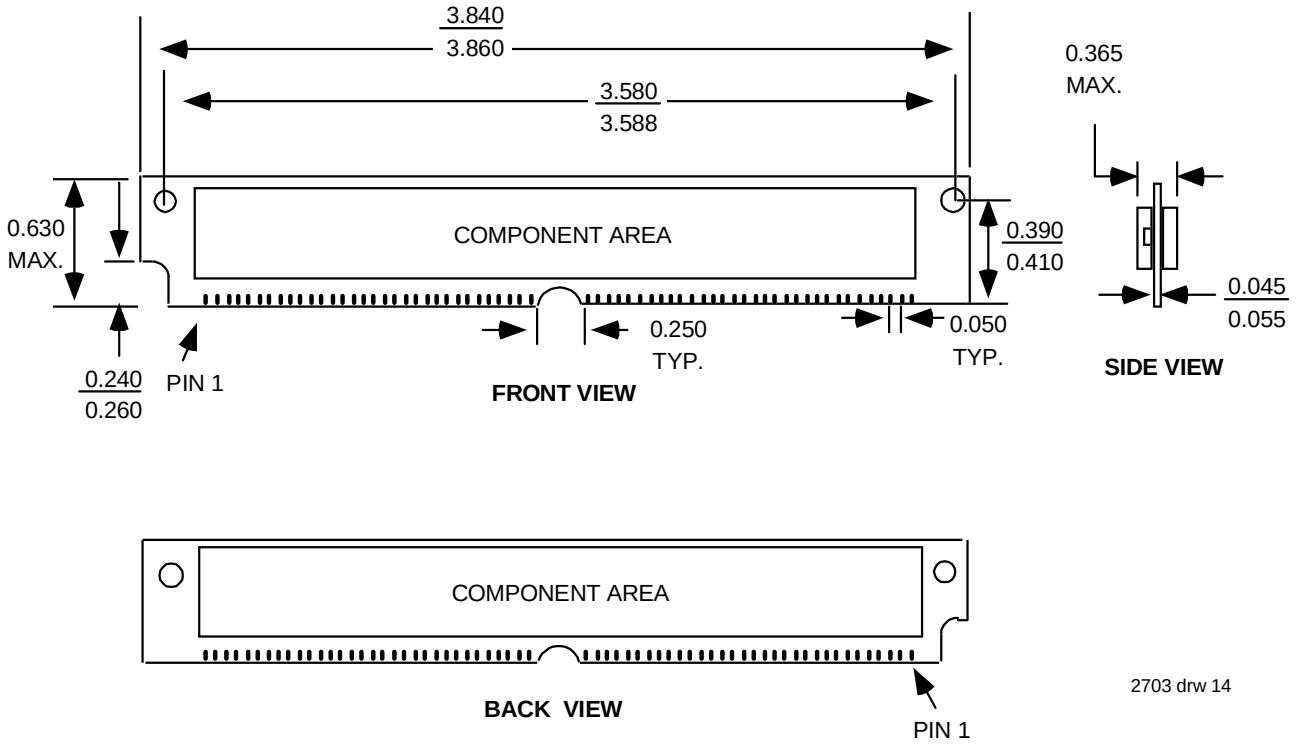
7MP4045 SIMM VERSION



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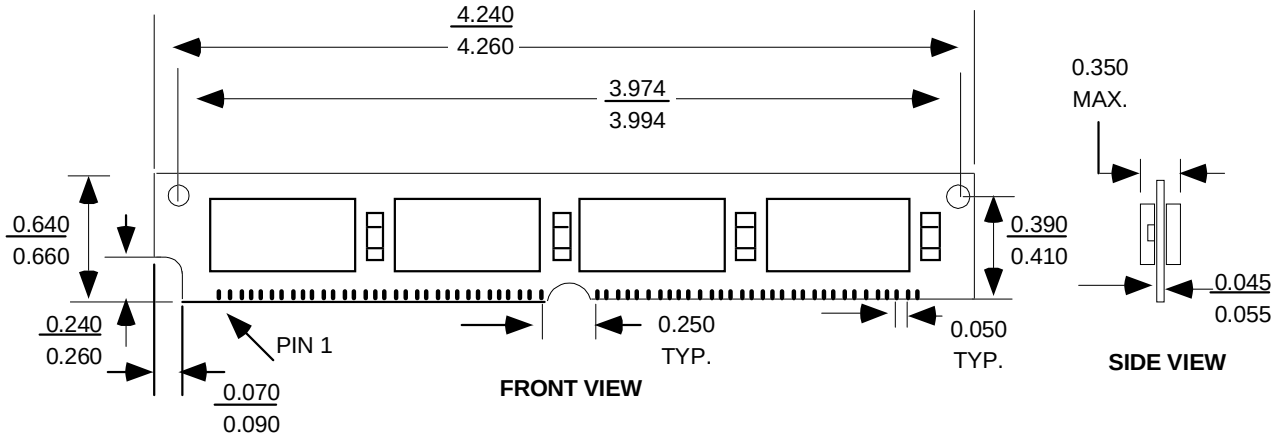
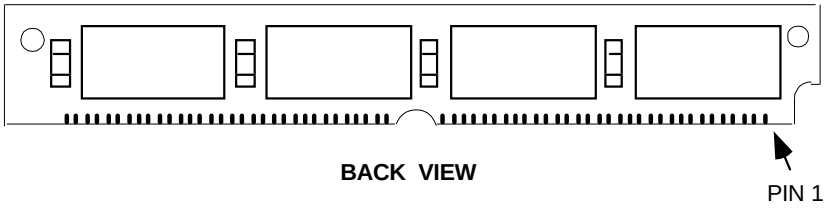
7MP4145 SIMM VERSION





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Ordering Information

IDT XXXXX X X X X

Device Type	Power	Speed	Package	Process/ Temperature Range	
				Blank	Commercial (0°C to +70°C)
			Z		FR-4 ZIP (Zig-Zag In-line vertical Package, 4045 only)
			M		FR-4 SIMM (Single In-line Memory Module)
		15 20 25			Speed in Nanoseconds
	S				Standard Power
7MP4045 7MP4145					256K x 32 Static RAM Module 256K x 32 Static RAM Module

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