



64K x 32 CMOS Static RAM Module

IDT7MP4036

Features

- ◆ High-density 2MB Static RAM module
- ◆ Low profile 64-pin ZIP (Zig-zag In-line vertical Package) or 64-pin SIMM (Single In-line Memory Module)
- ◆ Ultra fast access time: 12ns (max.)
- ◆ Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- ◆ Single 5V ($\pm 10\%$) power supply
- ◆ Multiple GND pins and decoupling capacitors for maximum noise immunity
- ◆ Inputs/outputs directly TTL-compatible

Pin Configuration⁽¹⁾

		1	GND	
PD0	2	3	PD1	PD0 – OPEN
I/O0	4	5	I/O8	PD1 – GND
I/O1	6	7	I/O9	
I/O2	8	9	I/O10	
I/O3	10	11	I/O11	
VCC	12	13	A0	
A7	14	15	A1	
A8	16	17	A2	
A9	18	19	I/O12	
I/O4	20	21	I/O13	
I/O5	22	23	I/O14	
I/O6	24	25	I/O15	
I/O7	26	27	GND	
WE	28	29	A15	
A14	30	31	CS2	
CS1	32			
		33	CS4	
CS3	34	35	NC	
NC	36	37	OE	
GND	38	39	I/O24	
I/O16	40	41	I/O25	
I/O17	42	43	I/O26	
I/O18	44	45	I/O27	
I/O19	46	47	A3	
A10	48	49	A4	
A11	50	51	A5	
A12	52	53	VCC	
A13	54	55	A6	
I/O20	56	57	I/O28	
I/O21	58	59	I/O29	
I/O22	60	61	I/O30	
I/O23	62	63	I/O31	
GND	64			

2682 drw 02

ZIP, SIMM Top View

NOTE:

1. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the density of the module. If PD0 reads Open and PD1 reads GND, then the module had a 64K depth.

Description

The IDT7MP4036 is a 64K x 32 Static RAM module constructed on an epoxy laminate (FR-4) substrate using eight 64K x 4 Static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 256K Static RAMs fabricated in IDT's high-performance, high-reliability CMOS technology. The IDT7MP4036 is available with access time as fast as 12ns with minimal power consumption.

The IDT7MP4036 is packaged in a 64-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low-profile package is ideal for systems with minimum board spacing, while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4036 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 64K depth.

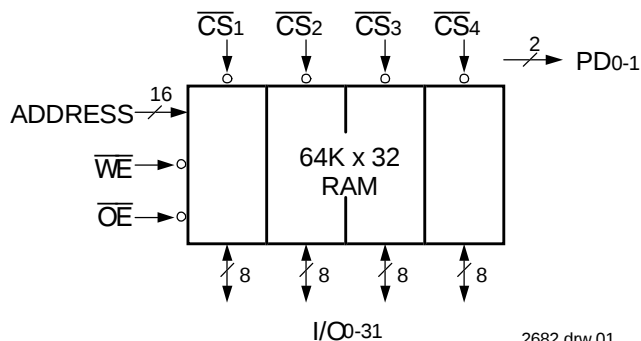
Pin Names

I/O0-31	Data Inputs/Outputs
A0-15	Addresses
CS1-4	Chip Selects
WE	Write Enable
OE	Output Enable
PD0-1	Depth Identification
Vcc	Power
GND	Ground
NC	No Connect

2682 tbl 01

DECEMBER 1999

Functional Block Diagram



Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2682 tbl 05

Capacitance ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	$V_{IN} = 0V$	15	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{IN} = 0V$	70	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	15	pF

2682 tbl 02

NOTE:

1. This parameter is guaranteed by design but not tested.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	$^\circ\text{C}$
T_{BIAS}	Temperature Under Bias	-10 to +85	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55 to +125	$^\circ\text{C}$
I_{OUT}	DC Output Current	50	mA

2682 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. I/O pins must not exceed $V_{CC} + 0.5V$.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
$V_{IH}^{(2)}$	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

2682 tbl 03

NOTES:

1. $V_{IL}(\text{min}) = -1.5V$ for pulse width less than 10ns.
2. I/O pins must not exceed $V_{CC} + 0.5V$.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	VCC
Commercial	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$	0V	5V $\pm$ 10%

2682 tbl 04

DC Electrical Characteristics

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I _{LI}	Input Leakage Current (Address and Control)	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	80	μA
I _{LI}	Input Leakage Current (Data)	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	10	μA
I _{LOI}	Output Leakage Current	V _{CC} = Max., $\overline{CS}$ = V _{IH} , V _{OUT} = GND to V _{CC}	—	10	μA
V _{OL}	Output Low Voltage	I _{OL} = 8mA, V _{CC} = Min.	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{CC} = Min.	2.4	—	V
I _{CC}	Dynamic Operating Current	V _{CC} = Max., $\overline{CS}$ = V _{IL} , f = f _{MAX} , Outputs Open	—	1280	mA
I _{SB}	Standby Supply Current	V _{CC} = Max., $\overline{CS}$ ≥ V _{IH} , f = f _{MAX} , Outputs Open	—	360	mA
I _{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V _{CC} - 0.2V, f = 0 V _{IN} > V _{CC} - 0.2V or < 0.2V	—	240	mA

2682 tbl 07

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2682 tbl 08

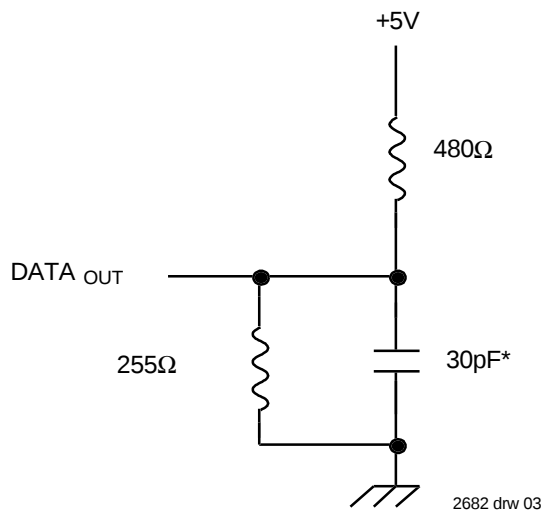


Figure 1. Output Load

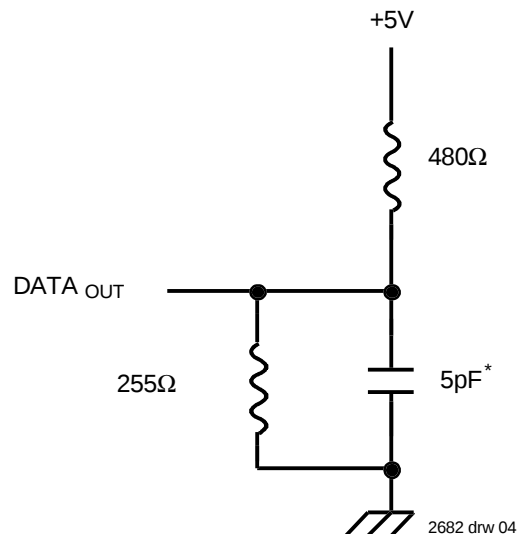


Figure 2. Output Load
(for t_{OLZ}, t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

*includes scope and jig.

AC Electrical Characteristics

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4036SxxZ, 7MP4036SxxM						Unit
		-12 ⁽²⁾		-13		-15		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	12	—	13	—	15	—	ns
t _{AA}	Address Access Time	—	12	—	13	—	15	ns
t _{ACS}	Chip Select Access Time	—	12	—	13	—	15	ns
t _{CLZ} ⁽¹⁾	Chip Select to Output in Low-Z	2	—	2	—	2	—	ns
t _{OE}	Output Enable to Output Valid	—	7	—	8	—	9	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t _{CHZ} ⁽¹⁾	Chip Deselect to Output in High-Z	—	7	—	7	—	8	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High-Z	—	7	—	7	—	8	ns
t _{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t _{PU} ⁽¹⁾	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t _{PD} ⁽¹⁾	Chip Deselect to Power-Down Time	—	12	—	13	—	15	ns
Write Cycle								
t _{WC}	Write Cycle Time	12	—	13	—	15	—	ns
t _{CW}	Chip Select to End-of-Write	10	—	11	—	12	—	ns
t _{AW}	Address Valid to End-of-Write	11	—	12	—	13	—	ns
t _{AS}	Address Set-up Time	1	—	1	—	1	—	ns
t _{WP}	Write Pulse Width	10	—	11	—	12	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{WHZ} ⁽¹⁾	Write Enable to Output in High-Z	—	7	—	7	—	8	ns
t _{DW}	Data to Write Time Overlap	7	—	7	—	8	—	ns
t _{DH}	Data Hold Time	1	—	1	—	1	—	ns
t _{OW} ⁽¹⁾	Output Active from End-of-Write	2	—	2	—	1	—	ns

2682 tbl 09

NOTES:

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

AC Electrical Characteristics

(V_{cc} = 5V ±10%, T_A = 0°C to +70°C)

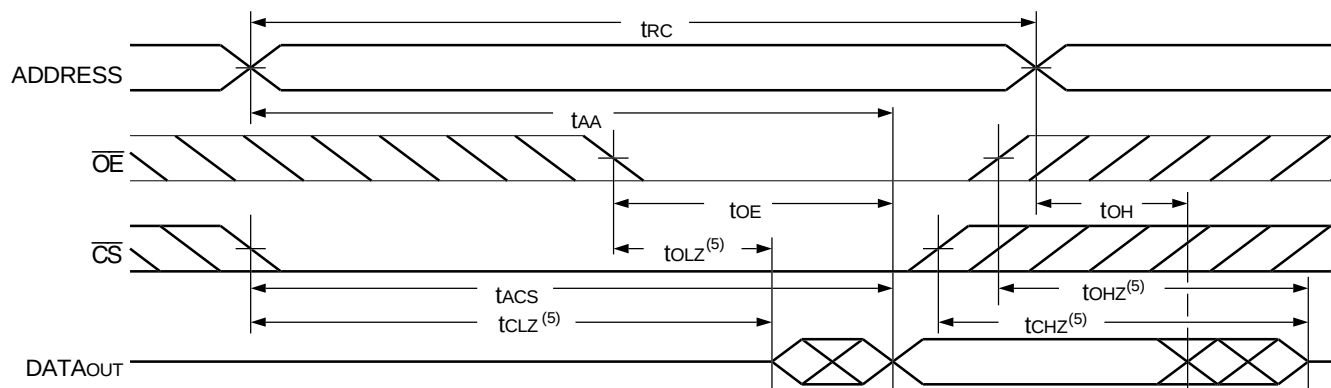
Symbol	Parameter	7MP4036SxxZ, 7MP4036SxxM						Unit
		-20		-25		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	35	ns
t _{ACS}	Chip Select Access Time	—	20	—	25	—	35	ns
t _{OLZ} ⁽¹⁾	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t _{OE}	Output Enable to Output Valid	—	10	—	12	—	25	ns
t _{OLZ} ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t _{CHZ} ⁽¹⁾	Chip Deselect to Output in High-Z	—	10	—	15	—	22	ns
t _{OHZ} ⁽¹⁾	Output Disable to Output in High-Z	—	10	—	15	—	22	ns
t _{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t _{PU} ⁽¹⁾	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t _{PD} ⁽¹⁾	Chip Deselect to Power-Down Time	—	20	—	25	—	35	ns
Write Cycle								
t _{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t _{CW}	Chip Select to End-of-Write	15	—	20	—	30	—	ns
t _{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	15	—	20	—	30	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{WHZ} ⁽¹⁾	Write Enable to Output in High-Z	—	12	—	15	—	18	ns
t _{DW}	Data to Write Time Overlap	12	—	15	—	20	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	ns
t _{OW} ⁽¹⁾	Output Active from End-of-Write	0	—	0	—	0	—	ns

2682 tbl 10

NOTES:

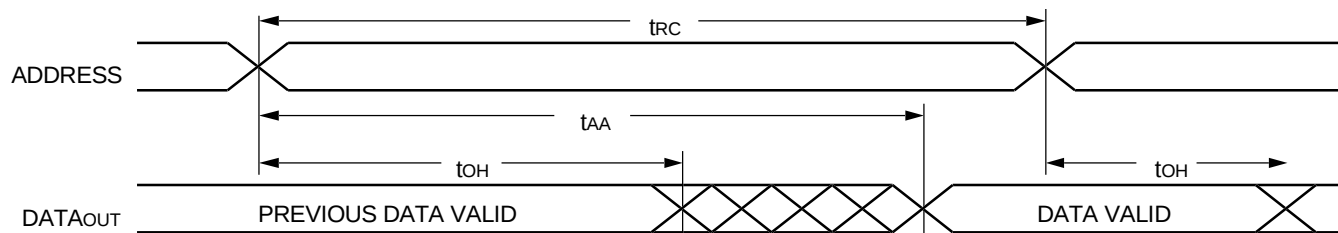
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

Timing Waveform of Read Cycle No. 1⁽¹⁾



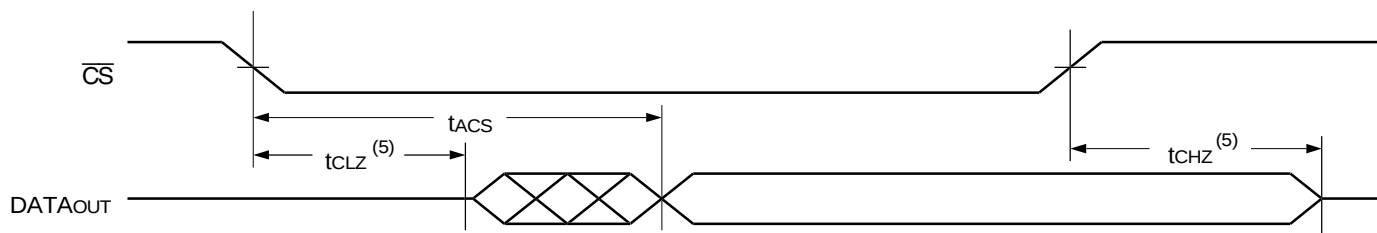
2682 drw 07

Timing Waveform of Read Cycle No. 2^(1,2,4)



2682 drw 08

Timing Waveform of Read Cycle No. 3^(1,3,4)

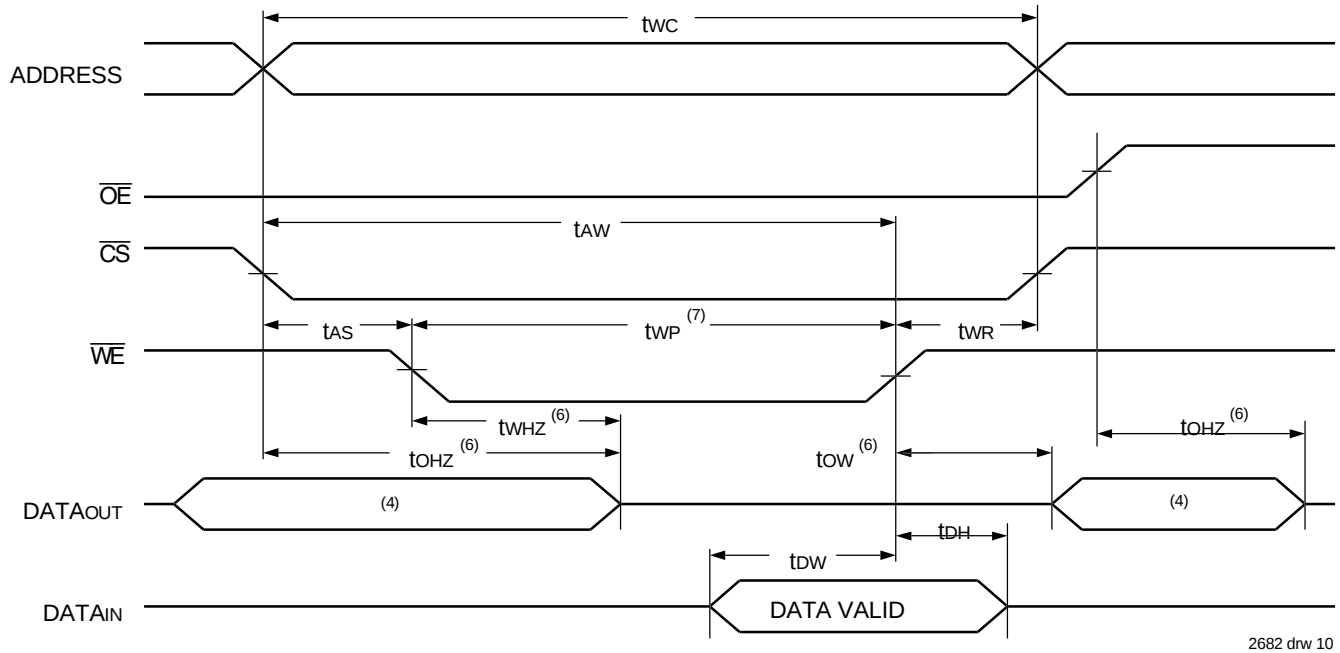


2682 drw 09

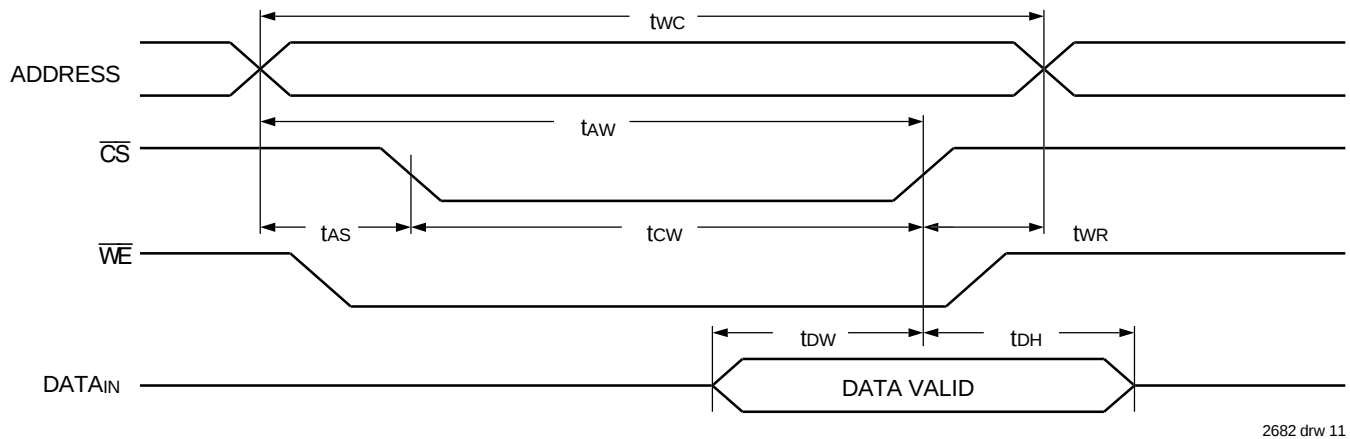
NOTES:

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200\text{mV}$ from steady state. This parameter is guaranteed by design, but not tested.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)^(1,2,3,7)



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)^(1,2,3,5)

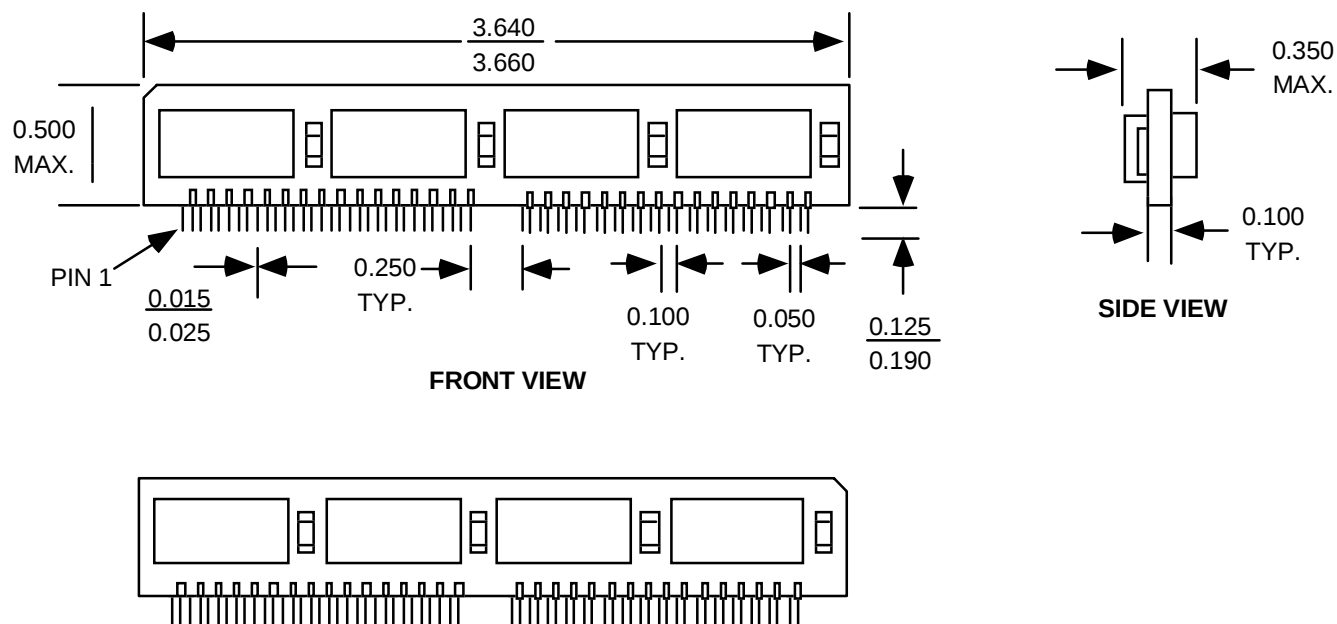


NOTES:

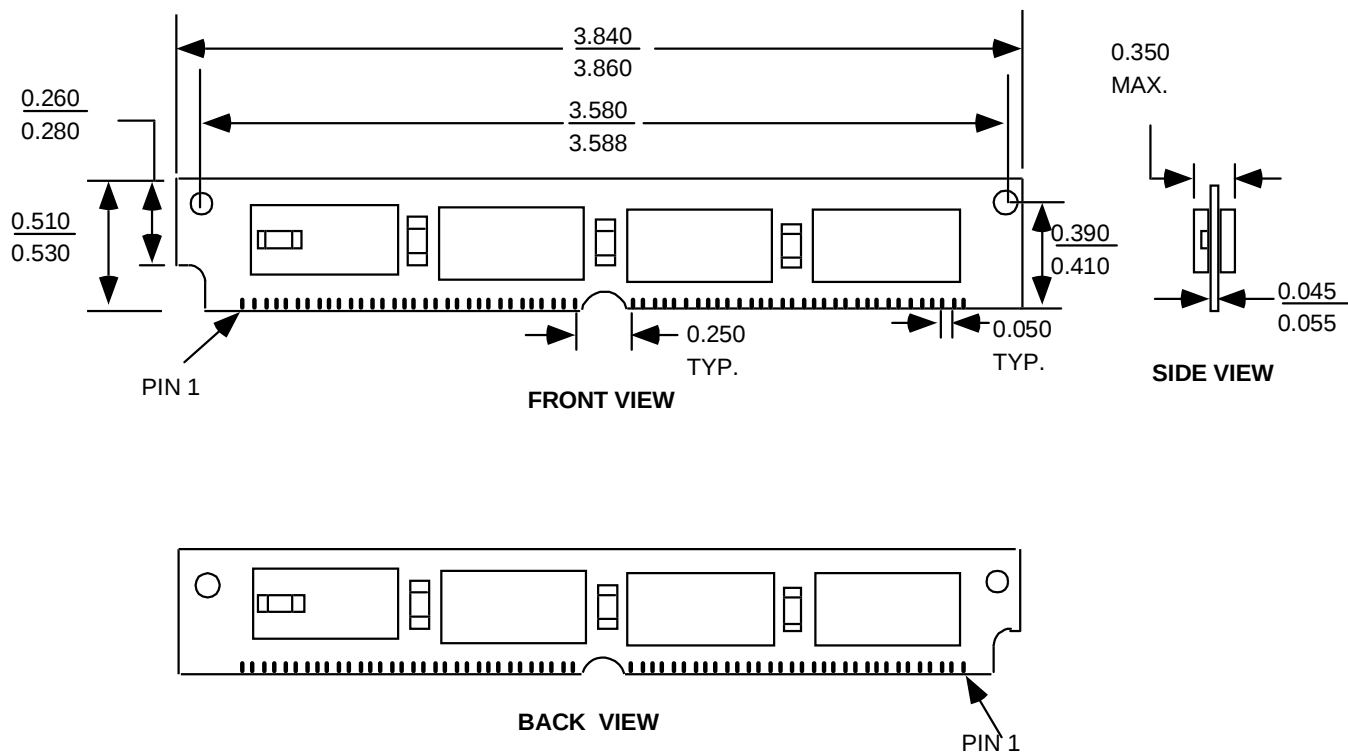
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{OW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

Package Dimensions

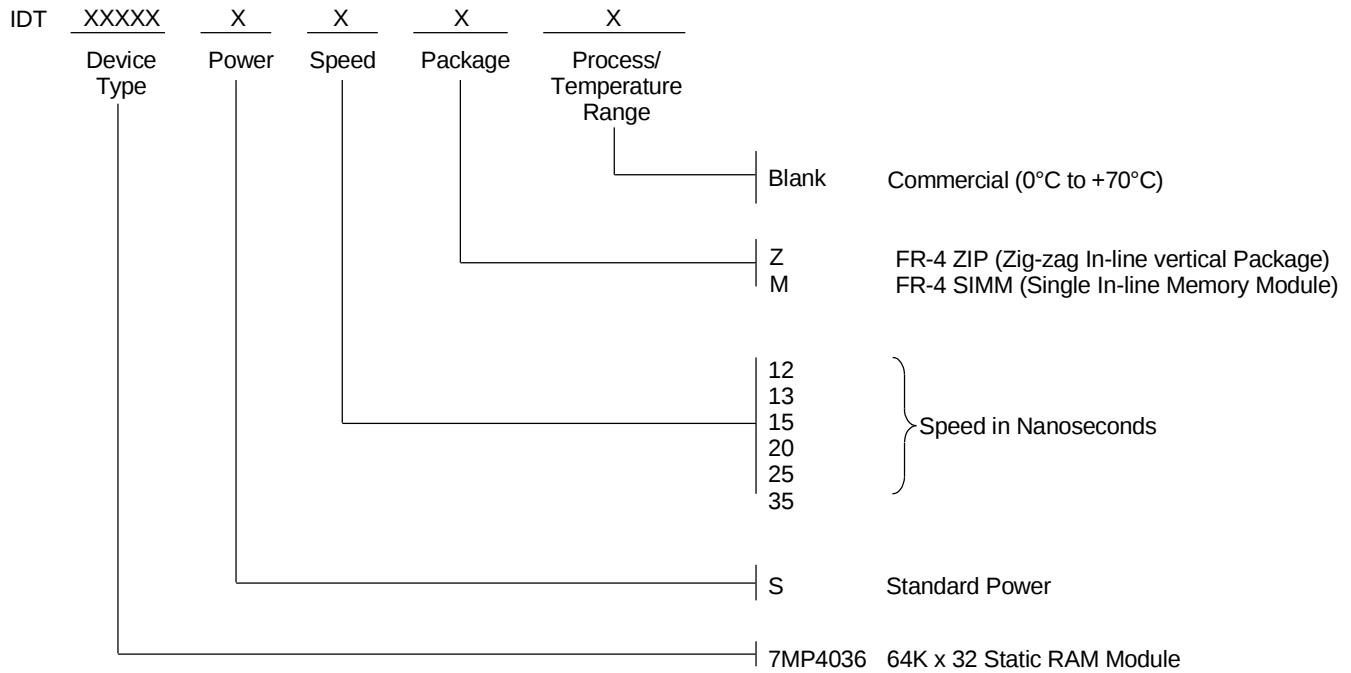
ZIP VERSION



SIMM VERSION



Ordering Information



2682 drw 14



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
sramhelp@idt.com
800 544-7726, x4033

The IDT logo is a registered trademark of Integrated Device Technology, Inc.