Integrated Device Technology, Inc.

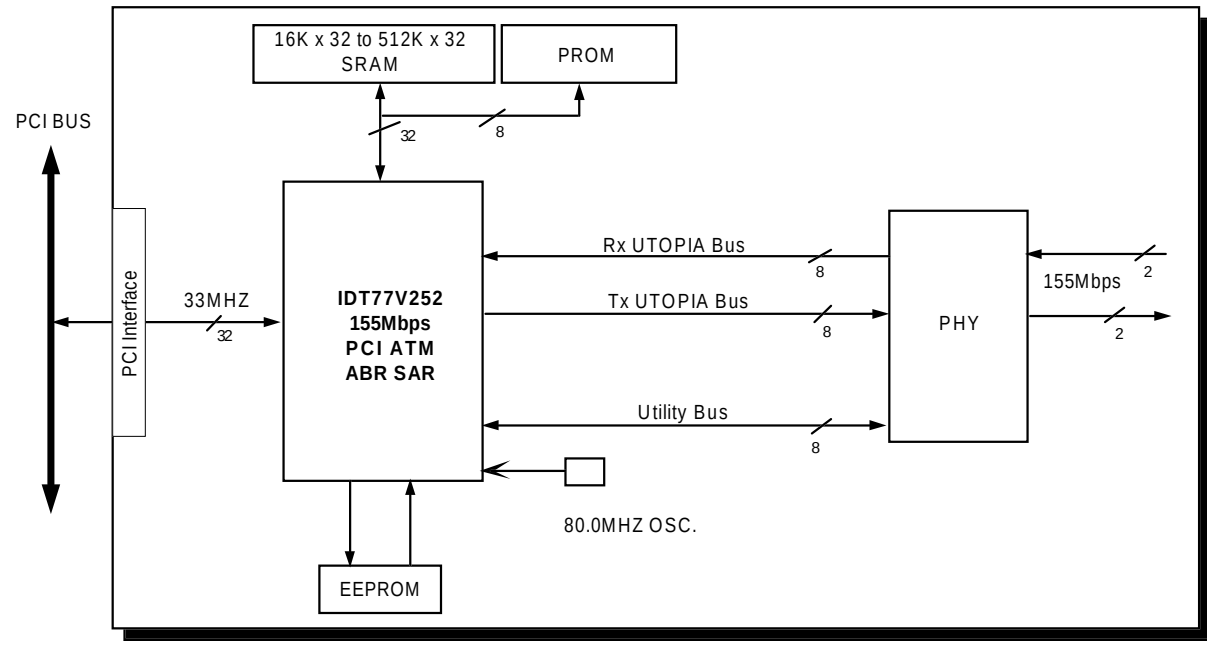
3.3V 155 Mbps ATM SAR CONTROLLER WITH ABR SUPPORT FOR PCI-BASED NETWORKING APPLICATIONS

IDT77V252

KEY FEATURES

- Full-duplex Segmentation and Reassembly (SAR) at 155 Mbps "wire-speed" (310 Mbps aggregate speed)
- Operates with ATM Networks up to 155.52 Mbps
- Stand-alone Controller: Embedded Processor not required
- Performs ATM Layer Protocol Functions
- Supports AAL5, AAL3/4, AAL0 and Raw Cell Formats
- Supports Constant Bit Rate (CBR), Variable Bit Rate (VBR), and Unassigned Bit Rate (UBR), and Available Bit Rate (ABR) Service Classes
- Segments and Reassembles CS-PDUs into Host Memory
- Up to 16K Open Transmit Connections
- Up to 16K Simultaneous Receive Connections
- ABR, VBR, UBR Selectable per VC Time-out
- Automatic AAL5 Padding
- Four Buffer Pools for Independent or Chained Reassembly
- Buffer Management Options for MPEG Operation
- Supports Any Buffer Alignment Condition
- Free Bufffer Queues Mapped Into PCI Memory Space
- Rx FIFO Size (Configurable to 1024 Kbytes)
- Configurable Transmit FIFO Depth for Reduced Latency
- Supports Big and Little Endian Data Transfers
- UTOPIA Master/Slave Mode
- Null Cell Disable Option During Transmit
- RM Cell Handling
- Option to Select ITU or ATM Null Cell Format
- NAND, Scan, and Output Test Modes
- UTOPIA Level 1 Interface to PHY
- Utility Bus Interface for PHY Management
- Serial EEPROM Interface
- EPROM Interface
- PCI 2.1 Compliant
- Compact PCI R1.0 Hot Swap Friendly Compliant
- UNI 3.1, TM 4.0 Compliant
- Meets PCI Bus Power Management and Interface Specification Revision 1.1
- Pin Compatible with IDT 77211/77252 SAR
- Software Compatible with the IDT 77252
- Commercial and Industrial Temprature Ranges
- 208-Lead PQFP Package (28 x 28mm)
- Software Drivers:
  - SARWIN 2 Demonstration Program
  - NDIS Driver
  - Vx Works (3rd party)
  - Linux (3rd party)

SYSTEM-LEVEL FUNCTIONAL BLOCK DIAGRAM



5350 drw 01

NICStAR is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

©2001 Integrated Device Technology, Inc.

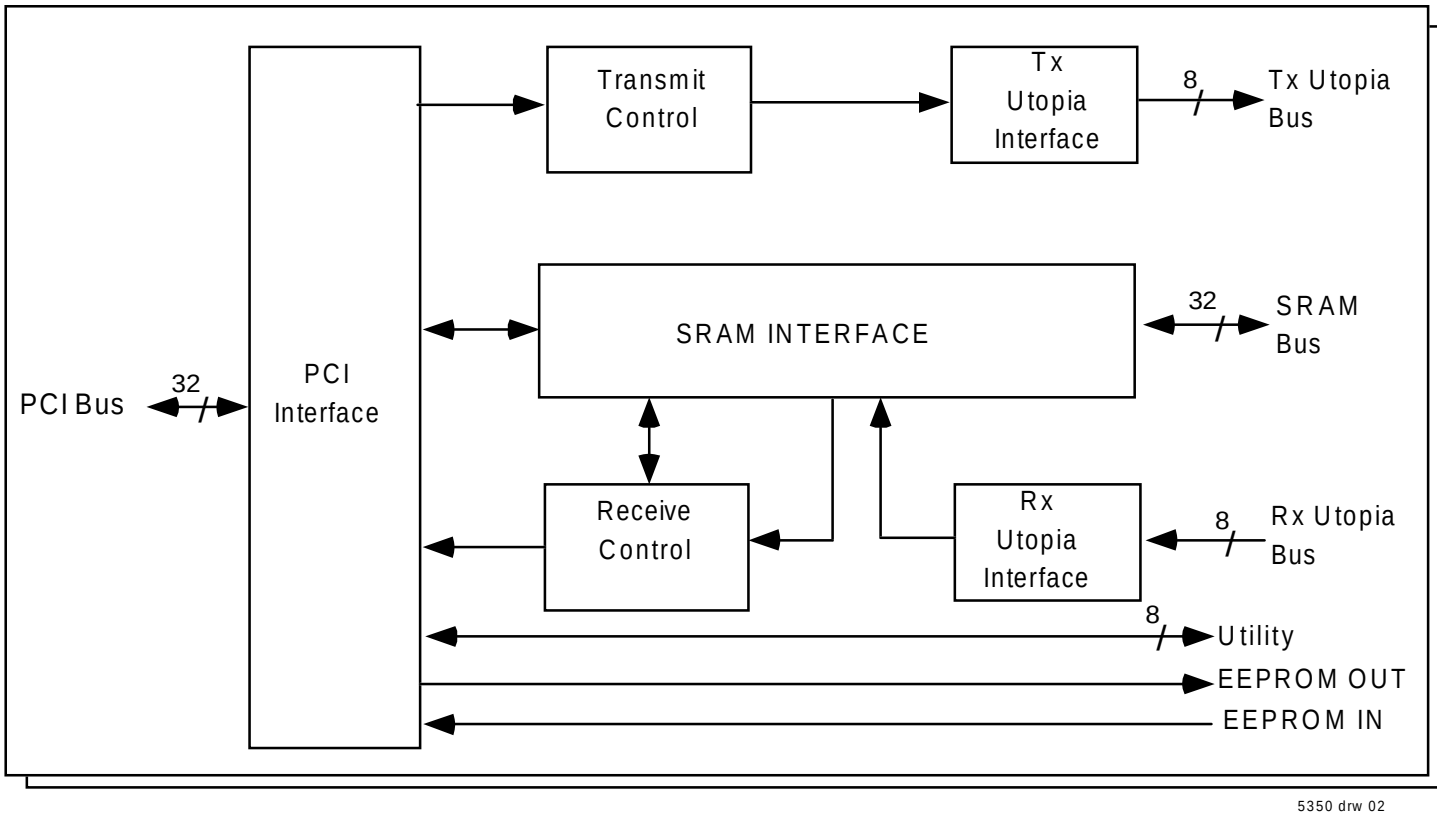
DSC-5350/8

DESCRIPTION

The IDT77V252 NICStAR™ is a member of IDT's family of products for Asynchronous Transfer Mode (ATM) networks. The ABR SAR performs both the ATM Adaptation Layer (AAL) Segmentation and Reassembly (SAR) function and the ATM layer protocol functions.

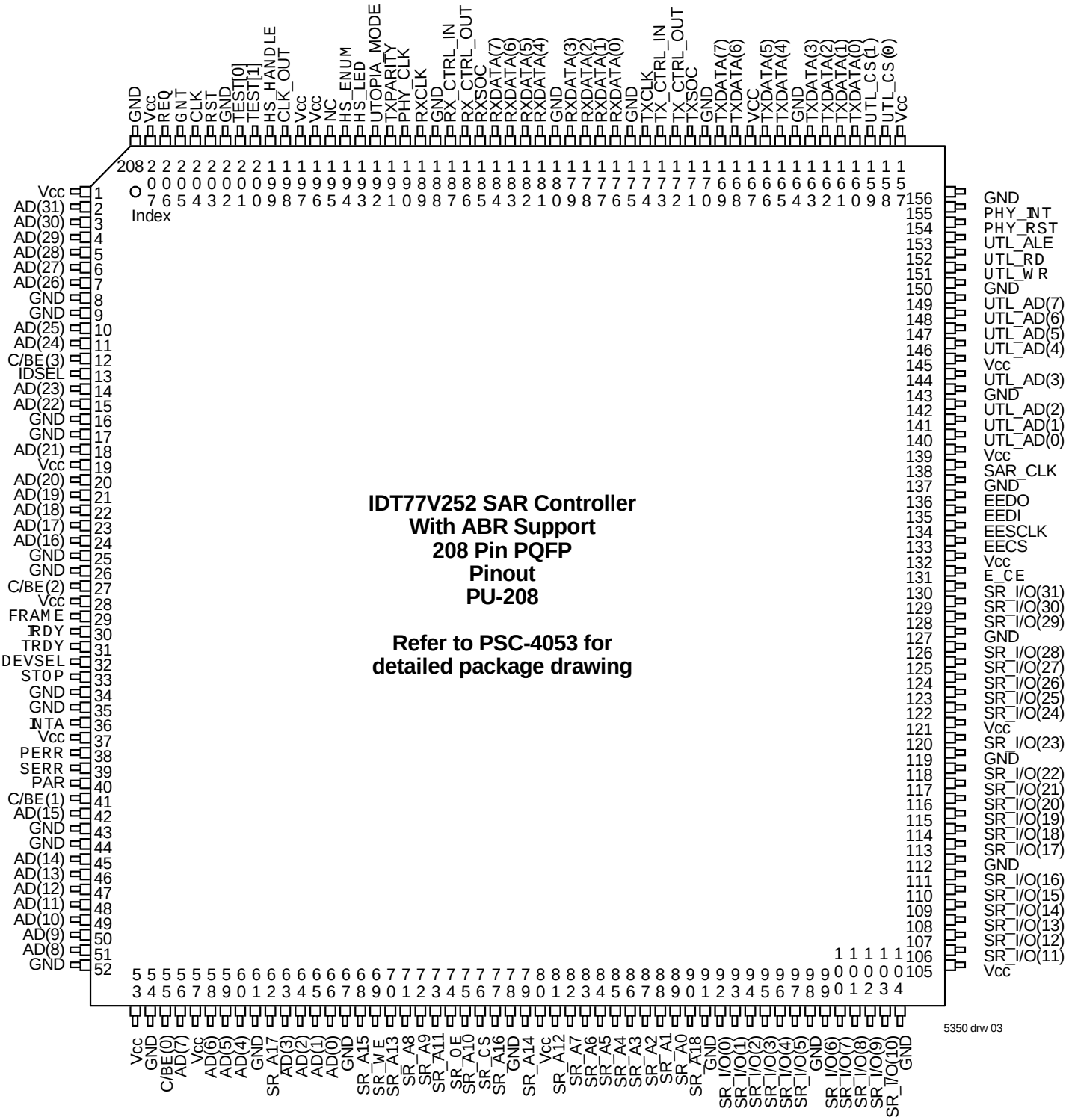
A Network Interface Card (NIC) or internetworking product based on the ABR SAR uses host memory, rather than local memory, to reassemble Convergence Sublayer Protocol Data Units (CS-PDUs) from ATM cell payloads received from the network. When transmitting, as CS-PDUs become ready, they are queued in host memory and segmented by the ABR SAR into ATM cell payloads. From this, the ABR SAR then creates complete 53-byte ATM cells which are sent through the network. The ABR SAR's on-chip PCI bus master interface provides efficient, low latency DMA transfers with the host system, while its UTOPIA interface provides direct connection to PHY components used in 25.6 Mbps to 155 Mbps ATM networks.

The IDT77V252 is fabricated using state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

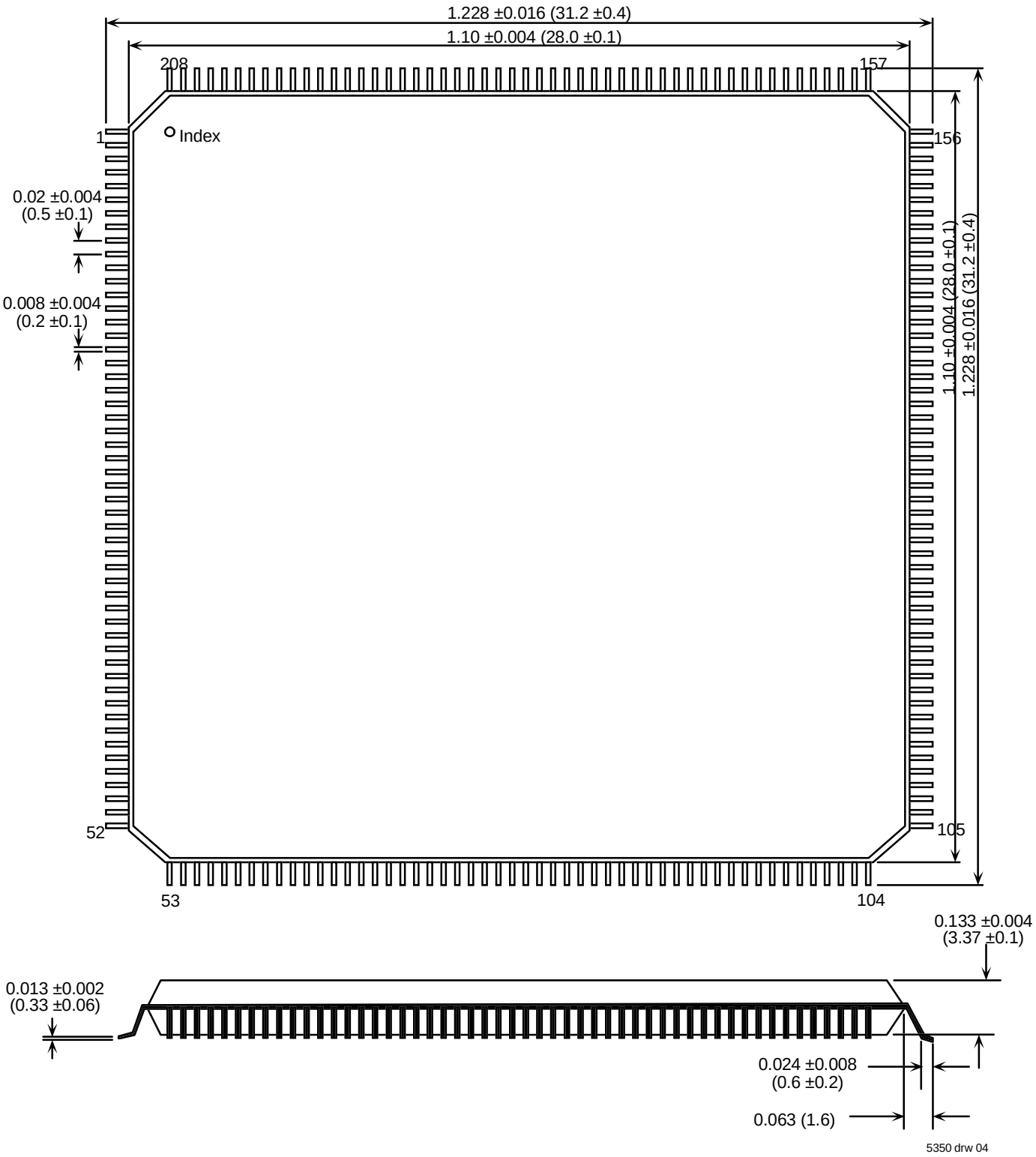


Block Diagram of the 77V252 ABR SAR

PACKAGE PINOUT



PACKAGE DRAWING



PIN DEFINITIONS

Pin #	Name	I/O	Bus Name	Description
1	Vcc	I	power	
2	AD(31)	I/O	PCI	address/data line
3	AD(30)	I/O	PCI	address/data line
4	AD(29)	I/O	PCI	address/data line
5	AD(28)	I/O	PCI	address/data line
6	AD(27)	I/O	PCI	address/data line
7	AD(26)	I/O	PCI	address/data line
8	GND	I	power	
9	GND	I	power	
10	AD(25)	I/O	PCI	address/data line
11	AD(24)	I/O	PCI	address/data line
12	C/$\overline{BE}$(3)	I/O	PCI	bus command
13	IDSEL	I	PCI	bus ID select
14	AD(23)	I/O	PCI	address/data line
15	AD(22)	I/O	PCI	address/data line
16	GND	I	power	
17	GND	I	power	
18	AD(21)	I/O	PCI	address/data line
19	Vcc	I	power	
20	AD(20)	I/O	PCI	address/data line
21	AD(19)	I/O	PCI	address/data line
22	AD(18)	I/O	PCI	address/data line
23	AD(17)	I/O	PCI	address/data line
24	AD(16)	I/O	PCI	address/data line
25	GND	I	power	
26	GND	I	power	
27	C/$\overline{BE}$(2)	I/O	PCI	bus command
28	Vcc	I	power	
29	$\overline{Frame}$	I/O	PCI	cycle frame
30	$\overline{IRDY}$	I/O	PCI	initiator ready
31	$\overline{TRDY}$	I/O	PCI	target ready
32	$\overline{DEVSEL}$	I/O	PCI	target indicating address decode
33	$\overline{STOP}$	I/O	PCI	target requesting master to stop
34	GND	I	power	
35	GND	I	power	
36	$\overline{INTA}$	O	PCI	"interrupt" "A" "request"
37	Vcc	I	power	
38	$\overline{PERR}$	I/O	PCI	data parity error
39	$\overline{SERR}$	O	PCI	system error
40	PAR	I/O	PCI	parity (for AD[0:31] and C/BE[0:3])
41	C/$\overline{BE}$(1)	I/O	PCI	bus command
42	AD(15)	I/O	PCI	address/data line
43	GND	I	power	
44	GND	I	power	
45	AD(14)	I/O	PCI	address/data line
46	AD(13)	I/O	PCI	address/data line
47	AD(12)	I/O	PCI	address/data line
48	AD(11)	I/O	PCI	address/data line

5350 tbl 01

PIN DEFINITIONS (CON'T.)

Pin #	Name	I/O	Bus Name	Description
49	AD(10)	I/O	PCI	address/data line
50	AD(9)	I/O	PCI	address/data line
51	AD(8)	I/O	PCI	address/data line
52	GND	I	power	
53	Vcc	I	power	
54	GND	I	power	
55	C/$\overline{BE}$(0)	I/O	PCI	bus command
56	AD(7)	I/O	PCI	address/data line
57	Vcc	I	power	
58	AD(6)	I/O	PCI	address/data line
59	AD(5)	I/O	PCI	address/data line
60	AD(4)	I/O	PCI	address/data line
61	GND	I	power	
62	SR_A17	O	SRAM	Address line
63	AD(3)	I/O	PCI	address/data line
64	AD(2)	I/O	PCI	address/data line
65	AD(1)	I/O	PCI	address/data line
66	AD(0)	I/O	PCI	address/data line
67	GND	I	power	
68	SR_A15	O	SRAM	Address line
69	$\overline{SR\_WE}$	O	SRAM	Write enable
70	SR_A13	O	SRAM	Address line
71	SR_A8	O	SRAM	Address line
72	SR_A9	O	SRAM	Address line
73	SR_A11	O	SRAM	Address line
74	$\overline{SR\_OE}$	O	SRAM	Output Enable control
75	SR_A10	O	SRAM	Address line
76	$\overline{SR\_CS}$	O	SRAM	Chip Select
77	SR_A16	O	SRAM	Address line
78	GND	I	power	
79	SR_A14	O	SRAM	Address line
80	Vcc	I	power	
81	SR_A12	O	SRAM	Address line
82	SR_A7	O	SRAM	Address line
83	SR_A6	O	SRAM	Address line
84	SR_A5	O	SRAM	Address line
85	SR_A4	O	SRAM	Address line
86	SR_A3	O	SRAM	Address line
87	SR_A2	O	SRAM	Address line
88	SR_A1	O	SRAM	Address line
89	SR_A0	O	SRAM	Address line
90	SR _A18	O	SRAM	Address line
91	GND	I	power	
92	SR_I/O(0)	I/O	SRAM	Data input/output line
93	SR_I/O(1)	I/O	SRAM	Data input/output line
94	SR_I/O(2)	I/O	SRAM	Data input/output line
95	SR_I/O(3)	I/O	SRAM	Data input/output line
96	SR_I/O(4)	I/O	SRAM	Data input/output line

5350 tbl 02

PIN DEFINITIONS (CON'T.)

Pin #	Name	I/O	Bus Name	Description
97	SR_I/O(5)	I/O	SRAM	Data input/output line
98	GND	I	power	
99	SR_I/O(6)	I/O	SRAM	Data input/output line
100	SR_I/O(7)	I/O	SRAM	Data input/output line
101	SR_I/O(8)	I/O	SRAM	Data input/output line
102	SR_I/O(9)	I/O	SRAM	Data input/output line
103	SR_I/O(10)	I/O	SRAM	Data input/output line
104	GND	I	power	
105	Vcc	I	power	
106	SR_I/O(11)	I/O	SRAM	Data input/output line
107	SR_I/O(12)	I/O	SRAM	Data input/output line
108	SR_I/O(13)	I/O	SRAM	Data input/output line
109	SR_I/O(14)	I/O	SRAM	Data input/output line
110	SR_I/O(15)	I/O	SRAM	Data input/output line
111	SR_I/O(16)	I/O	SRAM	Data input/output line
112	GND	I	power	
113	SR_I/O(17)	I/O	SRAM	Data input/output line
114	SR_I/O(18)	I/O	SRAM	Data input/output line
115	SR_I/O(19)	I/O	SRAM	Data input/output line
116	SR_I/O(20)	I/O	SRAM	Data input/output line
117	SR_I/O(21)	I/O	SRAM	Data input/output line
118	SR_I/O(22)	I/O	SRAM	Data input/output line
119	GND	I	power	
120	SR_I/O(23)	I/O	SRAM	Data input/output line
121	Vcc	I	power	
122	SR_I/O(24)	I/O	SRAM	Data input/output line
123	SR_I/O(25)	I/O	SRAM	Data input/output line
124	SR_I/O(26)	I/O	SRAM	Data input/output line
125	SR_I/O(27)	I/O	SRAM	Data input/output line
126	SR_I/O(28)	I/O	SRAM	Data input/output line
127	GND	I	power	
128	SR_I/O(29)	I/O	SRAM	Data input/output line
129	SR_I/O(30)	I/O	SRAM	Data input/output line
130	SR_1/O(31)	I/O	SRAM	Data input/output line
131	$\overline{E\_CE}$	O	EPROM	EPROM chip select
132	Vcc	I	power	
133	EECS	O	EEPROM	chip select
134	EESCLK	O	EEPROM	clock
135	EEDI	I	EEPROM	Data input
136	EEDO	O	EEPROM	Data output
137	GND	I	power	
138	SAR_CLK	I		SAR clock input
139	Vcc	I	power	
140	UTL_AD(0)	I/O	Utility	address/data bus
141	UTL_AD(1)	I/O	Utility	address/data bus
142	UTL_AD(2)	I/O	Utility	address/data bus
143	GND	I	power	
144	UTL_AD(3)	I/O	Utility	address/data bus

5350 tbl 03

PIN DEFINITIONS (CON'T.)

Pin #	Name	I/O	Bus Name	Description
145	Vcc	I	power	
146	UTL_AD(4)	I/O	Utility	address/data bus
147	UTL_AD(5)	I/O	Utility	address/data bus
148	UTL_AD(6)	I/O	Utility	address/data bus
149	UTL_AD(7)	I/O	Utility	address/data bus
150	GND	I	power	
151	$\overline{\text{UTL\_WR}}$	O	Utility	write control
152	$\overline{\text{UTL\_RD}}$	O	Utility	read control
153	UTL_ALE	O	Utility	address latch enable
154	$\overline{\text{PHY\_RST}}$	O	PHY	rest control
155	$\overline{\text{PHY\_INT}}$	I	PHY	interrupt input from PHY
156	GND	I	power	
157	Vcc	I	power	
158	$\overline{\text{UTL\_CS(0)}}$	O	Utility	chip select (0)
159	$\overline{\text{UTL\_CS(1)}}$	O	Utility	chip select (1)
160	TxData(0)	O	UTOPIA	transmit data bit 0
161	TxData(1)	O	UTOPIA	transmit data bit 1
162	TxData(2)	O	UTOPIA	transmit data bit 2
163	TxData(3)	O	UTOPIA	transmit data bit 3
164	GND	I	power	
165	TxData(4)	O	UTOPIA	transmit data bit 4
166	TxData(5)	O	UTOPIA	transmit data bit 5
167	Vcc	I	power	
168	TxData(6)	O	UTOPIA	transmit data bit 6
169	TxData(7)	O	UTOPIA	transmit data bit 7
170	GND	I	power	
171	TxSOC	O	UTOPIA	transmit start of cell
172	Tx_Ctrl_Out	O	UTOPIA	transmit control output (see Diagram 5)
173	Tx_Ctrl_In	I	UTOPIA	transmit control input (see Diagram 5)
174	TxCLK	I/O	UTOPIA	transmit data sync clock
175	GND	I	power	
176	RxData(0)	I	UTOPIA	receive data bit 0
177	RxData(1)	I	UTOPIA	receive data bit 1
178	RxData(2)	I	UTOPIA	receive data bit 2
179	RxData(3)	I	UTOPIA	receive data bit 3
180	GND	I	power	
181	RxData(4)	I	UTOPIA	receive data bit 4
182	RxData(5)	I	UTOPIA	receive data bit 5
183	RxData(6)	I	UTOPIA	receive data bit 6
184	RxData(7)	I	UTOPIA	receive data bit 7
185	RxSOC	I	UTOPIA	receive start of cell
186	Rx_Ctrl_Out	O	UTOPIA	receive control output (see Diagram 5)
187	Rx_Ctrl_In	I	UTOPIA	receive control input (see Diagram 5)
188	GND	I	power	
189	RxClk	I/O	UTOPIA	receive data sync clock
190	PHY_Clk	I	UTOPIA	transmit sync clock input
191	TxParity	O	UTOPIA	transmit data parity bit
192	UTOPIA_Mode	I	UTOPIA	UTOPIA Master/Slave mode select ("0" = Master ; "1" = Slave)

5350 tbl 04

PIN DEFINITIONS (CON'T.)

Pin #	Name	I/O	Bus Name	Description
193	$\overline{HS\_LED}$	O	PCI	hot swap friendly status LED
194	$\overline{HS\_Enum}$	O	PCI	hot swap friendly configuration signal
195	NC	---	---	no connection
196	V_{CC}	I	power	
197	V_{CC}	I	power	
198	CLKout	O		SAR_Clk divided by 3
199	$\overline{HS\_Handle}$	I	PCI	hot swap friendly handle switch
200	Test[1]	I	power	test mode control (see Table 1)
201	Test[0]	I	power	test mode control (see Table 1)
202	GND	I	power	
203	$\overline{RST}$	I	PCI	system bus reset
204	CLK	I	PCI	bus clock
205	$\overline{GNT}$	I	PCI	bus grant signal from arbiter
206	$\overline{REQ}$	O	PCI	bus request
207	V_{CC}	I	power	
208	GND	I	power	

5350 tbl 05

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	V_{SS} - 0.3	3.6	V
V_{IN}	Input Voltage	V_{SS} - 0.3	5.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3	V_{CC} + 0.3	V
V_{SS}	Ground Voltage	0	0	V
T_{stg}	Storage Temperature	-55	125	°C

5350 tbl 06

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
V_I	Input Voltage	0	V_{CC}	V
T_{A1}	Commerical operating temperature	0	+70	°C
T_{A2}	Industrial operating temperature	-40	+85	°C
titr	Input TTL rise time	—	2	ns
titf	Input TTL rall time	—	2	ns

5350 tbl 07

CLOCKING

Symbol	Parameter	Rate	Min.	Max.	Unit
SAR_CLK	SAR clock input freq.	155Mb/s	77	80	MHz
		25Mb/s	25	80	MHz
PHY_CLK	PHY clock input freq.	155Mb/s	19.44	40	MHz
		25Mb/s	3	40	MHz
PCI_CLK	PCI clock input freq.	33MHz	0	33.3	MHz

5350 tbl 08

CAPACITANCE

Symbol	Parameter	Condition	Min.	Max.	Typical	Unit
C_{IN}	Input Capacitance	except PCI Bus	—	—	4	pF
C_{OUT}	Output Capacitance	all outputs	—	8	6	pF
C_{bid}	Bi-Directional Capacitance	all bi-directional pins	—	—	10	pF
C_{inpci}	PCI Bus Input Capacitance	PCI Bus inputs	—	10	—	pF
C_{clkpci}	PCI Bus Clock Input Capacitance	—	5	12	—	pF
C_{idsel}	PCI Bus ID Select Input Capacitance	—	—	8	—	pF

5350 tbl 09

DC OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Max.	Typical	Unit
Vil	Low-level TTL input voltage	—	-0.7V	(0.3)Vcc	—	V
Vih	High-level TTL input voltage	—	(0.5)Vcc	Vcc + 0.2V	—	V
Vol	Low-level TTL output voltage	—	—	0.4	—	V
Voh	High-level TTL output voltage	—	Vcc - 0.4V	—	—	V
Iol	Low-level TTL output current: SR_A(18-0)	Vss + 0.4V	12	—	—	mA
Ioh	High-level TTL output current: SR_A(18-0)	Vcc - 0.4V	-4	—	—	mA
Iol	Low-level TTL output current: Rx_Ctrl_Out, RxClk, TxSOC, TxData (7-0), Tx_Ctrl_Out, TxParity, TxClk, $\overline{WE}$, $\overline{OE}$, $\overline{CS}$, SR_D31-0	Vss + 0.4V	6	—	—	mA
Ioh	High-level TTL output current: Rx_Ctrl_Out, RxClk, TxSoc, TxData7-0, Tx_Ctrl_Out, TxParity, TxClk, $\overline{SR\_WE}$, $\overline{SR}$, $\overline{OE}$, $\overline{SR\_CS}$, SR_I/O(31-0)	Vcc - 0.4V	-2	—	—	mA
Iol	Low-level TTL output current: UTL_AD(7-0), $\overline{UTL\_RD}$, $\overline{UTL\_WR}$, UTL_ALE, $\overline{UTL\_CS0/1}$, EESCLK, EECS, EEDO, $\overline{PHY\_RST}$	Vss + 0.4V	3	—	—	mA
Ioh	High-level TTL output current: UTL_AD(7-0_, $\overline{UTL\_RD}$, $\overline{UTL\_WR}$, UTL_ALE, $\overline{UTL\_CS0/1}$, EESCLK, EECS, EEDO, $\overline{PHY\_RST}$	Vcc - 0.4V	-1	—	—	mA
Iil	Input leakage current	Vss ≤ VIN ≤ Vdd	-1	1	—	uA
Ityp	Dynamic Supply Current	—	—	300	195	mA

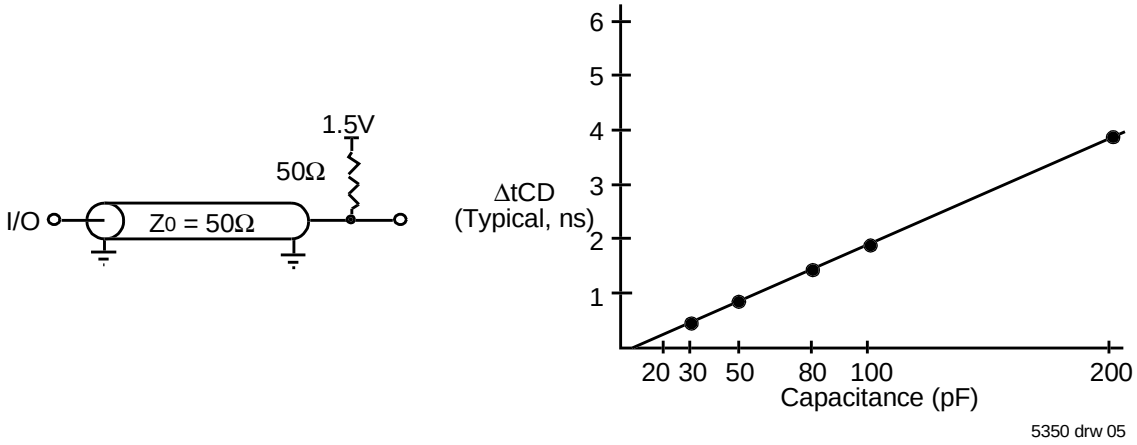
5350 tbl 10

AC OPERATING CONDITIONS

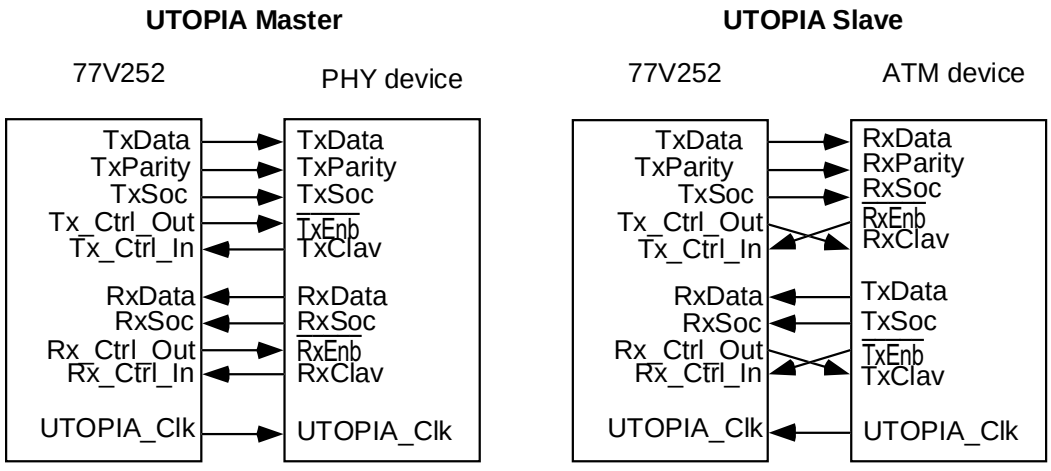
AC TEST CONDITIONS

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Ref. Level	1.5V
Output Ref. Level	1.5V
AC Test Load	See Figure Below

5350 tbl 11



5350 drw 05



Note:
1. Connect a pullup resistor to PHY_CIK (pin 190) when the 77V222 is configured for UTOPIA Slave mode.

5350 drw 06

Diagram 5. UTOPIA Modes

NAND CHAIN

The NAND Chain provides a simple test to verify that all bond wires are installed correctly and that all pads are correctly soldered on a PCB.

All signal pads are linked in a NAND chain, which is enabled by asserting a high, or “1”, on Test[0] (pin 201), and a low, or "0" on Test[1] (pin 200). Asserting a “1” on the other inputs forces EEDO (pin 136) to “1”. By successively setting the inputs to “0”, starting at $\overline{\text{HS\_Handle}}$ (pin 199) and moving to $\overline{\text{RST}}$ (pin 203), EEDO will toggle with each change.

1. Apply a "1" to Test[0] and a "0" to Test[1].
2. Set all the I/O's in the chain to "0" and EEDO should be a "1".The connection order of the pins in the chain are shown in the NAND Tree Pin Order table located on the following page.
3. Set $\overline{\text{HS\_Handle}}$ to a "0" and the EEDO should be a "0".
4. Leaving $\overline{\text{HS\_Handle}}$ at a "1" set $\overline{\text{HS\_Enum}}$ to "1" and EEDO should be a "1".
5. Repeat for all remaining I/O's in the NAND chain.

Test[0]	Test[1]	Mode
0	0	Normal operation.
0	1	NAND test. EEDO (pin 136) is the output of the NAND chain when using the NAND test mode.
1	0	Scan test. EEDI (pin 135) is scan data input, EEDO (pin 136) is scan data output, and EESCLK (pin 134) is scan clock.
1	1	Output test. All outputs equal EEDI (pin 135).

5350 tbl 12

Table 1. Test Modes

NAND Tree Order	Pin #	NAND Tree Order	Pin #	NAND Tree Order	Pin #	NAND Tree Order	Pin #	NAND Tree Order	Pin #
1	199	32	158	63	115	94	76	125	36
2	194	33	155	64	114	95	75	126	33
3	193	34	154	65	113	96	74	127	32
4	192	35	153	66	111	97	73	128	31
5	191	36	152	67	109	98	72	129	30
6	190	37	151	68	108	99	71	130	29
7	189	38	149	69	107	100	70	131	27
8	187	39	148	70	106	101	69	132	24
9	186	40	147	71	103	102	68	133	23
10	185	41	146	72	102	103	66	134	22
11	184	42	144	73	101	104	65	135	21
12	183	43	142	74	100	105	64	136	20
13	182	44	141	75	99	106	63	137	18
14	181	45	140	76	97	107	62	138	15
15	179	46	138	77	96	108	60	139	14
16	178	47	135	78	95	109	59	140	13
17	177	48	134	79	94	110	58	141	12
18	176	49	133	80	93	111	56	142	11
19	174	50	131	81	92	112	55	143	10
20	173	51	130	82	90	113	51	144	7
21	172	52	129	83	89	114	50	145	6
22	171	53	128	84	88	115	49	146	5
23	169	54	126	85	87	116	48	147	4
24	168	55	125	86	86	117	47	148	3
25	166	56	124	87	85	118	46	149	2
26	165	57	123	88	84	119	45	150	206
27	163	58	122	89	83	120	42	151	205
28	162	59	120	90	82	121	41	152	204
29	161	60	118	91	81	122	40	153	203
30	160	61	117	92	79	123	39		
31	159	62	116	93	77	124	38		

5350 tbl 13

Table 2. NAND Tree Pin Order

PCI BUS (SEE FIGURE 1& 2)

Symbol	Parameter	Min.	Max.	Unit
tval	CLK to Output Signal Valid Delay: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$	2	11	ns
tval(ptp)	CLK to Output Signal Valid Delay: REQ	2	12	ns
ton	Float to Signal Active Delay: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$	2	----	ns
toff	Signal Active to Float Delay: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$	----	28	ns
tsu	Input Setup Time to CLK: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$, $\overline{GNT}$	7	----	ns
tsu(ptp)	Input Setup Time to CLK: $\overline{GNT}$, ($\overline{REQ}$)	10(12)	----	ns
th	Input Hold Time from CLK: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$, $\overline{GNT}$	0	----	ns
trst-pwr	Reset Active Time After Power Stable	1	----	ns
trst-clk	Reset Active Time After CLK Stable	100	----	ns
trst-off	Reset Active to Output Float Delay: AD31-0, C/$\overline{BE}$3-0, PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{DEVSEL}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$	----	40	ns
thigh	Clock high time	11	----	ns
tlow	Clock low time	11	----	ns

5350 tbl 14

UTOPIA BUS (SEE FIGURE 3)

Symbol	Parameter	Min.	Max.	Unit
t1	TxClk, RxClk Delay from PHY_CLK	—	5	ns
t2	TxData(7-0), TxSOC, Tx_Ctrl_Out, TxParity Output Valid from TxClk	1	15	ns
t3	Tx_Ctrl_In Setup Time to TxClk	10	—	ns
t4	Tx_Ctrl_In Hold Time from TxClk	1	—	ns
t5	Rx_Ctrl_Out Output Valid from RxClk	1	15	ns
t6	RxData(7-0), RxSOC Setup Time to RxClk	10	—	ns
t7	RxData(7-0), RxSOC Hold Time from RxClk	1	—	ns
t8	Rx_Ctrl_In Setup Time to RxClk	10	—	ns
t9	Rx_Ctrl_In Hold Time from TxClk	0	—	ns

5350 tbl 15

UTILITY BUS WRITE CYCLE (SEE FIGURE 4)

Symbol	Parameter	Min.	Max.	Unit
tw1	UTL_ALE Pulse Width	25	—	ns
tw2	$\overline{\text{UTL\_CS0/1}}$ Output Valid to UTL_ALE falling edge	25	—	ns
tw3	$\overline{\text{UTL\_WR}}$ Output Valid from UTL_ALE falling edge	—	80	ns
tw4	$\overline{\text{UTL\_CS0/1}}$ Pulse Width	275	—	ns
tw5	$\overline{\text{UTL\_WR}}$ Pulse Width	185	—	ns
tw6	UTL_ALE falling edge to $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_WR}}$ rising edge	245	—	ns
tw7	UTL_AD(7-0) Address Setup Time to UTL_ALE falling edge	30	—	ns
tw8	UTL_AD(7-0) Address Hold Time from UTL_ALE falling edge	10	—	ns
tw9	UTL_AD(7-0) Data Setup Time to $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_WR}}$ rising edge	185	—	ns
tw10	UTL_AD(7-0) Data Hold Time from $\overline{\text{UTL\_CS0/1}}$, $\overline{\text{UTL\_WR}}$ rising edge	10	—	ns

5350 tbl 16

UTILITY BUS READ CYCLE (SEE FIGURE 5)

Symbol	Parameter	Min.	Max.	Unit
tr1	UTL_ALE Pulse Width	25	—	ns
tr2	$\overline{\text{UTL\_CS0/1}}$ Output Valid to UTL_ALE falling edge	25	—	ns
tr3	$\overline{\text{UTL\_RD}}$ Output Valid from UTL_ALE falling edge	—	80	ns
tr4	$\overline{\text{UTL\_CS0/1}}$ Pulse Width	275	—	ns
tr5	$\overline{\text{UTL\_RD}}$ Pulse Width	185	—	ns
tr6	UTL_ALE falling edge to $\overline{\text{UTL\_RD}}$ rising edge	250	—	ns
tr7	UTL_AD(7-0) Address Setup Time to UTL_ALE falling edge	30	—	ns
tr8	UTL_AD(7-0) Address Hold Time from UTL_ALE falling edge	10	—	ns
tr9	UTL_AD(7-0) Data Setup Time to $\overline{\text{UTL\_CS0/1}}$ rising edge	80	—	ns
tr10	UTL_AD(7-0) Data Hold Time from $\overline{\text{UTL\_CS0/1}}$ rising edge	10	—	ns
tr11	UTL_ALE falling edge to $\overline{\text{UTL\_CS0/1}}$ rising edge	225	—	ns

5350 tbl 17

SRAM BUS WRITE CYCLE (SEE FIGURE 6)

Symbol	Parameter	Min.	Max.	Unit
t1	SR_A(13-0) Setup Time to $\overline{SR\_WE}$ falling edge	2	----	ns
t2	$\overline{SR\_CS}$ falling edge to $\overline{SR\_WE}$ falling edge	0	----	ns
t3	$\overline{SR\_CS}$ pulse width	25	----	ns
t4	SR_I/O(31-0) Setup Time to $\overline{SR\_WE}$ rising edge	11	----	ns
t5	SR_I/O(31-0) Hold Time from $\overline{SR\_WE}$ rising edge	7	----	ns
t6	$\overline{SR\_WE}$ pulse width	10	----	ns

5350 tbl 18

SRAM BUS READ CYCLE (SEE FIGURE 7)

Symbol	Parameter	Min.	Max.	Unit
t1	SR_A(13-0) to SR_I/O(31-0) Valid	—	15	ns
t2	$\overline{SR\_OE}$ pulse width	25	—	ns

5350 tbl 19

Note : SR_I/O (31 - 0) Setup and Hold times are guaranteed by design when t1 access time is met.

EPROM (SEE FIGURE 8)

Symbol	Parameter	Min.	Max.	Unit
t1	SR_I/O(7-0) Hold Time from $\overline{E\_CE}$ rising edge	0	----	ns
t2	$\overline{E\_CE}$ pulse width	75	----	ns
t3	SR_A(13-0) Change to SR_I/O(7-0) Valid	----	70	ns
t4	SR_A(13-0) pulse width	75	----	ns

5350 tbl 20

EEPROM (SEE FIGURE 9)

Symbol	Parameter	Min.	Max.	Unit	Comments
t1	SAR_CLK to Output Signal Valid Delay: EECS, EEDO, EECLK	100	----	ns	software controlled
t2	EEDI Input Setup Time to SAR_CLK	10	----	ns	software controlled
t3	EEDI Input Hold Time from SAR_CLK	0	----	ns	software controlled

5350 tbl 21

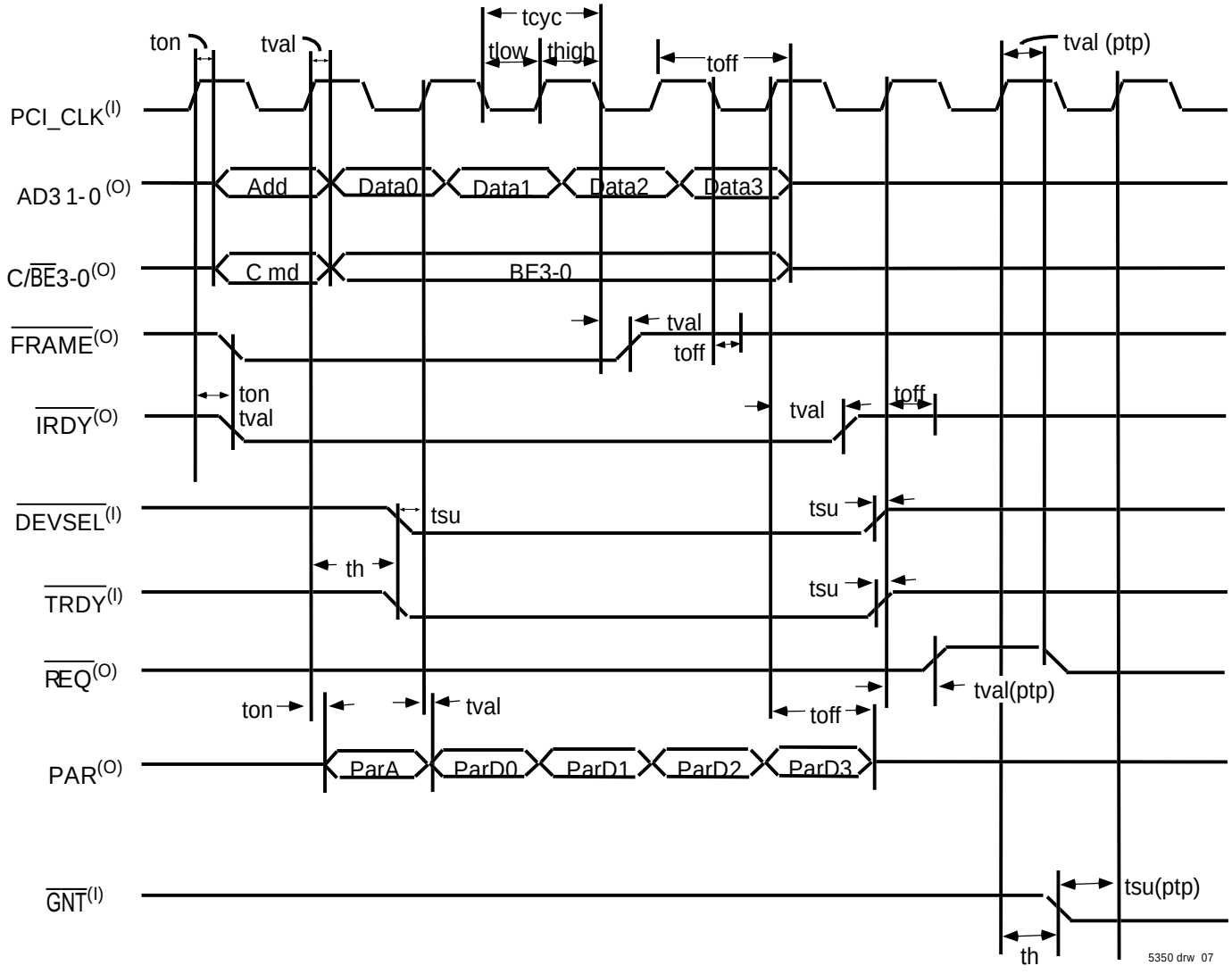


Figure 1. The ABR SAR as a PCI master (illustrates a 4-word write by the ABR SAR to host memory)

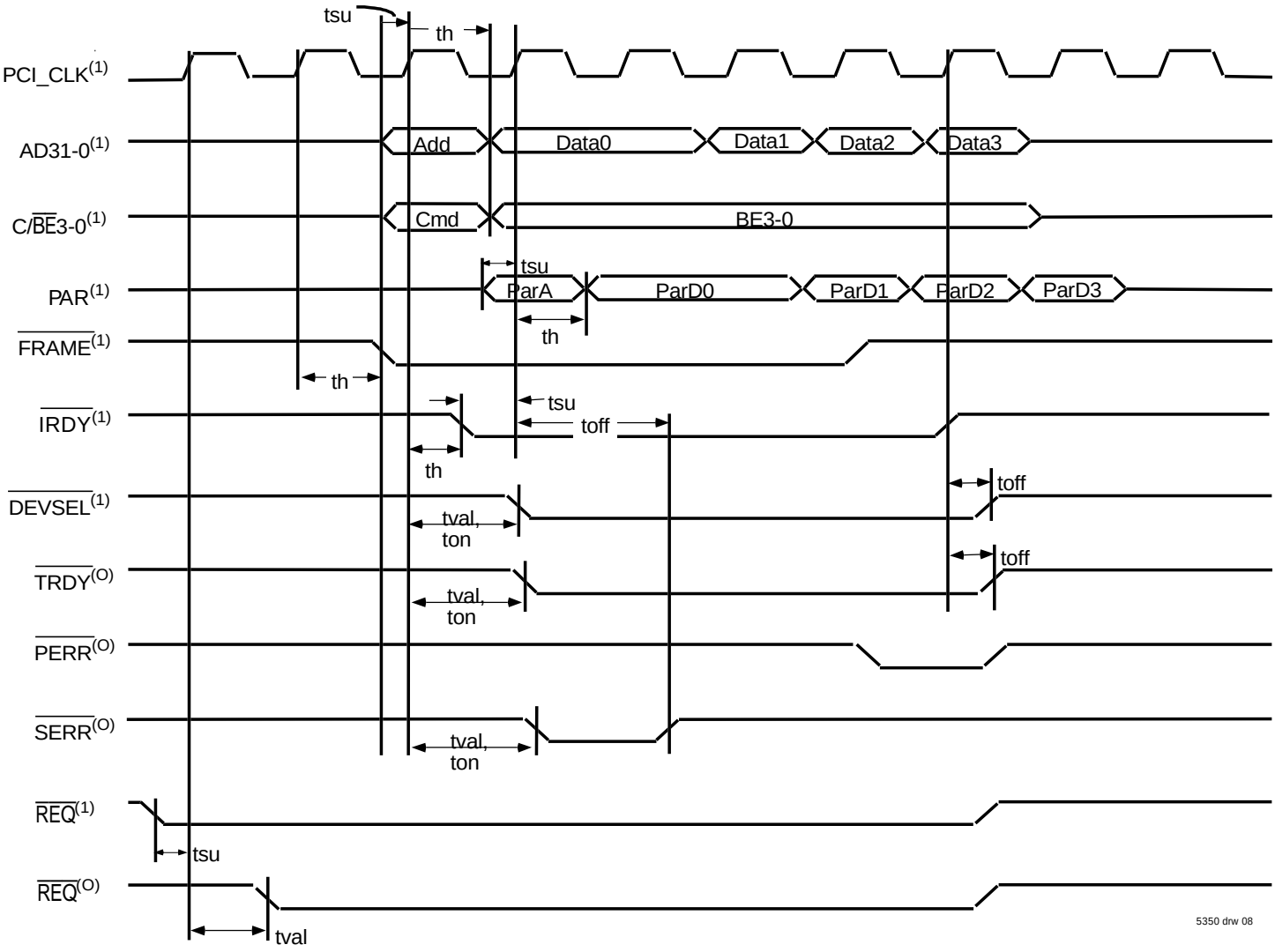


Figure 2. The ABR SAR as a PCI target
(illustrates a 4-word write operation by the host device driver to the ABR SAR)

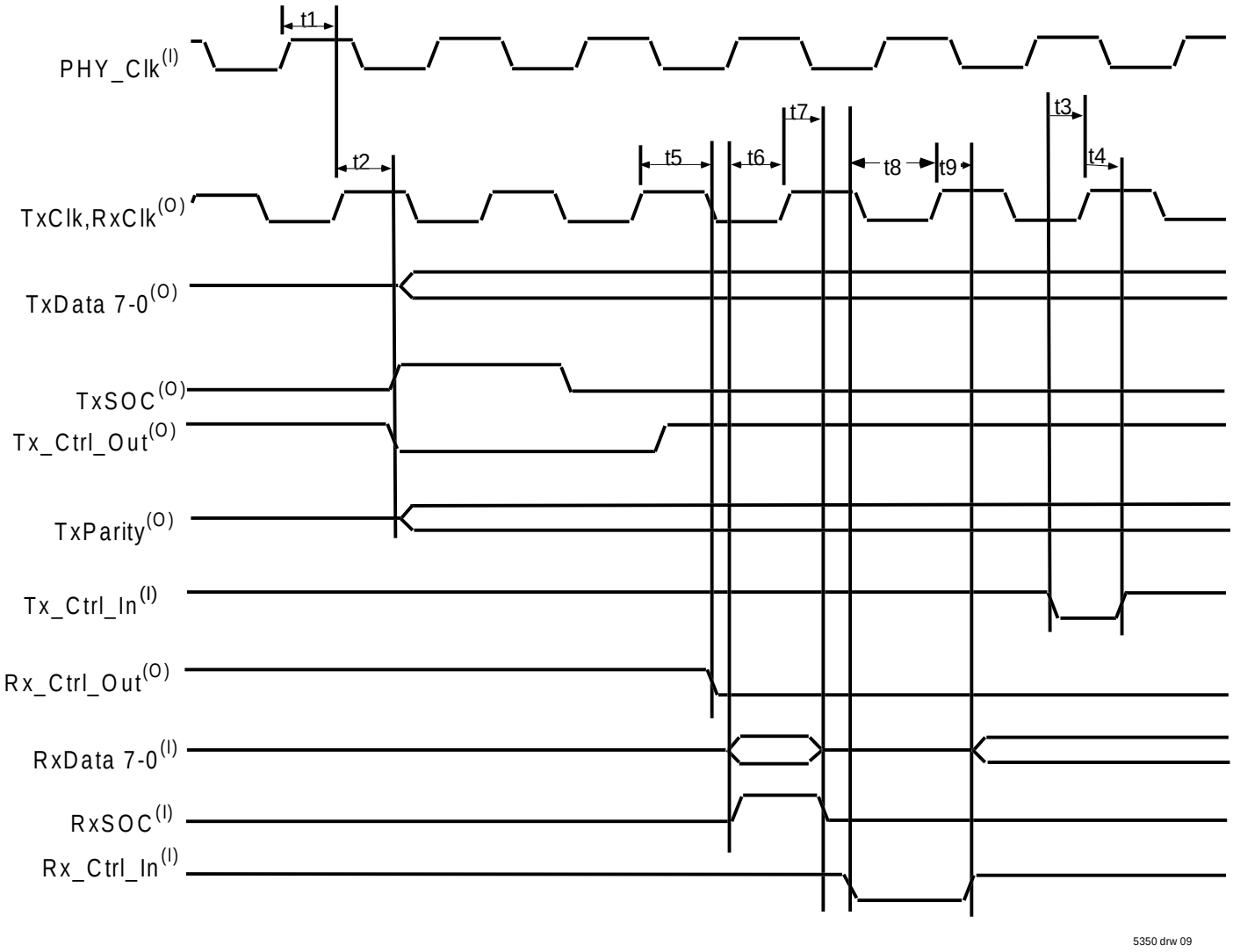


Figure 3. UTOPIA Bus Timing

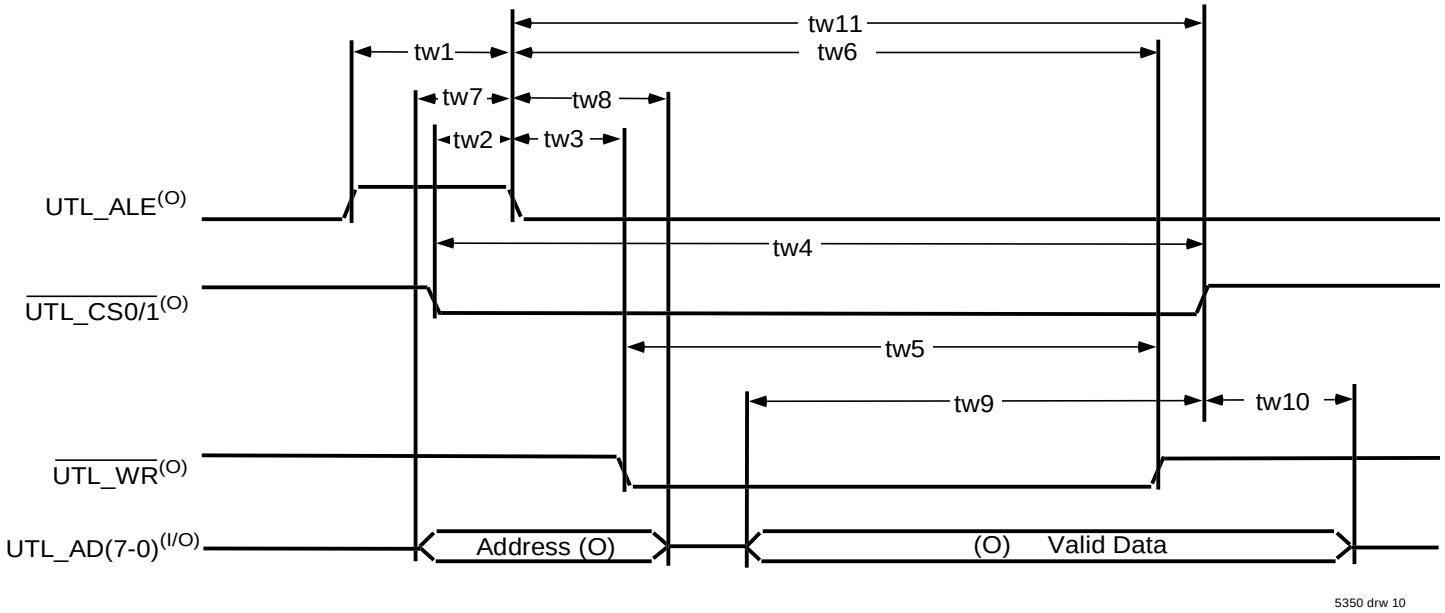


Figure 4. Utility Bus Write Cycle

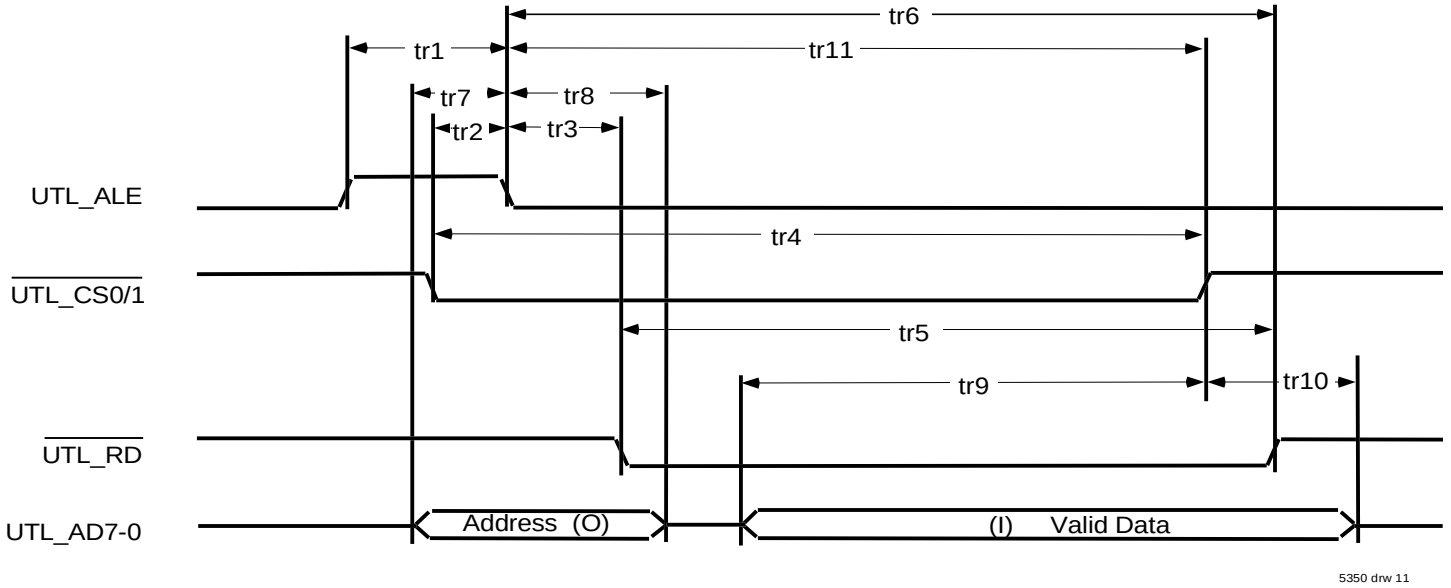


Figure 5. Utility Bus Read Cycle

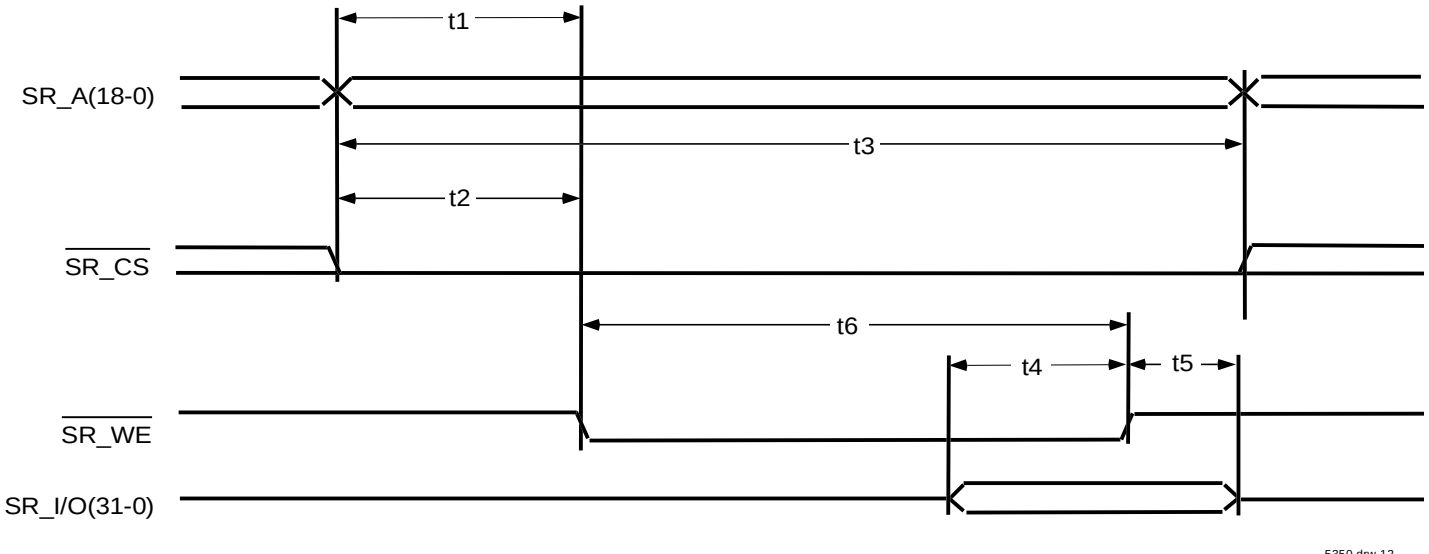


Figure 6. SRAM Bus Write Cycle Timing

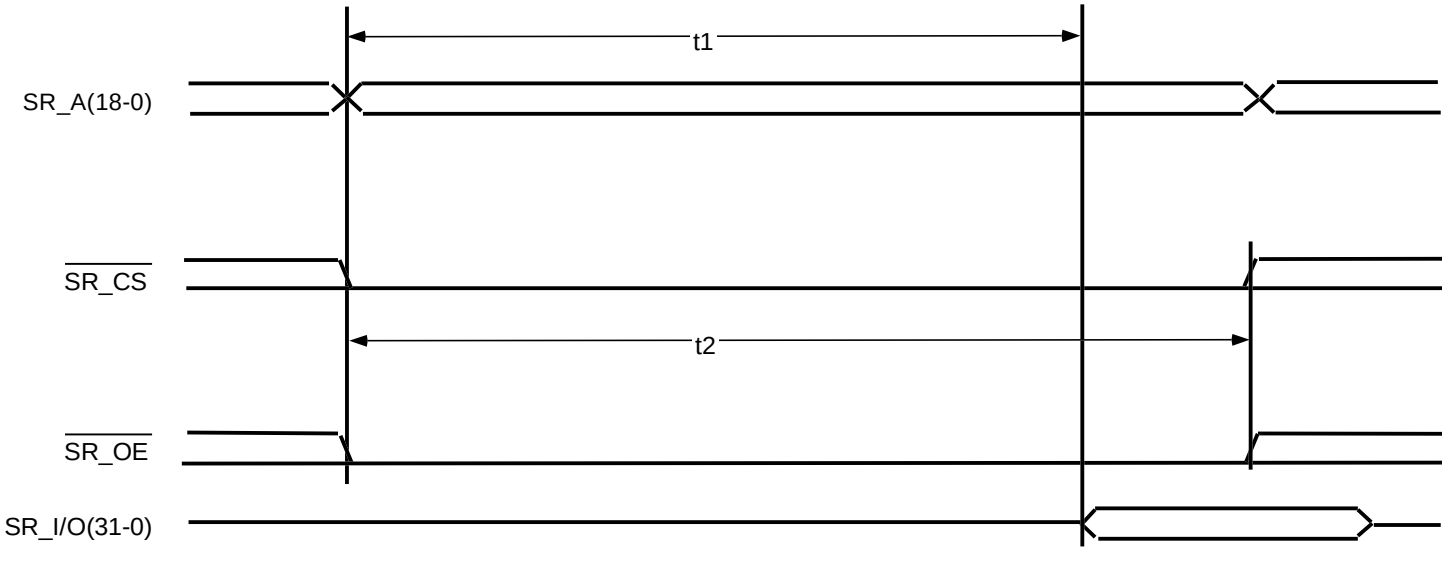


Figure 7. SRAM Bus Read Cycle Timing

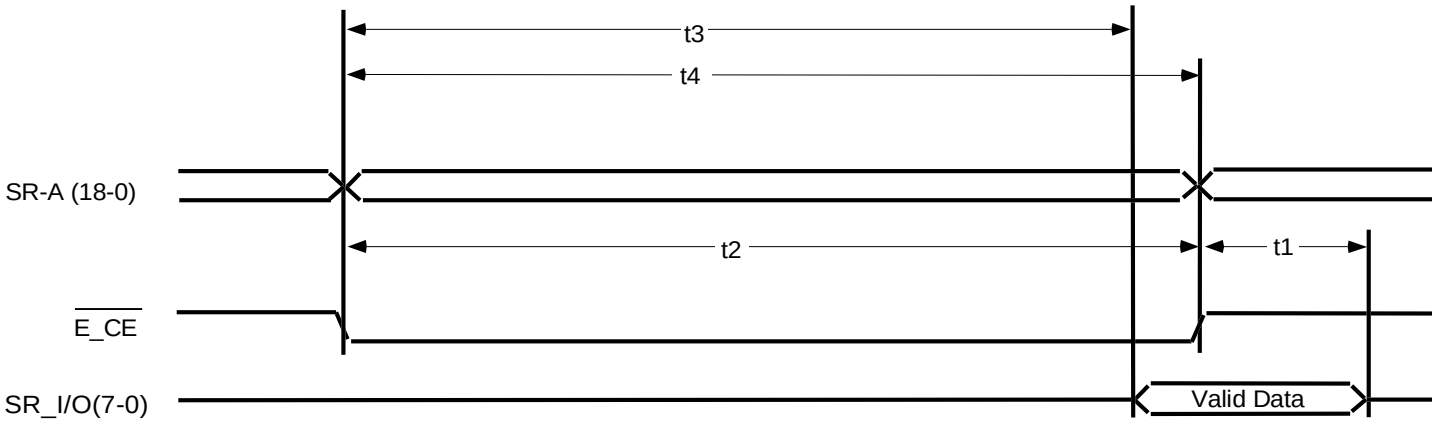


Figure 8. EPROM Timing

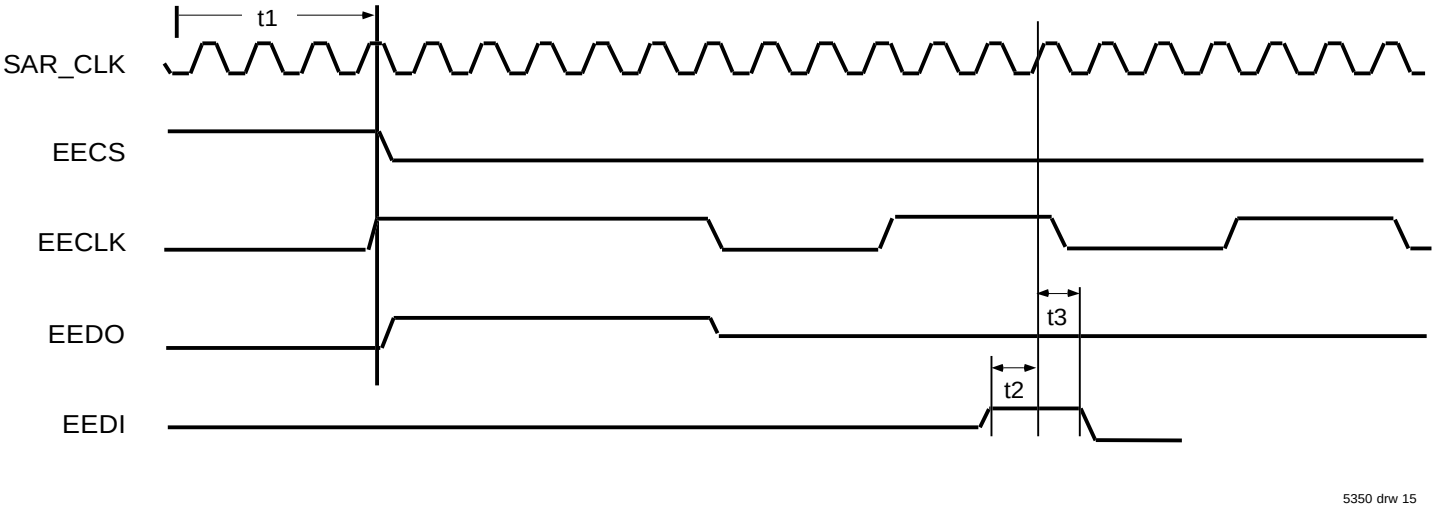


Figure 9. EEPROM Timing

´SOFTWARE AND SOFTWARE DRIVERS

Several software vendors have writen IDT77V252 software drivers for various operating systems. Please contact your local IDT sales representative for a vendor list, or e-mail atmhelp@idt.com.

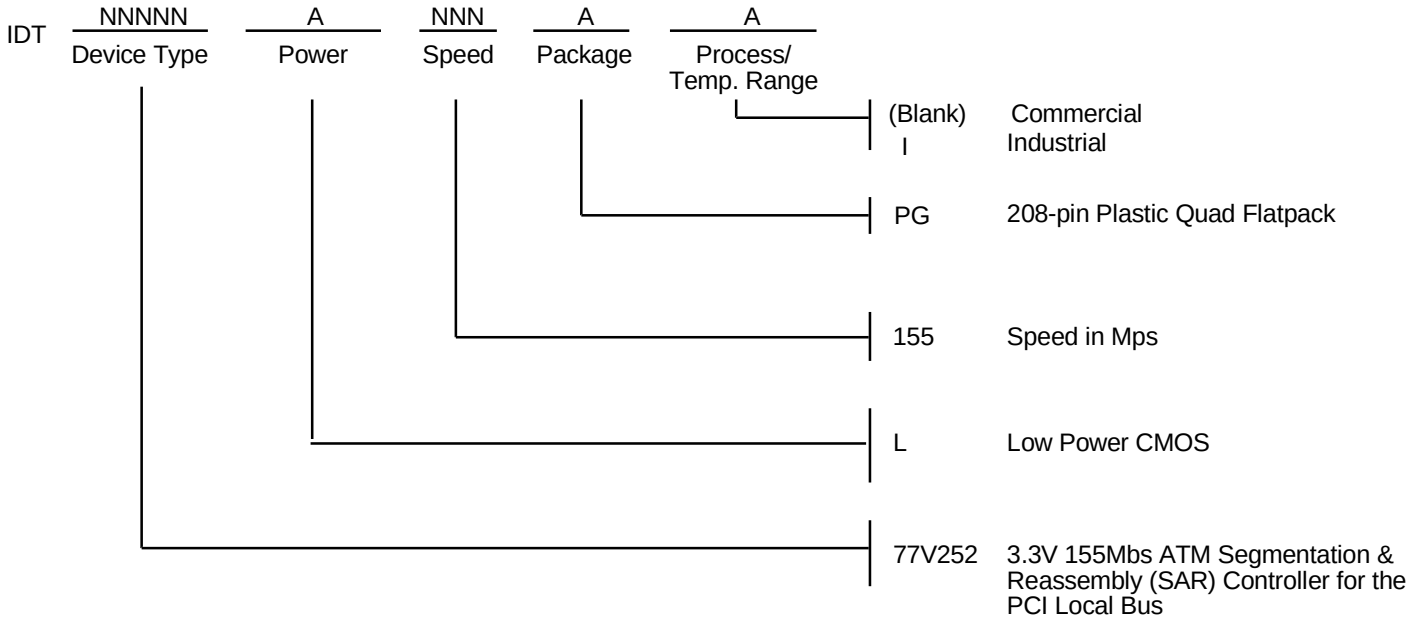
IDT offers the Sarwin2 demo driver and application suite, which can be used to evaluate the IDT77V252 when used with a IDT NIC reference or evaluation adapter. It may also be used as a reference for sample source code when developing a proprietary device driver. Please contact your IDT sales representative or e-mail atmhelp@idt.com to obtain a free cdrom.

NIC Reference and Evaluation Adapters

NIC Reference and Evaluation adapters are available in several form factors. Bill of Materials (BOM) and schematics are available upon request for each of the NIC adapters. A list of current NIC adapter offerings can be found at www.idt.com.

Note: The ABR SAR User Manual provides a detailed description of the 77V252 operation and registers.

ORDERING INFORMATION



5350 drw 16

Notes:

Refer to PSC-4053 for detailed package drawing.

Refer to errata list for revision history and how to identify revision.

Datasheet Document History

09/29/99: Created New Document

01/10/00: Changed VIH from Vcc+0.3 to 5.5V to reflect 5.5V tolerant Inputs.

03/27/00: Corrected pins 173 and 200 in 5350drw03.

04/11/00: Corrected table 5350tbl12.

04/26/00: Added information in Pin Description for TxCLK and RxCLK.

06/19/00: Corrected pin descriptions for pins 174, 189 and 199. Changed DC Operating conditions for Vil and Vih. Updated AC Test Conditions table and drawing. Updated UTOPIA Bus, Utility Bus Read and Write, SRAM Bus Read and Write, and EEPROM timing diagrams and tables. Changed data sheet from Advanced to Preliminary.

08/25/00: Updated UTOPIA Bus timing table.

10/06/00: Corrected Utopia Slave mode drawing 5351drw06 and added Max Cout parameter in Table 5350tbl09. Additional changes made to reflect Rev B silicon include changed Test[1] from pin 201 to pin 200, changed Test[0] from pin 200 to pin 201, changed bit order for Test[1:0] in Test Mode table 5351tbl12, removed PCI timing violation for "th" hold time.

01/16/01: Changed from Preliminary to Final data sheet. Added to and rearranged the Features list.

Integrated Device Technology, Inc. reserves the right to make changes to the specifications in this data sheet in order to improve design or performance and to supply the best possible product.

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-330-1748
www.idt.com

for Tech Support:
408-330-1752
sarhelp@idt.com

The IDT logo is a registered trademark of Integrated Device Technology, Inc.