Heathrow™ – 16 port Gigabit Ethernet Switch-On-A-Chip

PRELIMINARY - SUBJECT TO CHANGE

Overview

Targeted at desktop/workgroup LAN connectivity, Heathrow offers a high level of integration and performance for Gigabit Ethernet switch applications.

Heathrow provides non-blocking, wire-speed, Gigabit performance on all ports. The internal switching engine can process 32 Gbit/s and forward 24 million packets per second.

The on-chip switching engine, with filtering/forwarding functions and queuing capabilities, eliminates any requirements for external memory devices in the system design.

Unmanaged designs are possible by utilizing an external low-cost micro controller for configuration purposes. A serial peripheral interface (SPI) allows Heathrow to be monitored and configured.

In addition, the Layer-2 switching engine provides full wire-speed automatic Media Access Control (MAC) address learning. The chip also supports programmable higher layer classification and prioritization, thus enabling enhanced Quality of Service (QoS) support for real time applications such as Voice over Internet Protocol (VoIP).

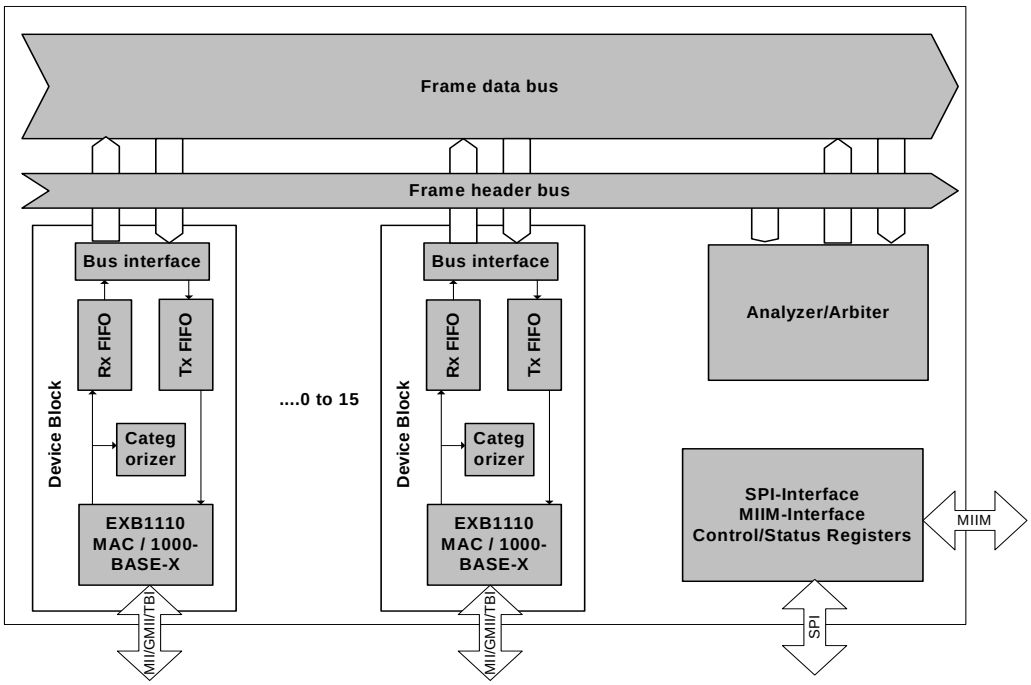

Figure 1 - Heathrow Block Diagram

Heathrow features 16 ports that each can be configured in the following manner:

- Triple-speed port for Copper PHYs with MII/GMII interface
- TBI port for optical transceivers

Key Features

- 16 Gigabit Ethernet ports with non-blocking wire-speed performance
- 32 Gbit/s internal switching bandwidth, 24 Mp/s forwarding rate
- Triple speed (10/100/1000) operation via MII/GMII/TBI interface
- Unmanaged Layer-2 switching is possible
- 256 KB On-chip frame buffer
- Programmable classifier for QoS (Multimedia)
- 4k MAC addresses
- Full duplex flow control (IEEE802.3x) and half duplex back pressure
- Priority based packet discard
- Flexible Link Aggregation based on IEEE802.3ad
- 4k VLAN support and support for Spanning Tree Protocol
- Store and forward based on Destination MAC address
- Statistics Counters

Functional Description

Heathrow operates as a VLAN aware Layer-2 switch. It forwards frames at Layer-2 based on information up to, and including, Layer-4.
Heathrow automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming frames. If the Source Address is not already known, Heathrow adds it to the MAC address table.
The header information in the frames is used by Heathrow to prioritize, forward, and filter the Frames.

A serial microprocessor interface is offered for monitoring and configuration of the switch (a 4-wire SPI interface). The status registers support statistics counters. The SPI interface gives access to capture and transmit Spanning Tree Protocol packets.

The main components of Heathrow are a Device Block and an Analyzer/Arbiter Block, as shown in Figure 1.

Device Block Architecture Description

The purpose of the Device Block is to receive frames from the Ethernet and transmit frames from the internal modules to the Ethernet port. When the MAC receives an incoming frame it is given a priority by the Categorizer and stored in the Rx-FIFO. The outgoing frames are stored in the Tx-FIFO and transmitted by the MAC.

The MAC functionality is provided by the MII/GMII receiver (RX) and transmitter (TX). In addition to this block, the MAC also consists of a full-duplex flow control

module (‘Pause’).

The Exbit EXB1000BASE-X core provides connectivity between the MAC layer via the Gigabit Medium Independent Interface (GMII) to the Physical Medium Attachment (PMA) layer. Using the core enables connection between the Exbit EXB1110 triple speed MAC and a Fiber Channel PHY device as described in ANSI X3.230-1994 (FC PH).

The connection between the MAC and the PHY is a MII/GMII or TBI interface.

Analyzer/Arbiter Block Architecture Description

The Analyzer/Arbiter Block is responsible for making the forwarding decision in the Heathrow switching system. The Analyzer receives frame information from the input devices and feeds the resulting forwarding decisions to the Arbiter.

At the same time, the incoming Source MAC and VLAN ID address is matched against the address table. If it is not known, it is inserted along with the associated port in the address table.

In addition to the normal backwards learning implemented by the algorithm described above, the external controller can also lock entries in the address table for special reasons, e.g. addresses and/or security.

The Analyzer also handles ingress and egress port aggregation. Two, four, or eight ports can be aggregated, with a frame distribution function based on either just the source MAC address or a combination of the Source and Destination MAC addresses.

The scheduler handles backpressure from congested output devices.

Application Example

The following example shows how to design a low cost 16-port Gigabit Ethernet Switch with only one Heathrow chip and four 10/100/1000 Quad-PHYs.

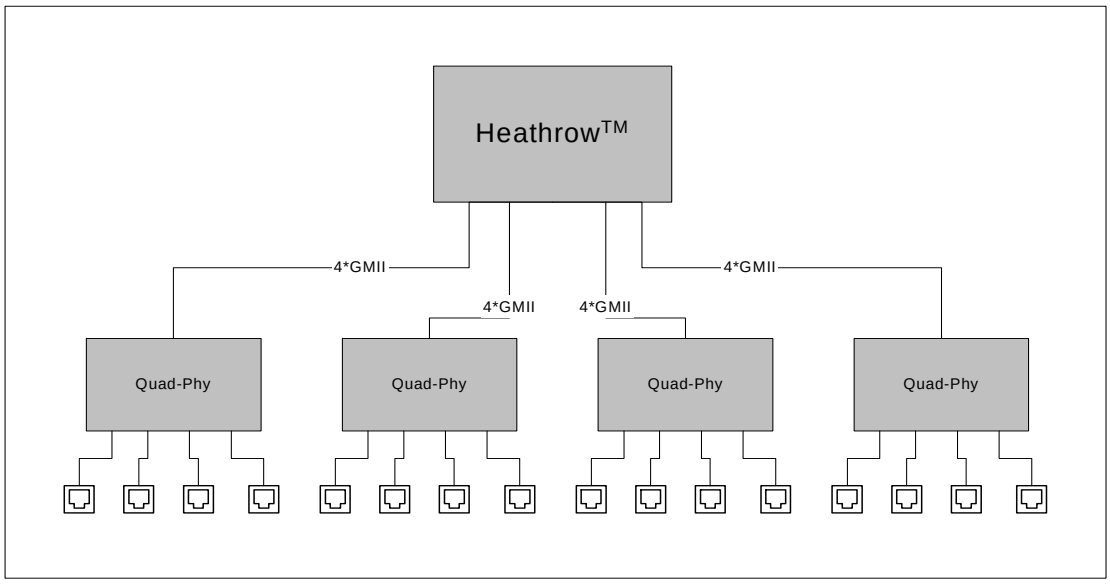

Figure 2 - 16 port Gigabit Ethernet Switch

Interface Description

Group	Port	I/O	Description
GMII [0-15]	GMII_TX_CLK	O	GMII transmit clock
	GMII_TX_EN	O	GMII transmit enable
	GMII_TXD[7-0]	O	GMII transmit data
	GMII_TX_ER	O	GMII transmit error
	GMII_RX_CLK	I	GMII receive clock
	GMII_RX_DV	I	GMII receive data valid
	GMII_RXD[7-0]	I	GMII receive data
	GMII_RX_ER	I	GMII receive error
	GMII_COL	I	GMII collision detected
	GMII_CRS	I	GMII carrier sense
MIIM	MIIM_MDC	O	Management data clock
	MIIM_MDIO	I/O	Management data
SPI	SPI_EN	I	SPI Enable
	SPI_DI	I	SPI data in
	SPI_CLK	I	SPI clock
	SPI_DO	O	SPI data out
JTAG	JTAG_RST	I	JTAG Reset
	JTAG_TCK	I	JTAG Clock
	JTAG_TMS	I	JTAG Test mode select
	JTAG_TDI	I	JTAG Test data in
	JTAG_TDO	O	JTAG Test data out

Specification Summary

Packaging	Heathrow chip comes in a 720 pin plastic TAB-BGA
Package Width x Length	40.00 x 40.00 mm
Power	Power dissipation < 4w
Lead Pitch	1.00 mm