GaAs MMIC +3V TRANSMIT / RECEIVE SWITCH DC - 2.0 GHz

FEBRUARY 2001 v01.0700

Features

LOW INSERTION LOSS: 0.6 dB

ULTRA SMALL PACKAGE: SOT26

HIGH INPUT P1dB : +35 to +38dBm

HIGH INPUT IP3 : +55 to +61 dBm

POSITIVE CONTROL: 0/+3V to 0/+8V

General Description

The HMC226 is a low-cost SPDT switch in a 6-lead SOT26 package for use in transmit-receive applications which require very low distortion at high signal power levels. The device can control signals from DC to 2.0 GHz and is especially suited for 450 MHz, 900 MHz and 1.8-2.0 GHz applications with 0.5 to 0.8 dB loss. The design provides exceptional P1dB and intermodulation performance; a +35 dBm 1 dB compression point and +55 dBm third order intercept at +3 volt bias. RF1 or RF2 is a reflective short when "Off". On-chip circuitry allows single positive supply operation at very low DC current with control inputs compatible with CMOS and most TTL logic families. Applications include ISM/Cellular 900 MHz and PCS 1900 MHz devices.

Guaranteed Performance *Vctl = 0/+3 Vdc, 50 Ohm System, -40 to +85 deg C*

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		DC - 0.5 GHz DC - 1.0 GHz DC - 2.0 GHz		0.5 0.6 0.8	0.8 0.9 1.2	dB dB dB
Isolation		DC - 0.5 GHz DC - 1.0 GHz DC - 2.0 GHz	23 17 12	26 20 15		dB dB dB
Return Loss		DC - 0.5 GHz DC - 1.0 GHz DC - 2.0 GHz	23 21 14	27 25 18		dB dB
Input Power for 1dB Compression	0/5V Control 0/3V Control	0.3 - 2.0 GHz	34 31	38 35		dBm
Input Third Order Intercept (Two-tone Input power = +26 dBm each tone)	0/5V Control 0/3V Control	0.3 - 2.0 GHz		61 55		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		DC - 2.0 GHz		 70 140		 nS nS

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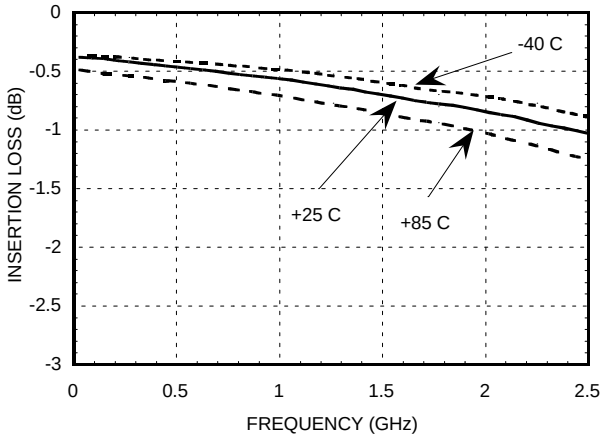
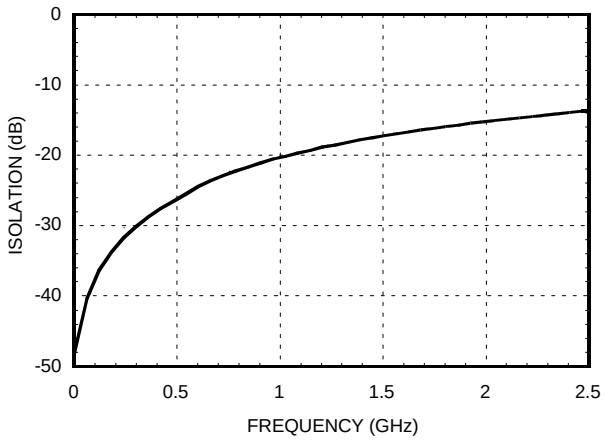
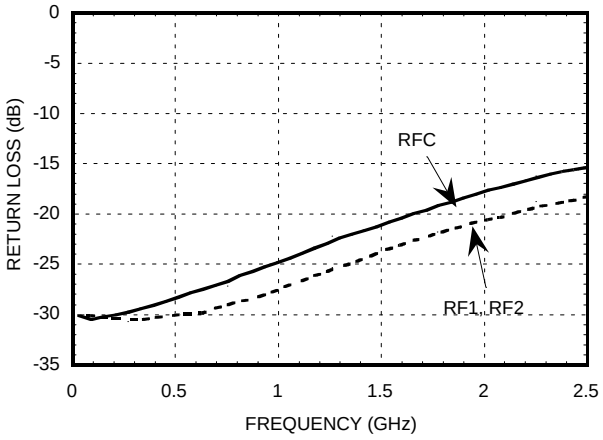
Insertion Loss vs Temperature



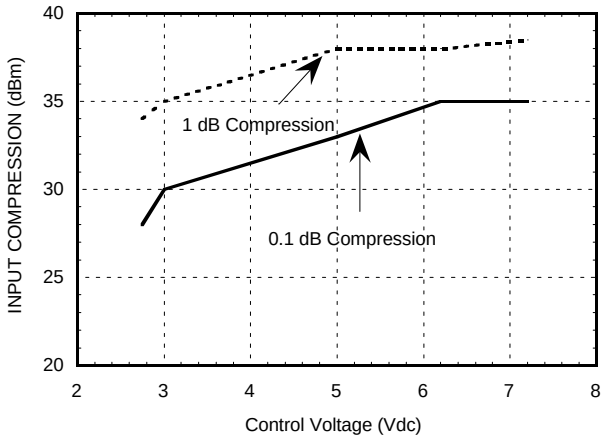
Isolation



Return Loss



Input 0.1 and 1.0 dB Compression vs Control Voltage @ 900 MHz



Compression vs Control Voltage @ 900 MHz

Control Input	Input Power for 0.1 dB Compression	Input Power for 1 dB Compression
(Vdc)	(dBm)	(dBm)
+3	30	35
+5	33	38
+7	35	38.5

Caution: Do not operate continuously at power levels > 1 db compression and do not 'hot switch' power levels greater than +23dBm (V_{CTL} = +3Vdc).

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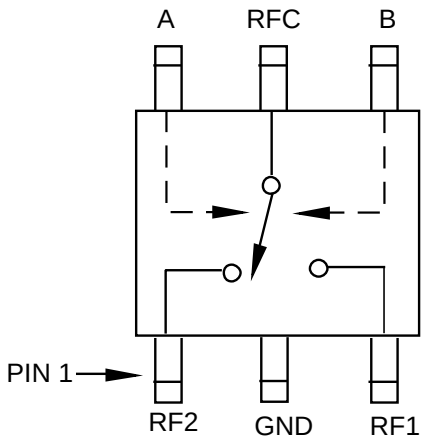
Functional Diagram



Truth Table

Control Input Tolerances are +/- 0.2 Vdc

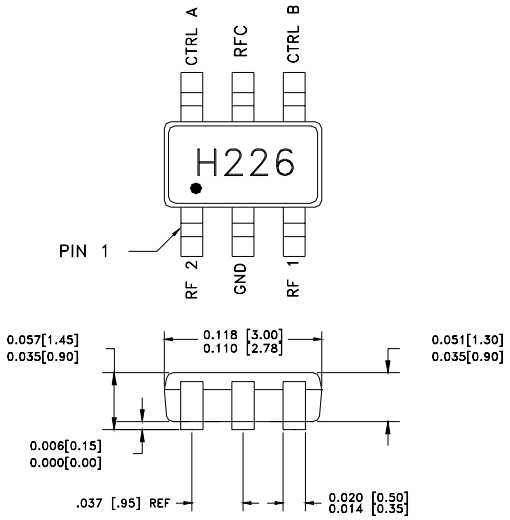
Control Input *		Control Current		Signal Path	
A (Vdc)	B (Vdc)	Ia (uA)	Ib (uA)	RF to RF1	RF to RF2
0	+3	-5	5	On	Off
+3	0	5	-5	Off	On
0	+5	-10	10	On	Off
+5	0	10	-10	Off	On
0	+8	-45	45	On	Off
+8	0	45	-45	Off	On

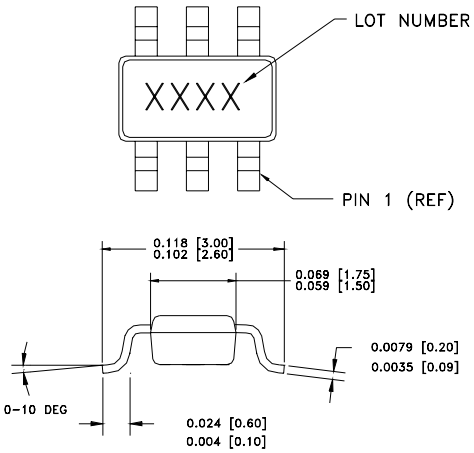
DC blocks are required at ports RFC, RF1 and RF2.

Absolute Maximum Ratings

Max. Input Power (V_{CTL} = 0/+3V) 0.05 GHz 0.5 - 2 GHz	+27 dBm +36 dBm
Control Voltage Range (A & B)	-0.2 to +12Vdc
Storage Temperature	-65 to +150 deg. C
Operating Temperature	-40 to +85 deg. C

Outline Drawing





1) MATERIAL:
A) PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED
B) LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS)
UNLESS OTHERWISE SPECIFIED TOL. ARE ±0.005(±0.13)

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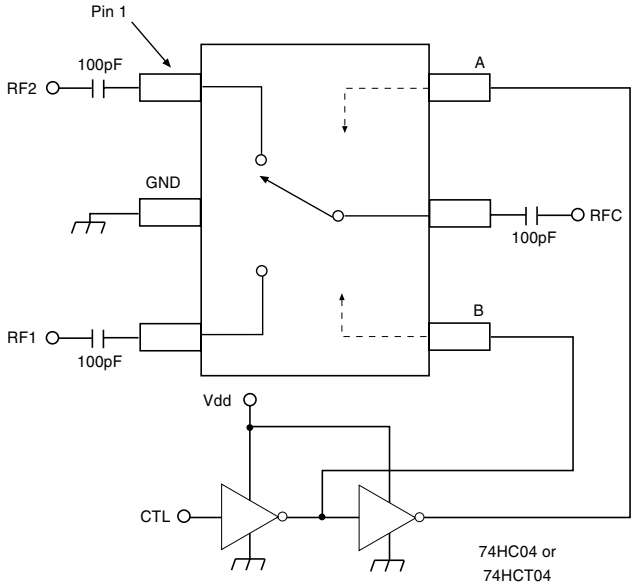
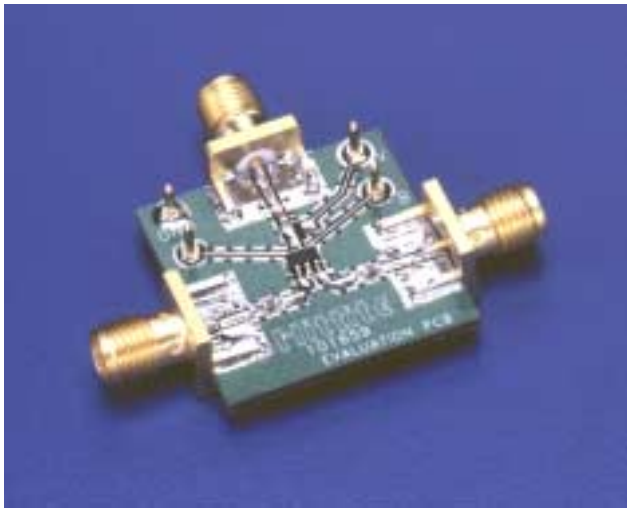
Typical Application Circuit



Notes:

1. Set logic gate and switch Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of 3 to 8 Volts applied to the CMOS logic gates and to pin 4 of the RF switch.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with V set to +10V. The switch will operate properly (but at lower RF power capability) at bias voltages down to +3V.

Evaluation Circuit Board



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown below. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Hittite upon request.

Evaluation Circuit Board Layout Design Details

Layout Technique	Grounded Co-Planar Waveguide (GCPW)
Material	FR4
Dielectric Thickness	0.028" (0.71 mm)
50 Ohm Line Width	0.037" (0.94 mm)
Gap to Ground Edge	0.010" (0.25 mm)
Ground VIA Hole Diameter	0.014" (0.36 mm)
Connectors	SMA-F (EF - Johnson P/N 142-0701-806)